

Does TDECQ Capture Jitter

Addressing D1.1 comments: 67, 78, 82, 95, 182, 561, 564, 565, 571, and 577

Ali Ghiasi - Ghiasi Quantum/Marvell

Karl Muth – Broadcom

Pavel Zivny - Tektronix

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List of Supporters

- Chris Cole – Coherent**
- Phil Sun – Credo**
- Bill Simms – Nvidia.**

Overview

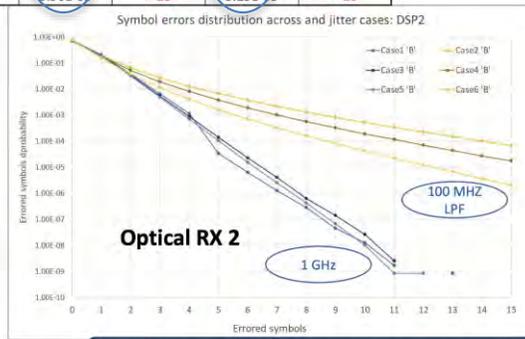
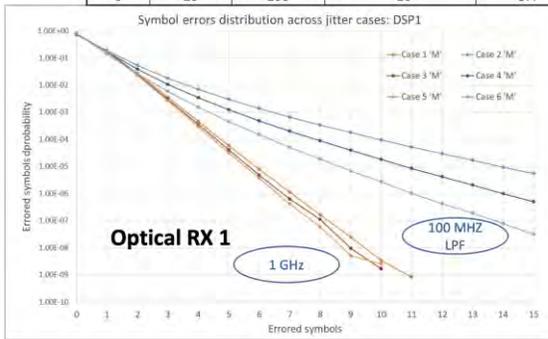
- ❑ Concern about TDECQ not capturing jitter
- ❑ Does TDECQ capture jitter
- ❑ Correlation of J_{RMS} with EECQ/TDECQ
- ❑ Background on SONET jitter generation
- ❑ Weakness in current JTOL
- ❑ What maybe the real problem
- ❑ Summary.

Concern Raised on Optical Transmit Jitter

- Concern raised that high phase noise in the 4-100 MHz may cause error floor, see [ran 3dj elec 01 240822](#)
 - What is not clear if receive DSP/modules were operated at min designed OMA or at levels lower to get a BER floor then pump concentrated RJ or SJ in the 4-100 MHz band to further degrade the error floor
 - Comparing Odd (LPF off good) vs Even (LPF on bad) cases even the use of integrated phase would be difficult to identify bad from good transmitters
 - There seem to be an issue with the measurement as the reported SNR of ~22.5 dB for filter on/off should result in much better BER than ~4E-5 irrespective of jitter!

Symbol Error Distribution SKU: NA21G

CASE	Frequency [MHz]		Random Jitter Relative Power Density	SECC [dB]	Optical RX 1		Optical RX 2	
	HPF	LPF			BER	Symbol Error	BER	Symbol Error
1	OFF	OFF	1	3.33	4.61E-05	13	3.94E-05	11
2	OFF	100	~10	3.33	5.83E-05	> 16	5.02E-05	> 16
3	20	OFF	~1	3.27	4.36E-05	11	3.77E-05	10
4	20	100	~10	3.39	4.94E-05	> 16	4.11E-05	> 16
5	10	OFF	~1	3.33	4.22E-05	12	3.64E-05	10
6	10	100	~10	3.4	3.96E-05	> 16	3.29E-05	> 16



Content provided by Marco Mazzini and Yi Tang

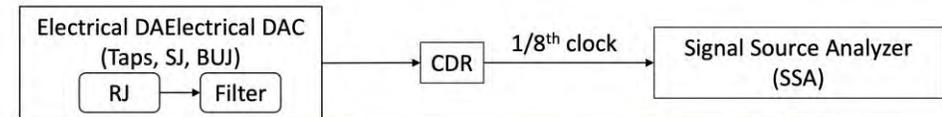
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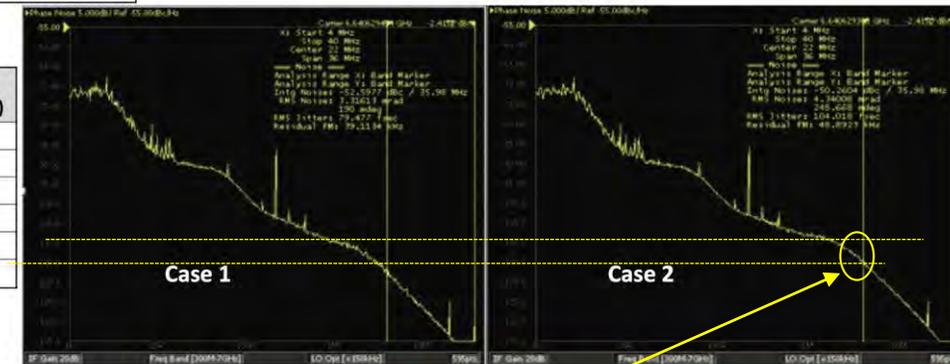
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Jitter Characterization of Test Cases



CASE	Frequency [MHz]	RJ _{RMS} [fs] (4MHz - 40MHz)
1	OFF	79.5
2	OFF	104
3	20	76
4	20	93.5
5	10	75.7
6	10	87



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Tiny amount of phase noise increase results in error floor

Does TDECQ/EECQ Capture Jitter Penalty

□ The short answer is – Yes

- All the wander and jitters due to pattern dependency, jitter multiplication, jitter peaking if data propagates from TP1 to TP2 and will get filtered by the Golden CDR and will get displayed on the scope
 - Each histogram window is 0.04 UI and the two histogram are separated by 0.1 UI
- The two histograms are measured at $4.8E-4$ but histogram confidence not defined
 - Assuming confidence level of 99% one would need to capture ~ 100 kSa (each histogram window assuming you get hit for each require only need 100 kUI)
- In today's sampling Oscopse with SSPRQ pattern typical acquisition time is ~ 3 seconds
 - J4U for sufficient confidence require 100k PRBS13Q waveform capture at sampling rate of 250 kSa/s for Oscopse will take ~ 1 hours!

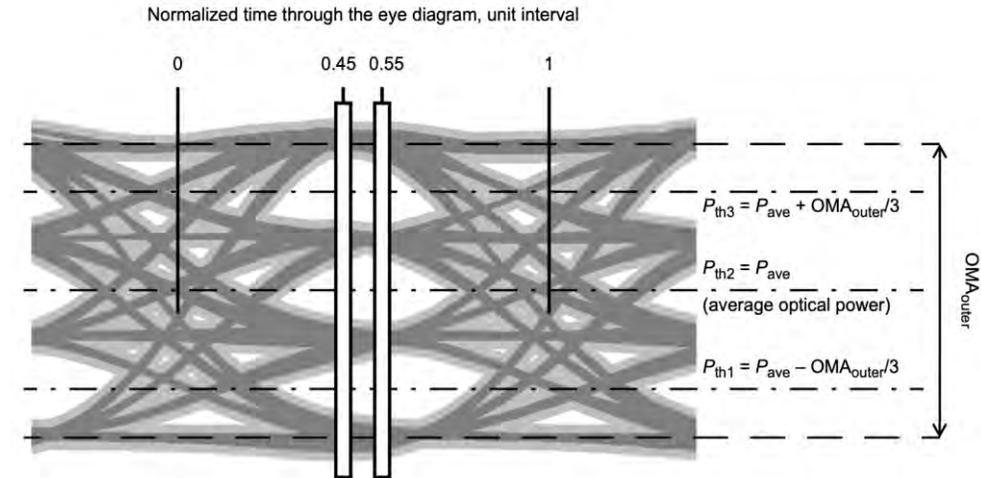
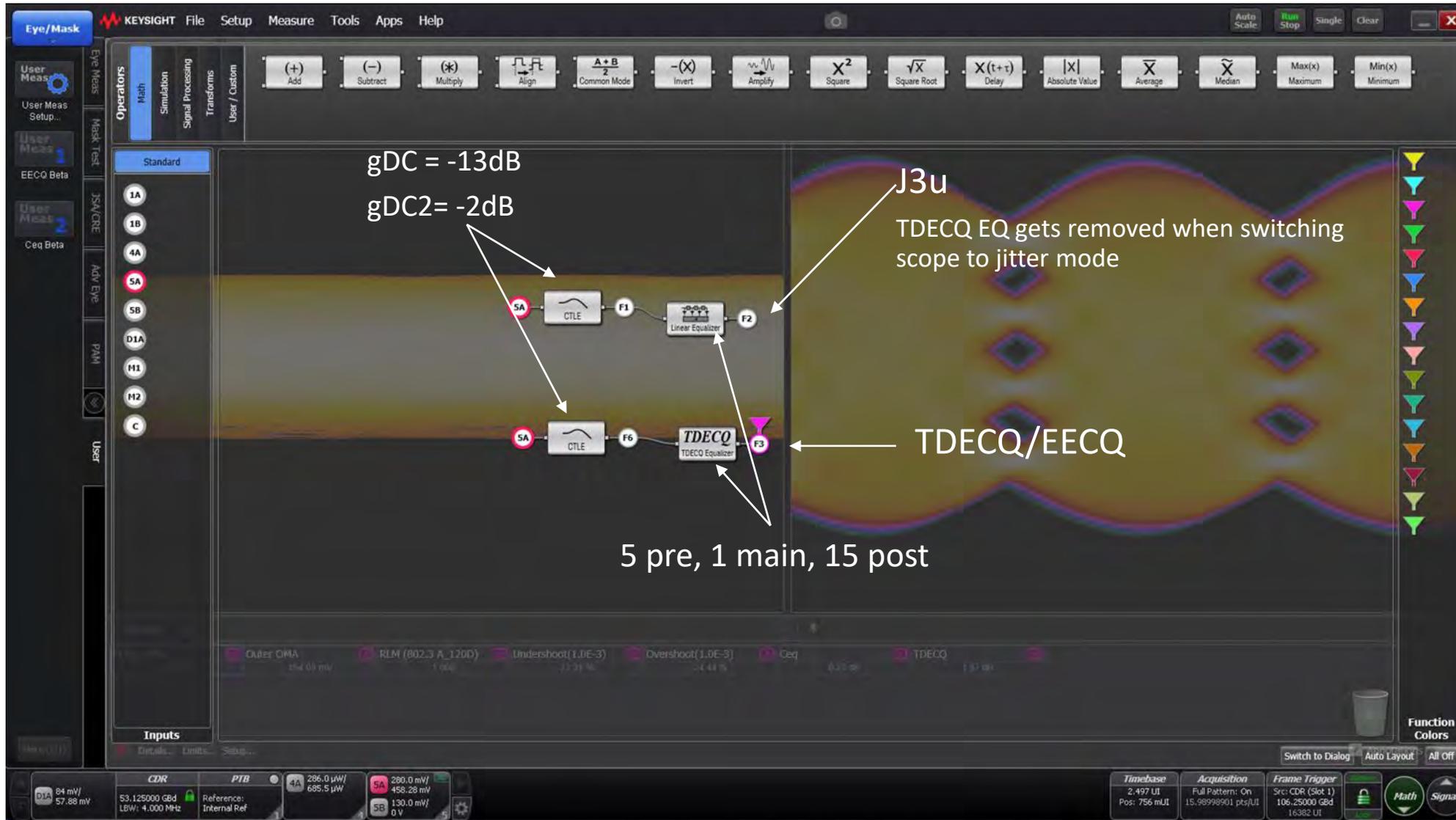


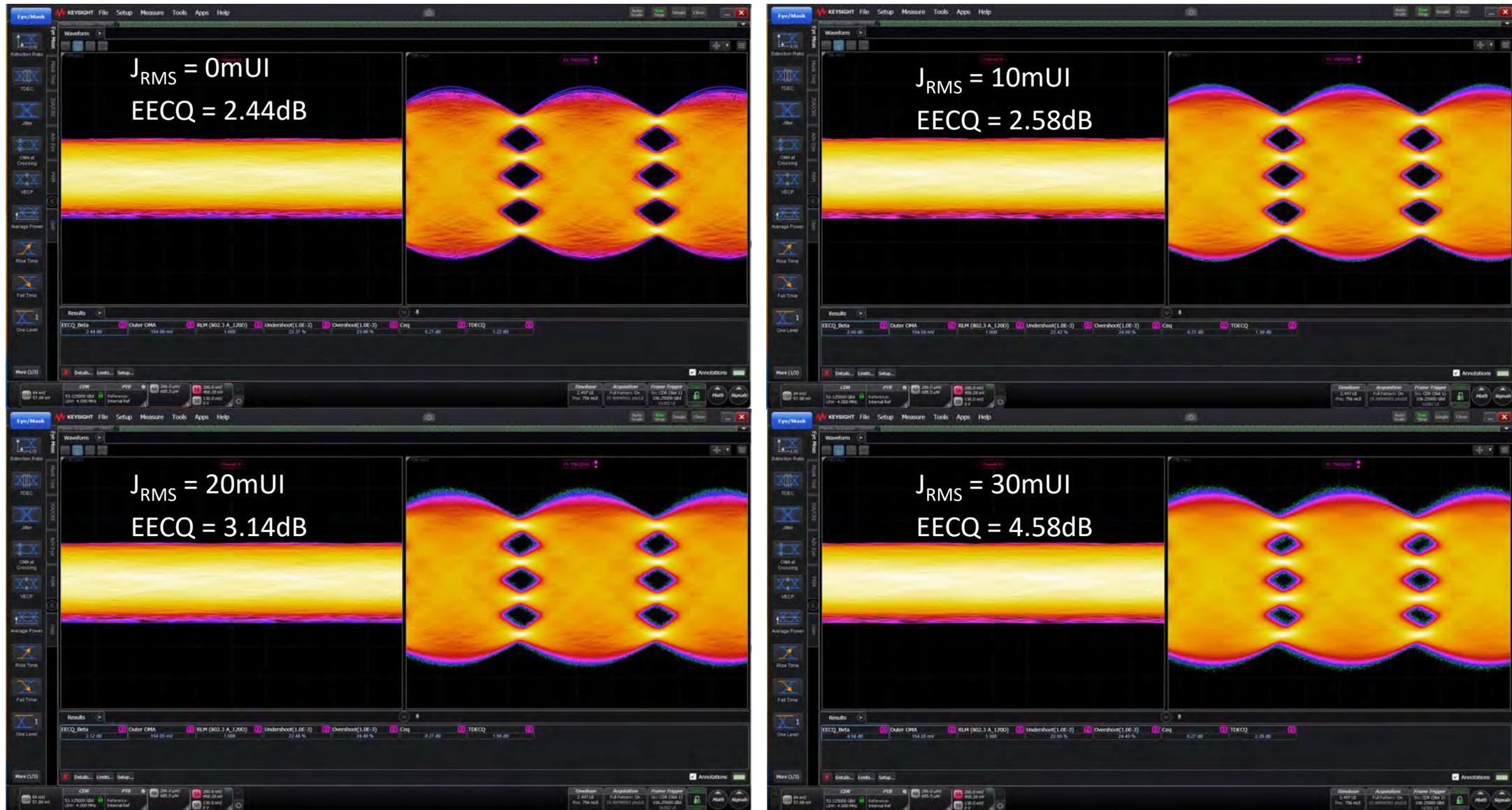
Figure 121-5—Illustration of the TDECQ measurement

Test Setup To Demonstrate Correlation of TDECQ/EECQ with Input Jitter

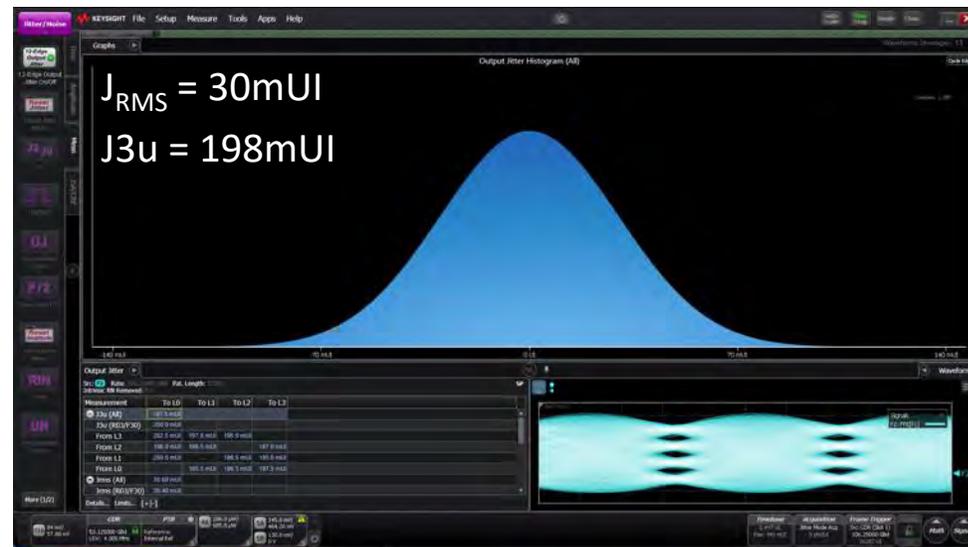
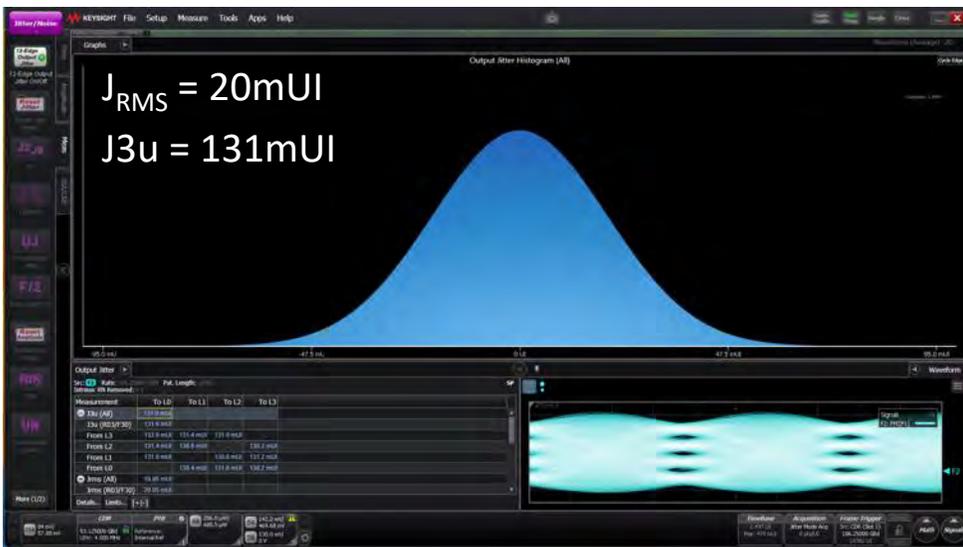
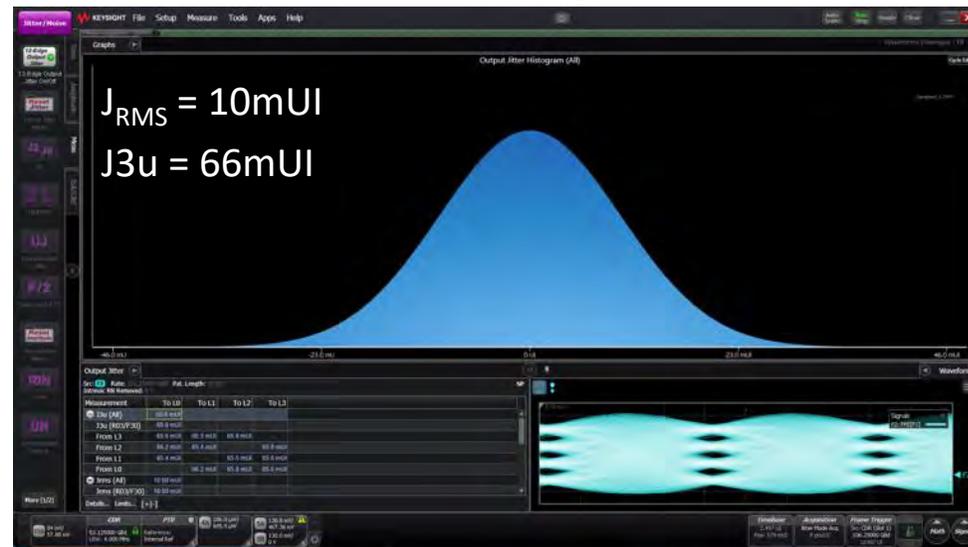
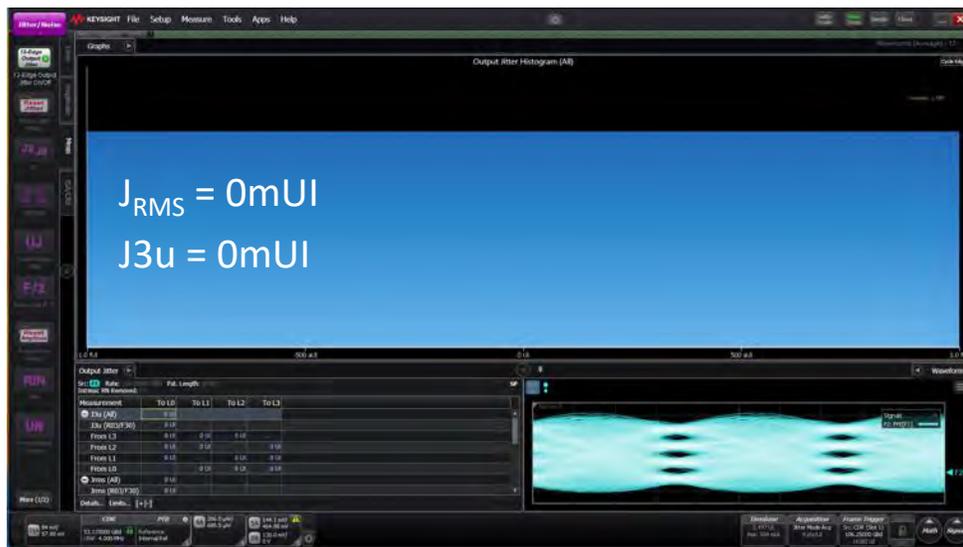


fbit = 212.5 Gb/s
PRBS13
Adding RJ in Scope
No crosstalk

Measured EECQ as Function of J_{RMS}

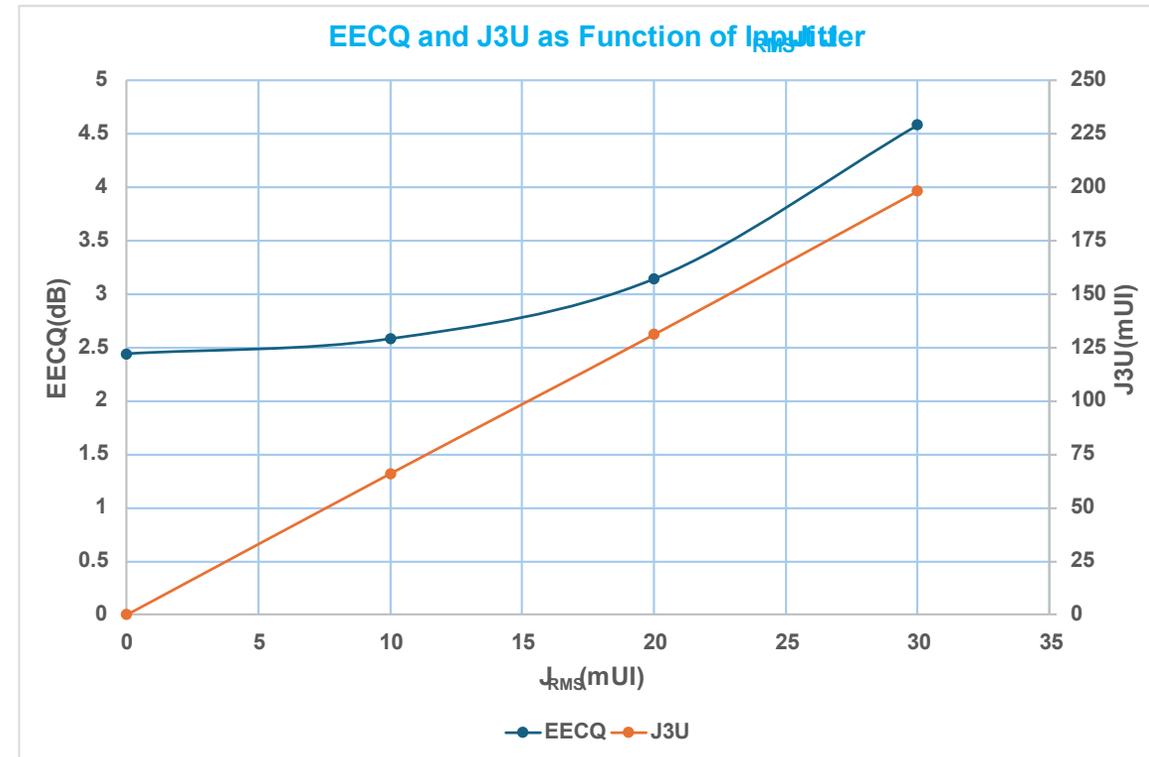


Measured J3U as Function of Input J_{RMS}



EECQ/TDECQ Correlation to Input Jitter

- ❑ Simulation show that there is strong correlation between EECQ/TDECQ and J3U as function of input J_{RMS}
 - J3U is a redundant measurement that is less effective than EECQ/TDECQ measured with a more representative SSPRQ pattern
- ❑ EECQ/TDECQ are very effective to capture jitter
 - The key is to make sure stress input applied to module input propagates to TP2 for TDECQ test otherwise jitter or impact jitter peaking will not be captured by TDECQ test or any other test!



Background on Integrated Phase Noise/RJ

- **Both SONET GR-253 and ITU-T G.709 define optical module jitter generation, transfer, and peaking considering there could be several dozens CDRs in the path for reliable network operation**
 - In XFP MSA/SNIA INF-8077i expert in the field considered both SONET and Ethernet requirements to produce a set of recommendations for the CDR/Signal conditional
 - Both SONET OC192 and 10 GbE both had 4 MHz JTOL corner frequency
 - In case of SONET there is a very tight requirement on jitter peaking and jitter generation 50 kHz-80 MHz limited to 10 mUI
 - In case of Ethernet jitter peaking is limited to 1 dB/CDR assuming 3 cascaded CDRs and there is no jitter generation
 - In case 802.3dj with 5 cascaded CDRs the jitter peaking per CDR would need to be limited to 0.6 dB.

Table 20 XFP Telecom Module Transmitter Requirement

For content of Table 20 see SNIA SFF INF-8077i
<https://members.snia.org/document/dl/26514>

Table 22 XFP Datacom Module Transmitter Requirement

For content of Table 22 see SNIA SFF INF-8077i
<https://members.snia.org/document/dl/26514>

Could SONET Jitter Generation Mitigate Burst Errors

□ SONET jitter generation for OC192 with 4 MHz corner was measured from 50 kHz-80 MHz

- In case of 100 GbE with 4 MHz the phase noise measurement would be from 40 kHz-40 MHz
- Table duplicates results presented by [ran 3dj elec 01 240822](#) but adds the RJ_{RMS} [mUI]
- Phase noise plots not clear enough to calculate the integrated phase noise from 40 kHz-40 MHz but likely these transmitters will pass SONET 10 mUI jitter generation

□ Unlikely we can come up with a discriminating transmit jitter requirements considering integrating RJ's are so close

- Ran results show that JTOL is a critical aspect of robust networks operation as there is a limit what can be done with transmit jitter testing!

Case	Frequency		RJ _{RMS} [fs] (4MHz-40MHz)	RJ _{RMS} [mUI] (4MHz-40MHz)
	HPF	LPF		
1	OFF	OFF	79.5	4.22
2	OFF	100	104	5.53
3	20	OFF	76	4.04
4	20	100	93.5	4.97
5	10	OFF	75.7	4.02
6	10	100	87	4.62

JTOL Spot Frequency Check

□ Spot frequency check can create holes in specifications especially when we have no limit for jitter peaking

- CDR designer may design around the JTOL frequencies and introduce large jitter peaks in untested bands
- JTOL need to be tested at least at every octave
- 6 test frequencies are just inadequate!

Applied sinusoidal jitter peak-to-peak amplitude (UI) (log scale)

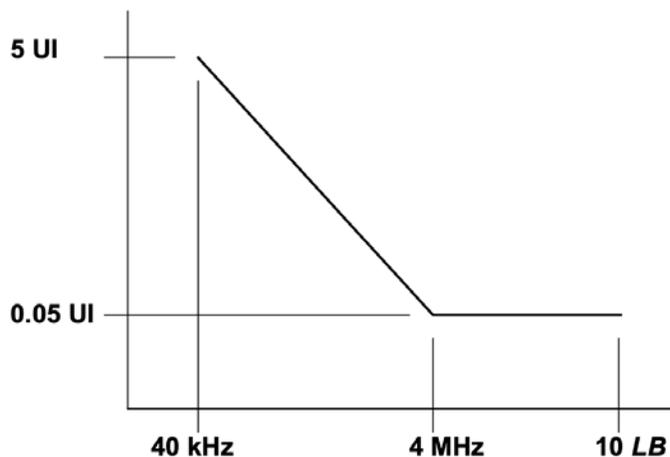
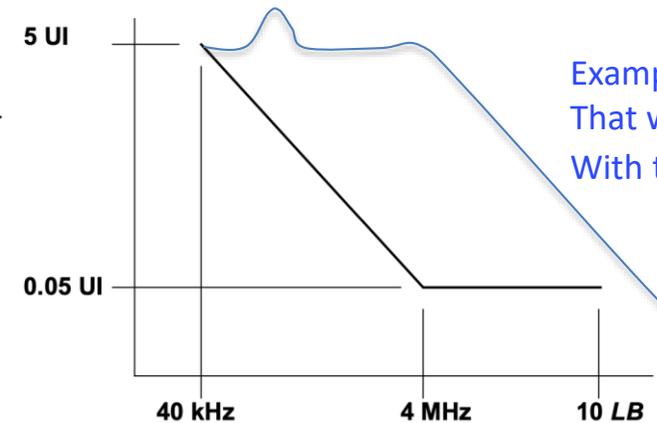


Figure 121-7—Illustration of the mask of the sinusoidal component of jitter tolerance

Table 162-17—Receiver jitter tolerance parameters

Parameter	Case A	Case B	Case C	Case D	Case E	Case F	Units
Jitter frequency	0.04	0.4	1.333	4	12	40	MHz
Jitter amplitude (pk-pk)	5	0.5	0.15	0.05	0.05	0.05	UI

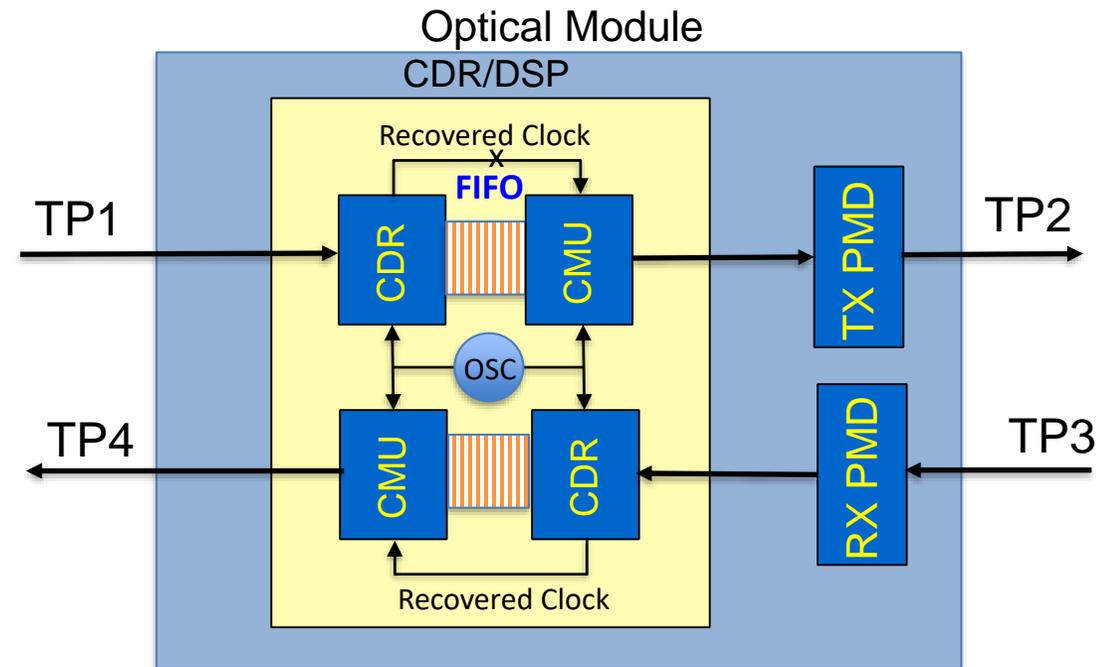
Applied sinusoidal jitter peak-to-peak amplitude (UI) (log scale)



Example of Bad CDR Design That won't be caught With the 6 test frequencies.

What May be the Real Problem

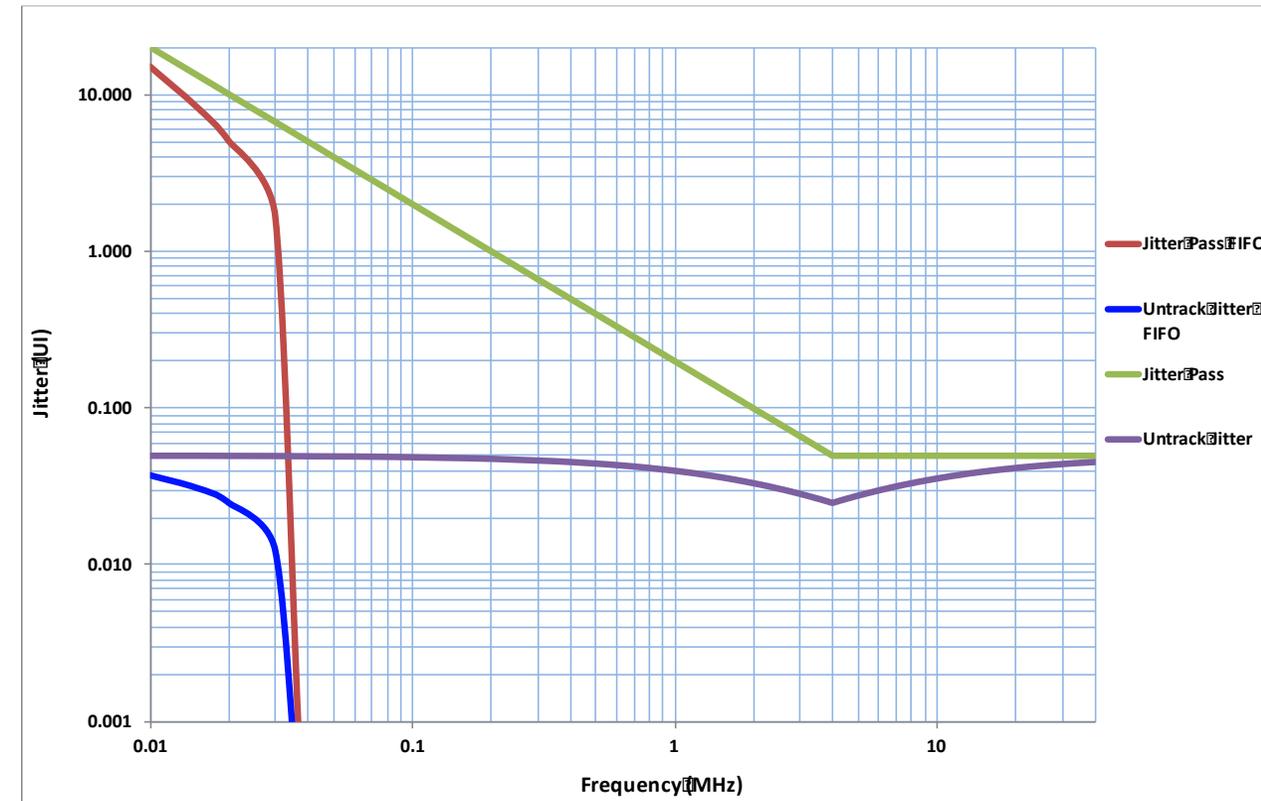
- ❑ **Current specifications are unclear how optical transmitters are tested for TDECQ when there is an optional AUI C2M present**
 - AUI C2M stress tested separately
 - SSPRQ is generated in the CMU mode without jitter and stress from AUI passing through the CDR
 - Applying stress input with SSPRQ at TP1a maybe too stressful for the CDR due to SSPRQ fast disparity changes
 - Instead PRBS31 would need to be applied at TP1a then the recovered clock must drive CMU generated SSPRQ pattern
 - Testing TDECQ with CMU generated pattern without any propagated jitter may have detrimental consequences for the system and likely the top reason for some of jitter anomaly reported [ran 3dj 02a 2407](#).



CMU Generated Patterns Misses Jitter Multiplication due to 2:1 Mux

□ Given that we didn't double the CDR BW with doubling Baudrate the CDR/DSP requires tricky FIFO to avoid excess jitter generated from 2:1 Mux

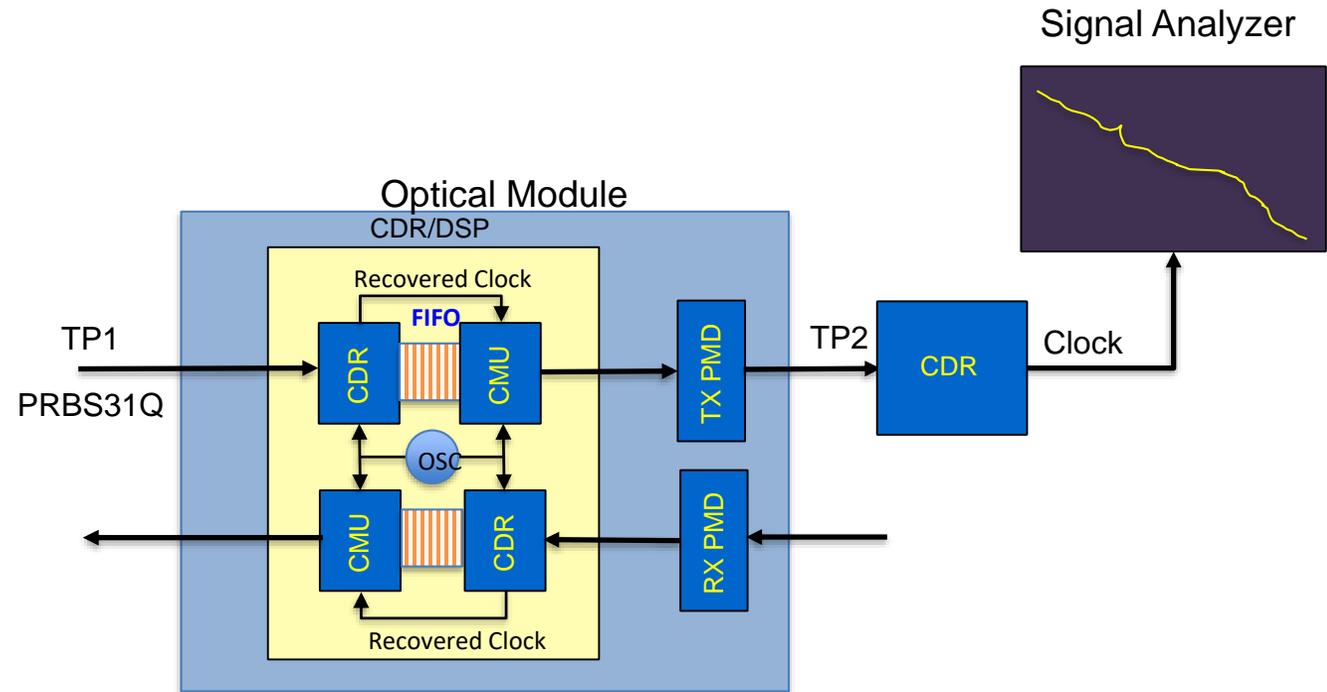
- Another tricky part of this FIFO is that the implementation must track without running out of FIFO and without using a very large FIFO but with right implementation practically there is no penalty, see [ghiasi 3dj 01a 2305](#)
 - A 2:1 mux chip with 5 UI (input serial bitrate) FIFO practically speaking has no penalty
 - A 2:1 Mux with no FIFO would have 0.05 UI of penalty
- For any type of transmitter/TDECQ unless the data is sourced through CDR/FIFO we maybe missing significant penalty!



Backup Up Approach to Capture TP2 Jitter

- In ideal world TP1 can be driven by stressed SSPRQ then the recovered data propagates to TP2 but SSPRQ containing transition density of PRBS31 that repeats in 2^{16} bits may break the CDR
 - Applying PRBS31Q to TP1 is a viable method then the recovered clock driver the CMU and SSPRQ
 - But this method will not exercise the mission mode FIFO, alternate method would need to be used to test the FIFO

- The backup approach to capture jitter and leverage SONET jitter generation method
 - With PRBS31Q or Ethernet traffic recover the clock with Golden CDR then integrate the phase noise
 - Jitter Gen ≤ 10 mUI measured from 40 kHz to 80 MHz.



Summary

- ❑ **Concern raised by [ran 3dj elec 01 240822](#) receivers having some jitter sensitivity is unlikely that even SONET jitter generation test can distinguish good vs bad transmitters**
 - Ran has stated that TDECQ doesn't capture jitter due to insufficient statistics, TDECQ with SSPRQ only require 3 seconds to provides statistically measurements
 - J3U/J4U measured on transitions of PRBS13 without exercising the CDR/FIFO would be an ineffective test that will increase TDECQ test time from few seconds to several minutes to as long as an hour
- ❑ **There have been reports of compliant TDECQ transmitters resulting in high FEC codeword errors**
 - Unless 1st hand data are shared difficult to pinpoint what is the exact issue
 - TDECQ is an effective test to capture jitter from the module if TP2 signal is based on recovered TP1 signal, but if SSPRQ gets generated in local CMU then critical jitters will not be captured by TDECQ
- ❑ **The real culprit here likely is that SSPRQ was generated in module CMU, therefore TDECQ is not capturing the mission mode jitter**
 - Only if stress input at TP1 propagates to TP2 or recovered clock drives the SSPRQ pattern then effect of jitter transfer, jitter peaking, and wander will be captured in TDECQ
 - Given SSPRQ maybe too stressful for the CDR then PRBS31Q has to be applied at TP1 then the recovered clock must source SSPRQ pattern
 - Some 20 years in XFP MSA we added 1 dB (max) jitter peaking for 10 GbE CDR/retimers, in case of 802.3dj excess jitter peaking with 5 CDR can be detrimental
 - An alternate approach for module that can't recover stressed input TP1 signal and use it to source SSPRQ would be to add SONET style output jitter specification
- ❑ **TDECQ can capture jitter but the shortcoming is that the module during TDECQ test is not in mission mode!**