



Reduction in Max Swing (Comments 523,524, 563, 570)

Bill Simms, Piers Dawe

NVIDIA

Supporters

- Vishnu Balan, NVIDIA
- Mike Dudek, Marvell
- Ali Ghiasi, Ghiasi Quantum

Reduction in Max Swing

Purpose

- Investigate the use of 1200mV differential peak-to-peak voltage (max) in the current specification
- Propose reduction of Differential peak to peak voltage (max) from 1200mV to 1000mV:
 - Represents current design practices in nm CMOS process technologies
 - Potential system power and noise savings
 - Reduction in XTALK terms leads to improved COM performance

1200mV swing referenced in the D1.1 spec

- Differential output voltage $v_{di} = S_{Li<p>} - S_{Li<n>}$
 - Source Lane positive and negative signals of transmitter's differential pair lane i (Fig83A-5)
 - Differential peak to peak is $V_{dpp} = V_{di}(1) - V_{di}(0)$ or $S_{Li<p1>} - S_{Li<n1>} - (S_{Li<p0>} - S_{Li<n0>})$
- Differential peak to peak voltage (max) is defined as 1200mV in
 - Table 176D-1 with reference to 93.8.1.3
 - Table 176E1 with reference to 176E.6.1
 - Table 176E-2 with reference to 176E.6.1
 - Table 178-6 with reference to 93.8.1.3
 - Table 179-7 with reference to 93.8.1.3
- Amplitude tolerance is 1200mV in:
 - Table 176E-3 reference 176E6.11
 - Table 176E-4 reference 176E.6.11
 - Table 179-10 subclass reference 179.9.5.2

Challenges of 1200mV support in current silicon

- Silicon process technologies have reduced voltage supplies over the last several node generations
 - Future technology nodes will likely continue this trend
- Many current RX designs cannot tolerate high TX Differential peak to peak voltage (max) and require use of swing control to request reduction
 - Overdriving the receiver front end can lead to linearity problems which impact accurate PAM4 recovery
- In short channel applications, RX will typically reduce Differential peak to peak voltage (max) to save power and reduce crosstalk
- Long channels are purported to need the margin provided by higher Differential peak to peak voltage (max) in high loss environment but even these would benefit from the XTALK relaxation

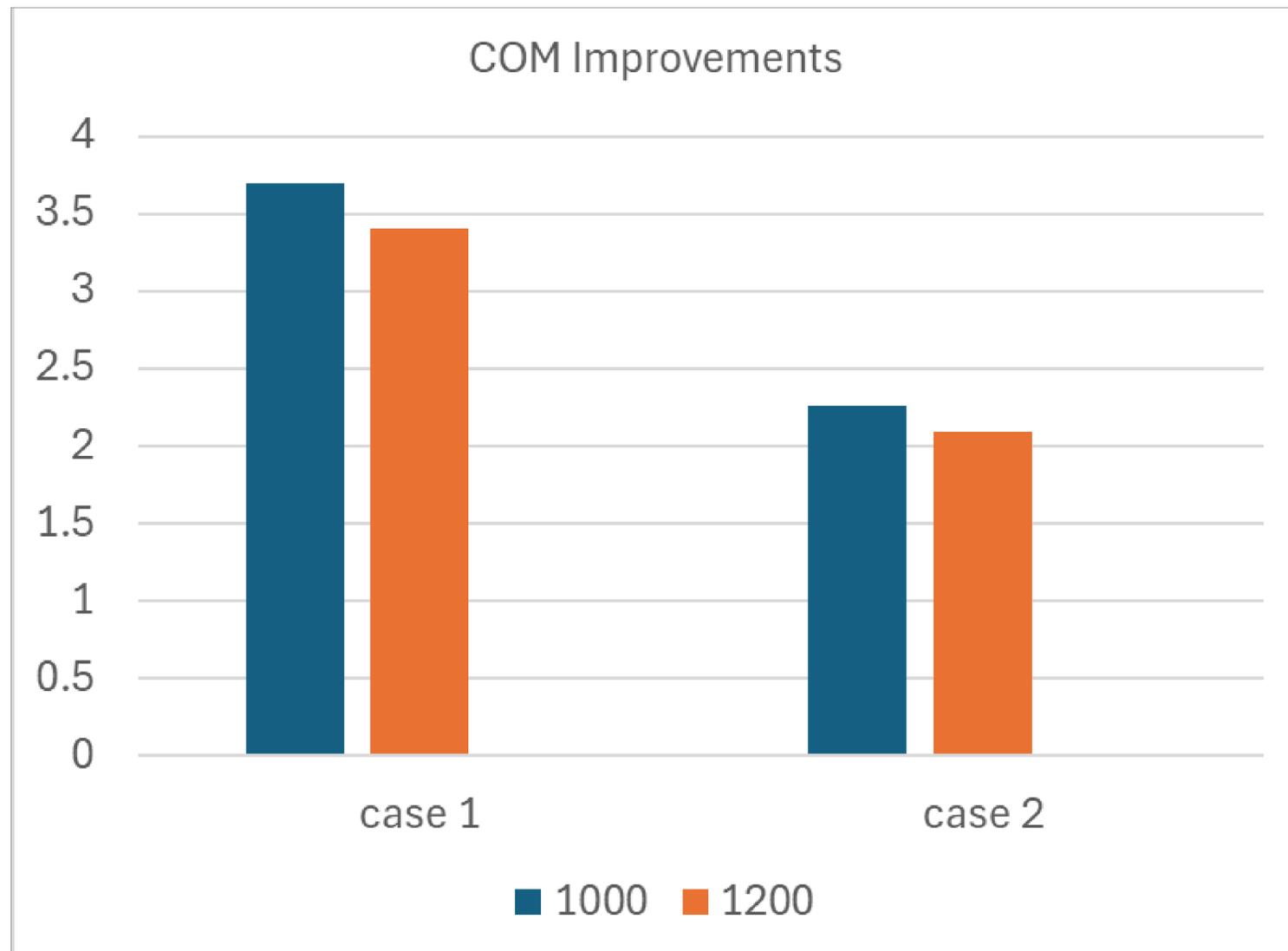
Proposed change 1200->1000mV

- Comments #523, 524, 563, and 570
- Updates to spec:
 - 1000mV replaces all 1200mV Differential peak to peak voltage (max) values in D1.1 spec
 - 20% tolerance 800-1200mV Differential peak to peak voltage (max) is reduced to roughly 10% (800-1000mV)
 - A_{ne} values used in COM scale down <some currently TBD in spec>
- Improvements to designs:
 - Lower complexity for low power supply designs by removing need for limiter or attenuator in front of RX
 - Lower power systems are enabled
- Aligns Ethernet with other SERDES standards like PCI Express
 - 5.0 spec all data rates 1200mV Differential peak to peak voltage (max) (2019)
 - 6.01 spec all data rates 1000mV Differential peak to peak voltage (max) (2022)
- Final values for CR and C2M for V-f, A_v, A_{fe}, and A_{ne} are not proposed by this presentation
 - Other COM values could improve with reduced Differential peak to peak voltage (max)

Comment Resolution Expressed Concern for CR/KR

- The reviewer commented that some designs have high loss which require more signal swing (Differential peak to peak voltage (max))
- However, increased Differential peak to peak voltage (max) also increases the impact of other signal impairments

COM Simulations for CR



0.3dB and 0.17 dB COM improvements

- Example Case showing impact of reducing the xtalk terms
- Simulations of marginal passing and marginal failing CR channels (Case 1 vs Case 2)
- Channels run with 1200 and then 1000mV swing
- Improvements noted in COM by reducing A_{ne} relative to other parameters
- Further investigation may show additional improvements of other COM parameters
- Final values of V_f , A_v , A_{fe} , and A_{ne} are not proposed by this presentation

Summary

- Reducing Differential peak-to-peak Voltage max from 1200mV to 1000mV
 - Enables lower power supply SERDES
 - Enables current and future silicon process nodes
 - Increases compatibility with other SERDES Specifications
 - Reduces complexity of receiver design
 - Reduces system power and noise



Thank You