

Host Channel/PCB Model Parameters for P802.3dj: Addressing Comment # 537

Mike Peng Li, Jenny Jiang, Masashi Shimanouchi, Hsinho Wu, Ilia Radashkevich, Itamar Levin, Ariel Cohen
Intel

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Background and Objectives

- Comment # 537 against 802.3dj D1.1 specification was made to address the Host channel /PCB model parameter TBDs

CI 179 SC 179.11.7.1 P 360 L 8 # 537

Li, Mike Intel

Comment Type TR Comment Status X

Table 179–17—PCB model parameter values TBDs

Suggested Remedy

Replace them with the filled table provided in the "PCB_models_parameters" sheet. A presentation "lim_3dj_01_2409" will be requested to explain how those values are derived.

Proposed Response Response Status O

Table 179–17—PCB model parameters and values

Parameter	Value	Units
γ_0	TBD 0	1/mm
a_1	TBD 5.95e-4	ns ^{1/2} /mm
a_2	TBD 2.6e-5	ns/mm
τ	TBD 5.79e-3	ns/mm
C_0	TBD 2.9e-5	nF
C_1	TBD 1.0e-5	nF
Z_c	TBD 92.5	Ω
R_0	50	Ω

 TBD filling

- This presentation provides the details on how host channel/PCB model parameters were derived

Introduction

- Host channel/PCB model and parameter definitions

178A.1.4.3 Host channel

Editor's Note (to be removed prior to final publication):

A host channel model has not yet been adopted. The model described in Clause 162 is used as a placeholder.

The host channel model is shown in Figure 178A-5 and is a function of the parameters summarized in Table 178A-5. It is the cascade connection of a first shunt capacitor C_0 , a transmission line, and a second shunt capacitor C_1 .

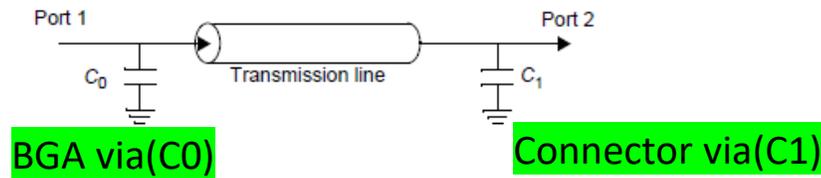
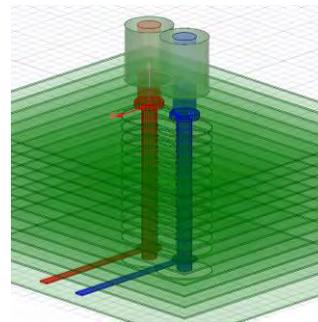


Figure 178A-5—Host channel model

Table 178A-5—Summary of host channel parameters

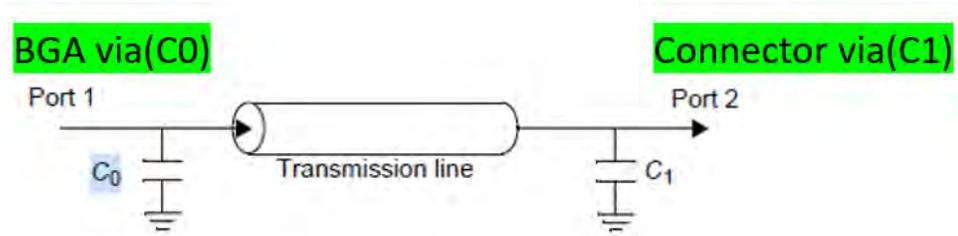
Parameter	Symbol	Units
Single-ended package capacitance at port 1 BGA via(C0)	C_0	nF
Host transmission line parameter, γ_0	$\gamma_0^{(h)}$	1/mm
Host transmission line parameter, a_1	$a_1^{(h)}$	ns ^{1/2} /mm
Host transmission line parameter, a_2	$a_2^{(h)}$	ns/mm
Host transmission line parameter, τ	$\tau^{(h)}$	ns/mm
Host transmission line differential characteristic impedance	$Z_c^{(h)}$	Ω
Host transmission line length	$z_p^{(h)}$	mm
Single-ended package capacitance at port 2 Connector via(C1)	C_1	nF



A PKG BGA via illustration (including stub)

A Host Channel Design Example

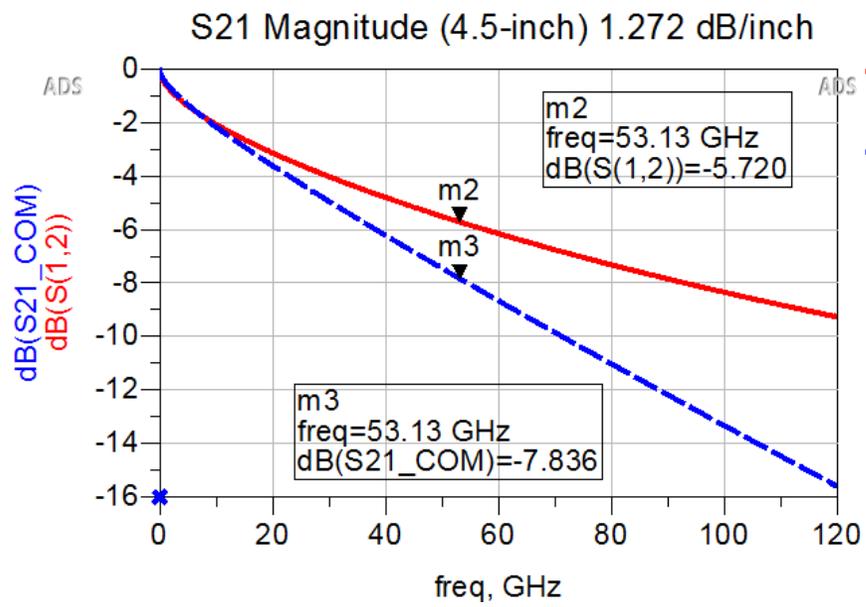
- Host BGA via->PCB-> Connector via



A 6.5dB Host Channel Design Example

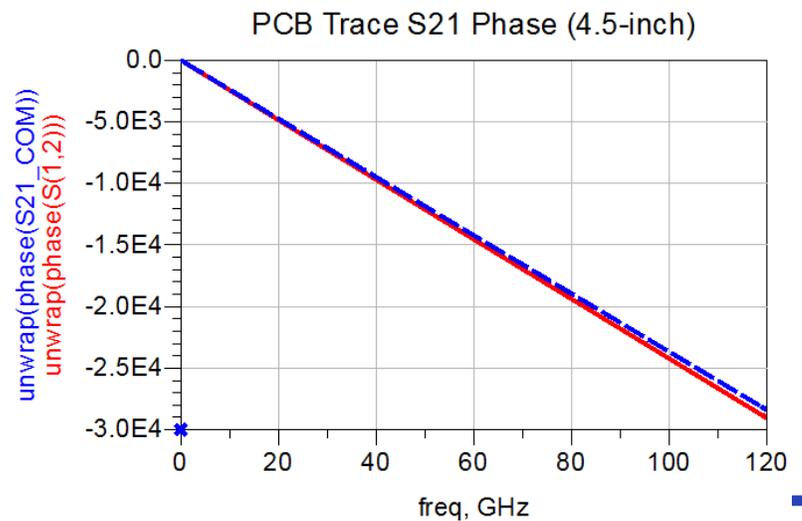
Component	Insertion Loss Port 1-Port 2 (dB) @ 53.125GHz
BGA via	0.6 dB
Host PCB Trace	1.272 dB/inch
Connector via	0.172 dB
Host Channel Length	4.5 inch
Total	6.5 dB

Start From 802.3ck 100G/L Host Channel Model Parameters: PCB Trace



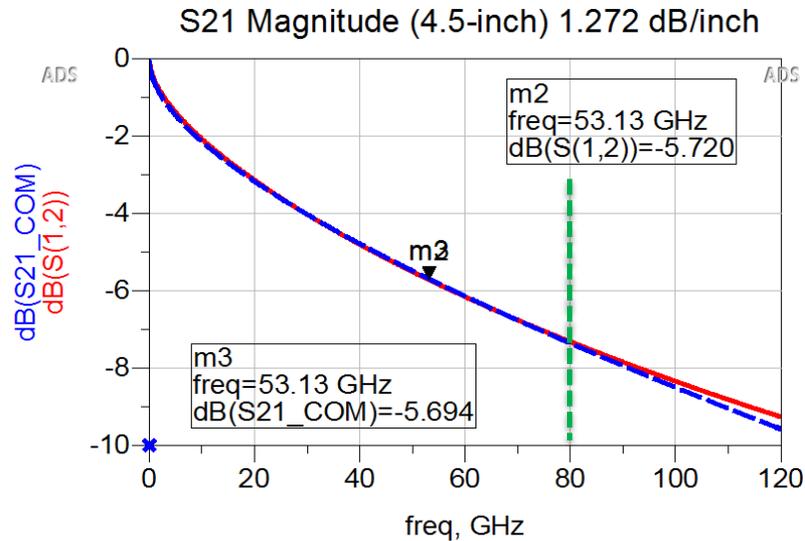
802.3ck Host Channel Model Parameters

Parameter	Value	Units
γ_0	0	1/mm
a_1	3.8206×10^{-4}	ns ^{1/2} /mm
a_2	9.5909×10^{-5}	ns/mm
τ	5.79×10^{-3}	ns/mm
C_0	2.9×10^{-5}	nF
C_1	1.9×10^{-5}	nF
Z_c	100	Ω
R_0	50	Ω

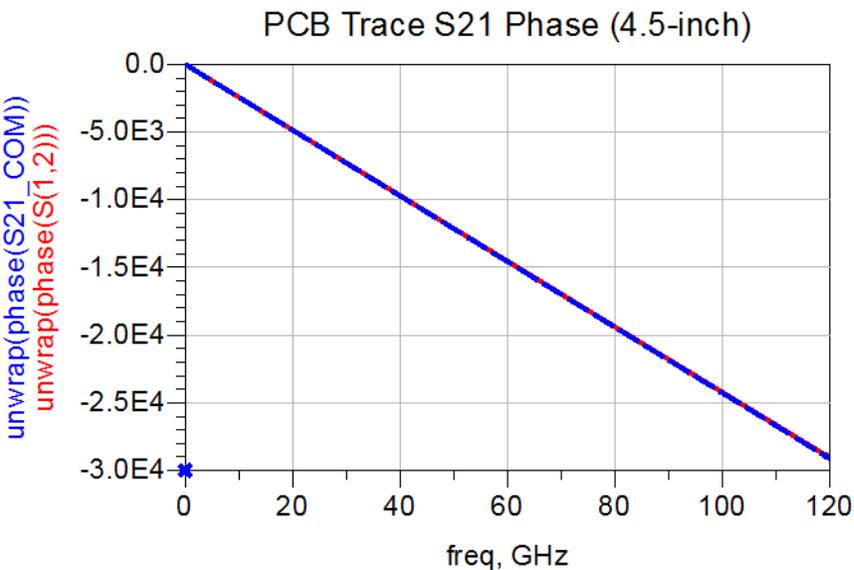


Adjust Host Channel Model Parameters to Match the 200G/L

Design (I): PCB Trace

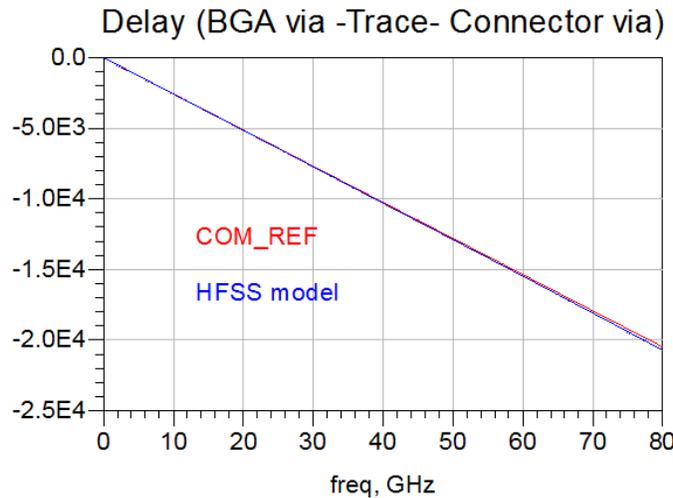
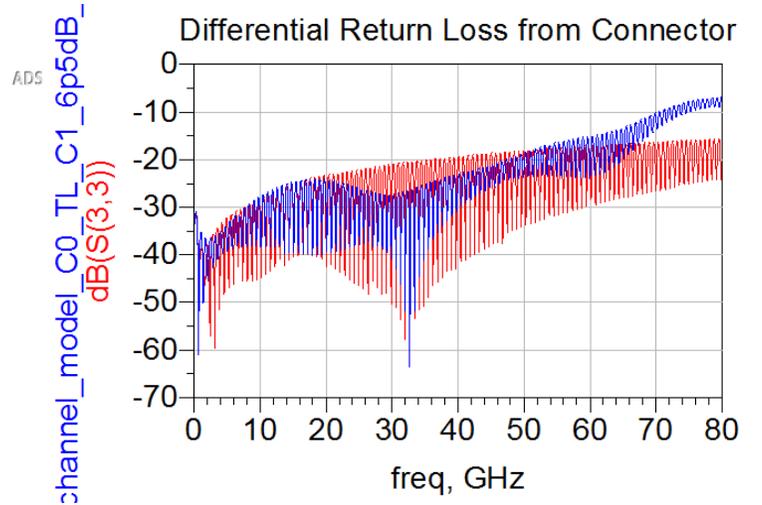
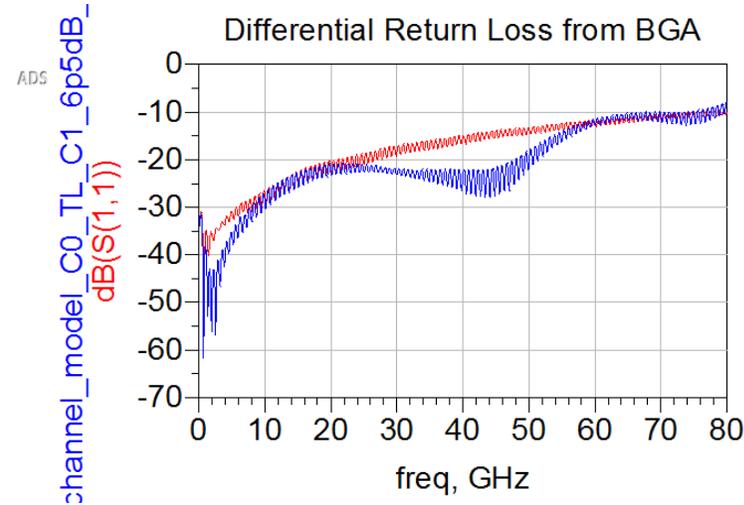
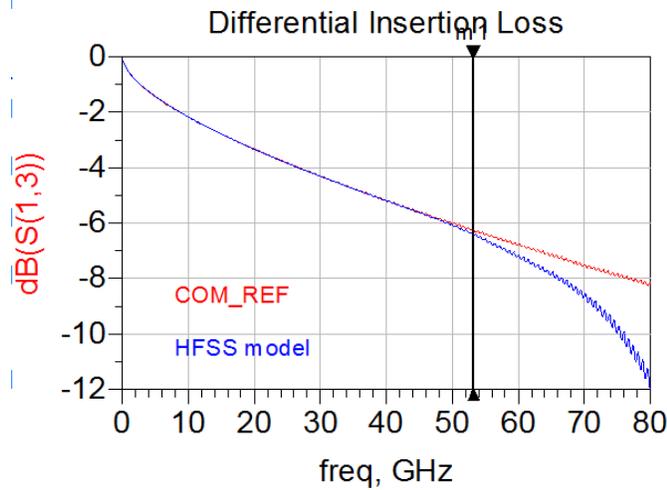


Parameter	Value	Units
γ_0	0	1/mm
a_1	5.95e-4 >	3.8206×10^{-4} ns ^{1/2} /mm
a_2	2.6e-5 <	9.5909×10^{-5} ns/mm
τ	5.79e-3 =	5.79×10^{-3} ns/mm
C_0		2.9×10^{-5} nF
C_1		1.9×10^{-5} nF
Z_c	92.5 <	100 Ω
R_0		50 Ω



Adjust Host Channel Model Parameters to Match the 200G/L

Design (II): BGA Via->PCB trace -> Connector Via



Parameter	Value	Units
γ_0	0	1/mm
a_1 5.95e-4	> 3.8206×10^{-4}	ns ^{1/2} /mm
a_2 2.6e-5	< 9.5909×10^{-5}	ns/mm
τ 5.79e-3	= 5.79×10^{-3}	ns/mm
C_0 2.9e-5	= 2.9×10^{-5}	nF
C_1 1.0e-5	< 1.9×10^{-5}	nF
Z_c 92.5	< 100	Ω
R_0	50	Ω

Proposed Host Channel/PCB Model Parameters

Table 179–17—PCB model parameters and values

Parameter	Value	Units
γ_0	TBD 0	1/mm
a_1	TBD 5.95e-4	ns ^{1/2} /mm
a_2	TBD 2.6e-5	ns/mm
τ	TBD 5.79e-3	ns/mm
C_0	TBD 2.9e-5	nF
C_1	TBD 1.0e-5	nF
Z_c	TBD 92.5	Ω
R_0	50	Ω



TBD filling

Thank You!