

Inner FEC sublayer updates and corrections for 800GBASE-LR1

(Support contribution for Comments #559 and #560)

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Agenda

- FEC Sublayer Delay (Comment #559)
- Correction to Pilot sequence table (Comment #560)

800GBASE-LR1 Inner FEC SublayerDelay

- The inner FEC sublayer delay is TBD in draft 1.1
 - As described in [gustlin 01 0216 logic](#) these delays are used as the worst case value in sizing buffers for pause operation and include 1TX + 1RX
- The delay includes two components
 - An inherent delay due to the buffering required by the various stages of the sublayers and therefore common to all implementations, and
 - An implementation delay which is vendor dependent
- Delays are quoted in “Bit time”, “Pause Quanta” and in absolute time (ns)

Inherent Delay of Inner FEC Sublayer

	Inner FEC Sublayer Blocks	Delay(ns)	Delay (Bit Time)	Pause Quanta	Notes
	Alignment	0.715	573	2	Align all 32 lanes to 20b RS symbol boundaries
	Permutation	0.000	0	0	No bit reordering relative to PCS
	Convolution Interleaver	54.212	43370	85	Max delay of 40*18*2b on each of 32 lanes
	BCH Encoder	0.518	415	1	Max delay of 16b on each of 32 lanes
	Circular Shift	3.235	2589	6	Max delay of 100b times on each of 32 lanes
	BCH Interleaver	3.571	2857	6	Max delay of 883b at output of 32 to 4 serializer
	Pilot Symbol Insertion	0.008	7	1	1 symbol delay
	Total	62.259	49808	98	

Implementation Delays

- Implementations are feasible with delays $< 50\text{ns}$
- Propose implementation delays not to exceed $\sim 102\text{ns}$ to accommodate all possible designs
 - Number chosen to limit delay to 256 Pause-Quanta

Comment #559: Proposed text for 184.7

184.7 Delay constraints

The maximum delay contributed by the Inner FEC (sum of transmit and receive delays at one end of the link) shall be no more than **131072** BT (**256** pause_quanta or **163.84** ns). A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 116.4 and its references.

Correction to Pilot Table (Table 184-2)

- Proposed resolution for Comment #560
- Pilot sequence in Table 184-2 is inconsistent with the intended sequence shown in Table 184-4 as 4-level signals
- Correction is highlighted in the table shown on this slide: Index 27, Output 2 should be “00” to be consistent with “-3” in Table 184-4.

	Output					Output					Output					Output				
	Index	0	1	2	3	Index	0	1	2	3	Index	0	1	2	3	Index	0	1	2	3
	0	10	00	10	00	24	00	10	00	00	48	10	10	00	10	72	00	00	00	10
	1	10	00	10	10	25	00	00	00	10	49	00	00	10	00	73	10	10	00	10
	2	10	10	10	10	26	10	10	10	00	50	10	00	10	10	74	00	10	00	00
	3	10	00	00	00	27	10	10	00	00	51	00	00	10	10	75	10	00	10	00
	4	10	00	00	10	28	10	10	10	00	52	10	10	00	00	76	00	10	00	00
	5	00	00	00	10	29	00	00	00	00	53	00	00	10	00	77	10	10	00	10
	6	10	10	00	00	30	00	10	00	00	54	10	00	10	00	78	00	10	00	00
	7	00	10	00	10	31	10	00	00	00	55	10	10	00	00	79	00	10	00	00
	8	00	10	00	00	32	10	10	00	10	56	00	00	00	10	80	00	10	10	10
	9	00	10	10	00	33	00	10	10	10	57	00	00	10	00	81	10	10	10	10
	10	00	00	00	00	34	00	00	10	00	58	10	00	00	00	82	10	00	10	10
	11	00	10	10	00	35	00	00	00	00	59	00	10	00	10	83	10	10	10	10
	12	10	10	10	10	36	10	00	00	10	60	10	00	10	10	84	00	10	10	00
	13	00	10	00	00	37	10	10	00	10	61	00	10	00	00	85	10	00	10	00
	14	00	00	10	10	38	10	00	00	00	62	10	10	00	00	86	00	00	10	10
	15	10	00	00	10	39	10	10	10	00	63	10	00	10	10	87	00	00	10	10
	16	00	10	00	10	40	10	10	10	10	64	10	00	00	10	88	10	10	10	00
	17	10	00	10	00	41	00	10	10	00	65	00	10	10	10	89	00	10	00	10
	18	10	00	10	10	42	00	10	00	00	66	10	10	00	10	90	00	00	10	10
	19	00	00	00	10	43	00	00	00	00	67	00	00	10	00	91	10	00	00	00
	20	10	00	10	10	44	00	00	00	10	68	00	10	00	10	92	10	00	10	00
	21	10	00	10	10	45	00	00	00	10	69	00	00	00	00	93	00	10	10	10
	22	10	10	10	00	46	10	10	10	00	70	10	10	10	00	94	10	00	10	10
	23	00	10	10	10	47	00	00	10	00	71	10	10	00	10	95	00	00	10	10

Thank you!