

802.3dj D1.1

Comment Resolution

Logic Topics

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Introduction

- This slide package was assembled by the 802.3dj editorial team to provide background and detailed resolutions to aid in comment resolution.
- Specifically, these slides are for the logic track comments

<Time Sync>

(Comments: 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294)

Time Sync - Introduction

- The following slides capture proposed updates to many clauses throughout the draft to better reference the optional support for time synchronization protocols “Clause 90: Ethernet support for time synchronization protocols”
- This presentation is in support of the following comments:

268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294

Time Sync - Overview of proposed changes

The changes fall into the several categories:

Within the Rate introductory clauses:

1. Add a new sub-clause that explains TimeSync support
2. Add Clause 90 to the PHY type and clause correlation tables

Within PCS/PMA/InnerFEC clauses:

3. Add instructions on how to calculate the path data delay and mention the related status variables
4. Add the status variables to the MDIO mapping table

Within the PMD clauses:

5. Add Clause 90 to the Physical Layer clauses tables

Time Sync - Clause 116

Change Table 116-3 to add a column for Clause 90 as follows (blue font indicates added text):

Table 116–3—PHY type and clause correlation (200GBASE copper with 2 or 4 lanes)

PHY type	Clause ^a																
	73	78	90	117	118	119	120	120B	120D	120F	136	137	162	163	176	176D	
	Auto-Negotiation	EEE	Time Synchronization	RS	200GMII	200GMII Extender	200GBASE-R PCS	200GBASE-R BM -PMA	200GAUI-8 C2C	200GAUI-4 C2C	200GAUI-2 C2C	200GBASE-CR4 PMD	200GBASE-KR4 PMD	200GBASE-CR2 PMD	200GBASE-KR2 PMD	200GBASE-R SMI -PMA	200GAUI-1 C2C
200GBASE-KR2	M		O	M	O	O	M	M	O	O	O				M	C	O
200GBASE-KR4	M	O	O	M	O	O	M	M	O	O			M			C	O
200GBASE-CR2	M		O	M	O	O	M	M	O	O	O			M		C	O
200GBASE-CR4	M	O	O	M	O	O	M	M	O	O		M				C	O

^a O = Optional, M = Mandatory, C = Conditional (refer to PMD clause for details).

Make similar changes to Table 116-3aa, Table 116-3a, Table 116-3b, Table 116-4, Table 116-4a, Table 116-5 and Table 116-5a.

Time Sync - Clause 116

Insert new subclause 116.2.9 after 116.2.8 as follows (blue font indicates added text):

116.2.9 Time Synchronization

A 200 Gb/s or 400 Gb/s Physical Layer may optionally support time synchronization protocols that require knowledge of packet egress and ingress time. Ethernet support for time synchronization protocols is defined in Clause 90.

If time synchronization is supported:

- the 200Gb/s and 400Gb/s Reconciliation Sublayer (RS) provides a Time Synchronization Service Interface (TSSI) that connects to a TimeSync client (see 90.4).
- the path data delay values of each PHY sublayer are reported as status variables and mapped to MDIO status registers (see 90.6).

Note: In 802.3df D1.1, “116.2.9 Inter-sublayer link training (ILT)” should be “116.2.8 Inter-sublayer link training (ILT)”, according to the associated editing instruction.

Time Sync - Clause 169

Change Table 169-2 to add a column for Clause 90 as follows (blue font indicates added text):

Table 169-2—PHY type and clause correlation (800GBASE copper)

PHY type	Clause ^a													
	73	90	170		171	171	173	120F	162	163	176	176D	178	179
	Auto-Negotiation	Time Synchronization	RS	800GMII	800GMII Extender	800GBASE-R PCS	800GBASE-R BM-PMA	800GAUI-8 C2C	800GBASE-CR8 PMD	800GBASE-KR8 PMD	800GBASE-R SM-PMA	800GAUI-4 C2C	800GBASE-KR4 PMD	800GBASE-CR4 PMD
800GBASE-KR4	M	O	M	O	O	M	C	O	=	=	M	O	M	=
800GBASE-KR8	M	O	M	O	O	M	M	O	=	M	C	O	=	=
800GBASE-CR4	M	O	M	O	O	M	C	O	=	=	M	O	=	M
800GBASE-CR8	M	O	M	O	O	M	M	O	M	=	C	O	=	=

^a O = Optional, M = Mandatory, C = Conditional (refer to PMD clause for details).

Make similar changes to Table 169-3 and Table 169-3a.

Time Sync - Clause 169

Insert new subclause 169.2.10 after 169.2.9 as follows (blue font indicates added text):

169.2.10 Time Synchronization

A 800 Gb/s Physical Layer may optionally support time synchronization protocols that require knowledge of packet egress and ingress time. Ethernet support for time synchronization protocols is defined in Clause 90.

If time synchronization is supported:

- the 800Gb/s Reconciliation Sublayer (RS) provides a Time Synchronization Service Interface (TSSI) that connects to a TimeSync client (see 90.4).
- the path data delay values of each PHY sublayer are reported as status variables and mapped to MDIO status registers (see 90.6).

Time Sync - Clause 174

Change Table 174-2 to add a column for Clause 90 as follows (blue font indicates added text):

Table 174-2—PHY type and clause correlation (1.6TBASE-R optical)

PHY type	Clause ^a												
	90	170		171	175	176	177	120F	120G	176D	176E	180	182
	Time Synchronization	RS	1.6TMMH	1.6TMMH Extender	1.6TBASE-R PCS	1.6TBASE-R SM-PMA	1.6TBASE-R Inner FEC	1.6TAUI-16 C2C	1.6TAUI-16 C2M	1.6TAUI-8 C2C	1.6TAUI-8 C2M	1.6TBASE-DR8 PMD	1.6TBASE-DR8-2 PMD
1.6TBASE-DR8	O	M	O	O	M	M	—	O	O	O	O	M	—
1.6TBASE-DR8-2	O	M	O	O	M	M	M	O	O	O	O	—	M

^a O = Optional, M = Mandatory.

Make similar changes to Table 174-3

Time Sync - Clause 174

Insert new subclause 174.2.12 after 174.2.11, and renumber all the subsequent subclauses, as follows (blue font indicates added text):

174.2.12 Time Synchronization

A 1.6 Tb/s Physical Layer may optionally support time synchronization protocols that require knowledge of packet egress and ingress time. Ethernet support for time synchronization protocols is defined in Clause 90.

If time synchronization is supported:

- the 1.6 Tb/s Reconciliation Sublayer (RS) provides a Time Synchronization Service Interface (TSSI) that connects to a TimeSync client (see 90.4).
- the path data delay values of each PHY sublayer are reported as status variables and mapped to MDIO status registers (see 90.6).

174.2.13 FEC Degrade

The FEC degrade feature provides the ability to detect and indicate a degrade condition at the RS-FEC decoder using FEC degrade detection, and to propagate the FEC degrade indication using FEC degrade signaling. The propagation of FEC degrade indications across PCS and XS is described in 116.6.

FEC degrade detection and signaling specifications for the 1.6TXS and 1.6TBASE-R PCS are summarized in 171.6 and 175.3, respectively.

Time Sync - Clause 175

Insert new subclause 175.6 after 175.5, and renumber all the subsequent subclauses, as follows (blue font indicates added text):

175.6 Path data delay for time synchronization

When the 1.6TBASE-R PCS is part of a Physical Layer that supports Time Synchronization, transmit and receive path data delays (see 90.7) are reported as if the DDMP (data delay measurement point) is at the start of the set of four interleaved FEC codewords.

Four separate data delay values are reported, each with nanosecond and (if supported) sub-nanosecond portions, in the following eight status variables:

- PCS_delay_ns_TX_max, PCS_delay_subns_TX_max
- PCS_delay_ns_TX_min, PCS_delay_subns_TX_min
- PCS_delay_ns_RX_max, PCS_delay_subns_RX_max
- PCS_delay_ns_RX_min, PCS_delay_subns_RX_min

Time Sync - Clause 175

Change Table 175-4 as follows (most unchanged rows not shown and blue font indicates added text):

Table 175-4—PCS status variables and MDIO mapping

Status variable	Variable reference	MDIO register/bit number	MDIO register/bit reference
...			
FEC_uncorrected_cw_counter	175.2.5.3	3.804, 3.805	45.2.3.63
PCS_delay_ns_TX_max	175.6	3.1801, 3.1802	45.2.3.68
PCS_delay_subns_TX_max	175.6	3.1809	45.2.3.68
PCS_delay_ns_TX_min	175.6	3.1803, 3.1804	45.2.3.68
PCS_delay_subns_TX_min	175.6	3.1810	45.2.3.68
PCS_delay_ns_RX_max	175.6	3.1805, 3.1806	45.2.3.69
PCS_delay_subns_RX_max	175.6	3.1811	45.2.3.69
PCS_delay_ns_RX_min	175.6	3.1807, 3.1808	45.2.3.69
PCS_delay_subns_RX_min	175.6	3.1812	45.2.3.69

Time Sync - Clause 176

Insert new subclause 176.10 after 176.9, and renumber all the subsequent subclauses, as follows (blue font indicates added text):

176.10 Path data delay for time synchronization

When the SM-PMA is part of a Physical Layer that supports Time Synchronization (see Clause 90), transmit and receive path data delays (see 90.7) are reported as if the DDMP (data delay measurement point) occurs on an odd PCS lane.

Four separate data delay values are reported, each with nanosecond and (if supported) sub-nanosecond portions, in the following eight status variables:

- PMA_delay_ns_TX_max, PMA_delay_subns_TX_max
- PMA_delay_ns_TX_min, PMA_delay_subns_TX_min
- PMA_delay_ns_RX_max, PMA_delay_subns_RX_max
- PMA_delay_ns_RX_min, PMA_delay_subns_RX_min

176.10.11 Management variables

PMA control and status variables intended to be accessible via a management system are listed in Table 176–6 and Table 176–7.

Time Sync - Clause 176

Change Table 176-7 as follows (most unchanged rows not shown and blue font indicates added text):

Table 176–7—PMA status variables and MDIO mapping

Status variable	Variable reference	MDIO register/bit number	MDIO register/bit reference
...			
symbol_pair_lock_demux<7:0>		TBD	
pcs_lane_mapping_demux<0:31>		TBD	
PMA_delay_ns_TX_max	176.10	1.1801, 1.1802	45.2.1.176
PMA_delay_subns_TX_max	176.10	1.1809	45.2.1.176
PMA_delay_ns_TX_min	176.10	1.1803, 1.1804	45.2.1.176
PMA_delay_subns_TX_min	176.10	1.1810	45.2.1.176
PMA_delay_ns_RX_max	176.10	1.1805, 1.1806	45.2.1.177
PMA_delay_subns_RX_max	176.10	1.1811	45.2.1.177
PMA_delay_ns_RX_min	176.10	1.1807, 1.1808	45.2.1.177
PMA_delay_subns_RX_min	176.10	1.1812	45.2.1.177

Time Sync - Clause 177

Insert new subclause 177.10 after 177.9, and renumber all the subsequent subclauses, as follows (blue font indicates added text):

177.10 Path data delay for time synchronization

When the InnerFEC is part of a Physical Layer that supports Time Synchronization transmit and receive path data delays (see 90.7) are reported as if the DDMP (data delay measurement point) occurs on the first symbol on FEC flow 0 after the 1024-bit pad insertion. This symbol corresponds to the largest delay for transmit and the shortest delay for receive.

Four separate data delay values are reported, each with nanosecond and (if supported) sub-nanosecond portions, in the following eight status variables:

- Inner_FEC_delay_ns_TX_max, Inner_FEC_delay_subns_TX_max
- Inner_FEC_delay_ns_TX_min, Inner_FEC_delay_subns_TX_min
- Inner_FEC_delay_ns_RX_max, Inner_FEC_delay_subns_RX_max
- Inner_FEC_delay_ns_RX_min, Inner_FEC_delay_subns_RX_min

177.11 Management variables

PMA control and status variables intended to be accessible via a management system are listed in Table 176–6 and Table 176–7.

Time Sync - Clause 177

Change Table 177-5 as follows (most unchanged rows not shown and blue font indicates added text):

Table 177-5—Inner FEC status variables and MDIO mapping

Status variable	Variable reference	MDIO register/bit number	MDIO register/bit reference
...			
Inner_FEC_codeword_error_bin_i (Inner FEC lane 7)	177.5.4.1.5	1.2140, 1.2141, 1.2142, 1.2143, 1.2144, 1.2145	45.2.1.213g
Inner_FEC_delay_ns_TX_max	177.10	1.1813, 1.1814	45.2.1.177a
Inner_FEC_delay_subns_TX_max	177.10	1.1817	45.2.1.177a
Inner_FEC_delay_ns_TX_min	177.10	1.1815, 1.1816	45.2.1.177a
Inner_FEC_delay_subns_TX_min	177.10	1.1818	45.2.1.177a
Inner_FEC_delay_ns_RX_max	177.10	1.1819, 1.1820	45.2.1.177b
Inner_FEC_delay_subns_RX_max	177.10	1.1823	45.2.1.177b
Inner_FEC_delay_ns_RX_min	177.10	1.1821, 1.1822	45.2.1.177b
Inner_FEC_delay_subns_RX_min	177.10	1.1824	45.2.1.177b

Time Sync - Clause 184

Insert new subclause 184.8 after 184.7, and renumber all the subsequent subclauses, as follows (blue font indicates added text):

184.8 Path data delay for time synchronization

When the InnerFEC is part of a Physical Layer that supports Time Synchronization transmit and receive path data delays (see 90.7) are reported as if the DDMP (data delay measurement point) occurs on **<TBD>**, corresponding to the largest delay for transmit and the shortest delay for receive.

Four separate data delay values are reported, each with nanosecond and (if supported) sub-nanosecond portions, in the following eight status variables:

- Inner_FEC_delay_ns_TX_max, Inner_FEC_delay_subns_TX_max
- Inner_FEC_delay_ns_TX_min, Inner_FEC_delay_subns_TX_min
- Inner_FEC_delay_ns_RX_max, Inner_FEC_delay_subns_RX_max
- Inner_FEC_delay_ns_RX_min, Inner_FEC_delay_subns_RX_min

184.89 Management variables

PMA control and status variables intended to be accessible via a management system are listed in Table 176–6 and Table 176–7.

Time Sync - Clause 184

Change Table 184-7 as follows (most unchanged rows not shown and blue font indicates added text):

Table 184–7—Inner FEC status variables and MDIO mapping

Status variable	Variable reference	MDIO register/bit number	MDIO register/bit reference
...			
FEC_total_bits_counter	184.5.7.3	1.2280, 1.2281, 1.2282, 1.2283	45.2.1.229
FEC_corrected_bits_counter	184.5.7.4	1.2284, 1.2285, 1.2286, 1.2287	45.2.1.230
Inner_FEC_delay_ns_TX_max	184.8	1.1813, 1.1814	45.2.1.177a
Inner_FEC_delay_subns_TX_max	184.8	1.1817	45.2.1.177a
Inner_FEC_delay_ns_TX_min	184.8	1.1815, 1.1816	45.2.1.177a
Inner_FEC_delay_subns_TX_min	184.8	1.1818	45.2.1.177a
Inner_FEC_delay_ns_RX_max	184.8	1.1819, 1.1820	45.2.1.177b
Inner_FEC_delay_subns_RX_max	184.8	1.1823	45.2.1.177b
Inner_FEC_delay_ns_RX_min	184.8	1.1821, 1.1822	45.2.1.177b
Inner_FEC_delay_subns_RX_min	184.8	1.1824	45.2.1.177b

Time Sync - Clause 186

Insert new subclause 186.6 after 186.5, and renumber all the subsequent subclauses, as follows (blue font indicates added text):

186.6 Path data delay for time synchronization

186.6.1 PCS path data delay for time synchronization

When the PCS is part of a Physical Layer that supports Time Synchronization transmit and receive path data delays (see 90.7) are reported as if the DDMP (data delay measurement point) occurs on:

- the start of the first non-fixed-stuff 257-bit GMP word of the tributary 0 multiframe (word 1 is always fixed stuff, so this is word 2)
- where the start of the PCS frame is also the start of an FEC frame (the start of the PCS frame and the start of the FEC frame are guaranteed to coincide every 128 FEC frames = 29 PCS frames)
- taking into account the maximum (transmit) and minimum (receive) data delay through the stuff-words mechanism

This corresponds to the absolute longest delay on transmit, and the absolute shortest delay on receive.

Four separate data delay values are reported, each with nanosecond and (if supported) sub-nanosecond portions, in the following eight status variables:

- PCS_delay_ns_TX_max, PCS_delay_subns_TX_max
- PCS_delay_ns_TX_min, PCS_delay_subns_TX_min
- PCS_delay_ns_RX_max, PCS_delay_subns_RX_max
- PCS_delay_ns_RX_min, PCS_delay_subns_RX_min

Time Sync - Clause 186

186.6.2 PMA path data delay for time synchronization

When the PMA is part of a Physical Layer that supports Time Synchronization transmit and receive path data delays (see 90.7) are reported as if the DDMP (data delay measurement point) occurs on the first data symbol of the PMA frame S<0>, corresponding to the maximum delay for transmit and minimum delay for receive.

Four separate data delay values are reported, each with nanosecond and (if supported) sub-nanosecond portions, in the following eight status variables:

- PMA_delay_ns_TX_max, PMA_delay_subns_TX_max
- PMA_delay_ns_TX_min, PMA_delay_subns_TX_min
- PMA_delay_ns_RX_max, PMA_delay_subns_RX_max
- PMA_delay_ns_RX_min, PMA_delay_subns_RX_min

Time Sync - Clause 186

Change Table 186-9 as follows (unchanged rows not shown and blue font indicates added text):

Table 186-9—PCS status variables and MDIO mapping

Status variable	Variable reference	MDIO register/bit number	MDIO register/bit reference
...			
PCS_delay_ns_TX_max	186.6.1	3.1801, 3.1802	45.2.3.68
PCS_delay_subns_TX_max	186.6.1	3.1809	45.2.3.68
PCS_delay_ns_TX_min	186.6.1	3.1803, 3.1804	45.2.3.68
PCS_delay_subns_TX_min	186.6.1	3.1810	45.2.3.68
PCS_delay_ns_RX_max	186.6.1	3.1805, 3.1806	45.2.3.69
PCS_delay_subns_RX_max	186.6.1	3.1811	45.2.3.69
PCS_delay_ns_RX_min	186.6.1	3.1807, 3.1808	45.2.3.69
PCS_delay_subns_RX_min	186.6.1	3.1812	45.2.3.69

Time Sync - Clause 186

Insert Table 186-10 after Table 186-9 as follows (contents to be filled in later):

Table 186–10—PMA control variables and MDIO mapping

Control variable	Variable reference	MDIO register/bit number	MDIO register/bit reference
...			

Insert Table 186-11 after Table 186-10 as follows (blue font indicates added text):

Table 186–11—PMA status variables and MDIO mapping

Status variable	Variable reference	MDIO register/bit number	MDIO register/bit reference
...			
PMA_delay_ns_TX_max	186.6.2	1.1801, 1.1802	45.2.1.176
PMA_delay_subns_TX_max	186.6.2	1.1809	45.2.1.176
PMA_delay_ns_TX_min	186.6.2	1.1803, 1.1804	45.2.1.176
PMA_delay_subns_TX_min	186.6.2	1.1810	45.2.1.176
PMA_delay_ns_RX_max	186.6.2	1.1805, 1.1806	45.2.1.177
PMA_delay_subns_RX_max	186.6.2	1.1811	45.2.1.177
PCS_delay_ns_RX_min	186.6.2	1.1807, 1.1808	45.2.1.177
PCS_delay_subns_RX_min	186.6.2	1.1812	45.2.1.177

Time Sync - Clause 178, 179, 180, 181, 182, 183, 185, 187

Change Table 178-1 to add a row for Clause 90 as follows (most unused rows not shown, blue font indicates added text):

Table 178-1—Physical Layer clauses associated with the 200GBASE-KR1 PMD

Associated clause	200GBASE-KR1
90—Time Synchronization	Optional
117—200 Gb/s RS	Required
117—200GMII ^a	Optional
...	

Make similar changes to:

- Table 178-2, Table 178-3, Table 178-4
- Table 179-1, Table 179-2, Table 179-3, Table 179-4
- Table 180-1, Table 180-2, Table 180-3, Table 180-4
- Table 181-1
- Table 182-1, Table 182-2, Table 182-3, Table 182-4
- Table 183-1
- Table 185-1
- Table 187-1

<PMA Service Interface>

Clause 176

Comments: 13, 17, 228, 229, 235, 236, 237, 238, 585

PMA Service Interface subclauses

176.2 PMA service interface

General PMA Interface definition

This PMA service interface is an instance of the inter-sublayer service interface defined in 116.3.1 (for 200GBASE-R or 400GBASE-R), 169.3.1 (for 800GBASE-R), or 174.3.1 (for 1.6TBASE-R).

The PMA service interface primitives (when applicable) are summarized as follows:

```
PMA:IS_UNITDATA_i.request(tx_symbol)
PMA:IS_SIGNAL.request(SIGNAL_OK)
PMA:IS_UNITDATA_i.indication(rx_symbol)
PMA:IS_SIGNAL.indication(SIGNAL_OK)
```

In the transmit direction, the PMA receives x parallel symbol streams from the client sublayer as PMA:IS_UNITDATA_0:($x-1$).request. In the receive direction, the PMA sends x parallel symbol streams to the client sublayer as PMA:IS_UNITDATA_0:($x-1$).indication.

When the client sublayer is an xBASE-R PCS, DTE xXS or a BM-PMA, each instance of tx_symbol and rx_symbol takes on one of two values: 0 or 1.

When the client sublayer is an xAUI-n, each instance of tx_symbol and rx_symbol takes on one of four values: 0, 1, 2, or 3 using PAM4 signaling.

The PMA receives signal status information from the sublayer above the PMA using the PMA:IS_SIGNAL.request primitive.

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Draft Amendment to IEEE Std 802.3-2022
IEEE P802.3dj 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force

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The PMA provides signal status information to the client sublayer using the PMA:IS_SIGNAL.indication primitive. The parameter SIGNAL_OK is set as defined for each PMA type.

176.4.2 PMA interfaces

m:n PMA Interface specifics

176.4.2.1 PMA service interface

The PMA service interface semantics are defined in 176.2 for $x = m$ input and output streams.

For the 200GBASE-R 8:1, 400GBASE-R 16:2 and 800GBASE-R 32:4 PMAs, the nominal interface data rate per stream is 26.5625 Gb/s.

For the 1.6TBASE-R 16:8 PMA, the nominal interface data rate per stream is 106.25 Gb/s.

176.5.2 PMA interfaces

n:m PMA Interface specifics

176.5.2.1 PMA service interface

The PMA service interface semantics are defined in 176.2 for $x = n$ input and output streams.

The nominal interface data rate per stream is 212.5 Gb/s.

176.6.2.1 PMA service interface

n:n PMA Interface specifics

The PMA service interface semantics are defined in 176.2 for $x = n$ input and output streams.

For the 200GBASE-R 1:1, 400GBASE-R 2:2, 800GBASE-R 4:4 PMA, and 1.6TBASE-R 8:8 PMAs, the nominal interface data rate per stream is 212.5 Gb/s.

For the 1.6TBASE-R 16:16 PMA, the nominal interface data rate per stream is 106.25 Gb/s.

PMA Service Interface subclauses

- Current clause structure and proposed reorganization

176.2 PMA Service Interface

176.3 Service Interface below the PMA

176.4 [m:n] SM-PMAs

176.4.2 Service Interfaces

176.4.2.1 PMA Service Interface

176.4.2.2 Service Interface below the PMA

176.5 [n:m] SM-PMAs

176.5.2 Service Interfaces

176.5.2.1 PMA Service Interface

176.5.2.2 Service Interface below the PMA

176.6 [n:n] SM-PMAs

176.6.2 Service Interfaces

176.6.2.1 PMA Service Interface

176.6.2.2 Service Interface below the PM

Proposed changes:

1. Move content from 176.4.2.1, 176.5.2.1 and 176.6.2.1 into 176.2

2. Move content from 176.4.2.2, 176.5.2.2 and 176.6.2.2 into 176.3

3. Remove 176.4.2, 176.5.2 and 176.6.2

<PMA Features List>

Clause 176

Comment #182

PMA Feature List – comment #182

176.1.4 Summary of PMA functions

D1.1 current:

- Adapt the PCS lane (PCSL) formatted signals to the appropriate number of abstract or physical lanes operating at 212.5 Gb/s
- Symbol-level multiplexing and demultiplexing
- PAM4 encoding and decoding
- Providing signal status information
- Optional local loopback from/to the PMA service interface
- Optional remote loopback from/to the service interface below the PMA
- Optional test-pattern generation and detection

Proposed new:

- Adapting data from PCS-formatted lanes (PCSLs) to one or more physical lanes operating at 212.5 Gb/s
- Symbol-level multiplexing and demultiplexing
 - Alignment to RS-FEC symbols using the PCSL alignment markers
 - Delay of alternating PCSLs by two FEC codewords for 200GBASE-R and 400GBASE-R PMAs
 - Four-way FEC codeword interleaving at all data rates
- PAM4 encoding and decoding
- Optional local and remote loopbacks
- Optional test-pattern generation and detection.