802.3dj D1.1 Comment Resolution Optical Topics

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Matt Brown (Alphawave Semi), 802.3dj Chief Editor

Introduction

- This slide package was assembled by the 802.3dj editorial team to provide background and detailed resolutions to aid in comment resolution.
- Specifically, these slides are for the various optical track comments.

ILT

ILT, block diagram
Comments 98, 106, 103, 105, 111, 113

These comments ask to update the optical PMD block diagrams to better address link training:
- show the complete transmit and receive functions
- label TX and RX lane explicitly and uniquely; proposes using same labels used for CR/KR
- associate the SIGNAL_OK signal with the receive function

In order for ILT to work there must be explicit pairing between a transmit lane and a receive lane.

Cl **180** *SC* **180.5.1** *P* **376** *L* **6** # 98

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **TR** *Comment Status* **D** *ILT*

Figure is missing PMD transmit function and PMD receive function

SuggestedRemedy

Add PMD transmit function between PMA and optical transmitter and PMD receive fucntion between optical receiver and receive PMA.
Also add following lable between PMD transmit function and optical transmit "Sli"
Also add following lable between optical receive and PMD receive function "DLi"
PMD Signal_OK shold be connected to the PMD receive function.
Alternatively you could combine PMD TX function with optical TX and optical RX with PMD RX function.
In Figure 180-2 L0-L3 (left) at PMA input can be replaced with SL1-SL3 and L0-L3 (Right) with DL0-DL3.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Background and proposed changes are provided in the "ILT" slides in following editorial presentation for CRG review.
URL/issenhuth_3dj_01_2409

Cl **182** *SC* **182.5.1** *P* **427** *L* **10** # 106

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **TR** *Comment Status* **D** *ILT*

Figure is missing PMD transmit function and PMD receive function

SuggestedRemedy

Add PMD transmit function between PMA and optical transmitter and PMD receive fucntion between optical receiver and receive PMA.
Also add following lable between PMD transmit function and optical transmit "Sli"
Also add following lable between optical receive and PMD receive function "DLi"
PMD Signal_OK shold be connected to the PMD receive function.
Alternatively you could combine PMD TX function with optical TX and optical RX with PMD RX function.
In Figure 182-2 L0-L3 (left) at PMA input can be replaced with SL1-SL3 and L0-L3 (Right) with DL0-DL3.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #98

Cl **181** *SC* **181.5.1** *P* **401** *L* **22** # 103

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **TR** *Comment Status* **D** *ILT*

Figure is missing PMD transmit function and PMD receive function

SuggestedRemedy

Add PMD transmit function between PMA and optical transmitter and PMD receive fucntion between optical receiver and receive PMA.
Also add following lable between PMD transmit function and optical transmit "Sli"
Also add following lable between optical receive and PMD receive function "DLi"
PMD Signal_OK shold be connected to the PMD receive function.
Alternatively you could combine PMD TX function with optical TX and optical RX with PMD RX function.
In Figure 181-2 L0-L3 (left) at PMA input can be replaced with SL1-SL3 and L0-L3 (Right) with DL0-DL3.
Use lable L0-L3 or Symbol (Lamda0-Lamda3) at input and ouptut of the Mux/De-mux. If you change L0 to Lamda0 then also need to change lable in tbale 181-3

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #98

Cl **181** *SC* **181.6** *P* **403** *L* **40** # 105

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **TR** *Comment Status* **D** *ILT*

Add sentence describing where L0-L3 data are coming

SuggestedRemedy

L0 to L3 into the Mux data are sourced respectively from SL1 and Sl2. L0 to L3 de-mux output data propagate respectively to DL1 to DL3. Also add reference to Figure 181-2

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #98

Cl **183** *SC* **183.5.1** *P* **453** *L* **15** # 111

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **TR** *Comment Status* **D** *ILT*

Figure is missing PMD transmit function and PMD receive function

SuggestedRemedy

Add PMD transmit function between PMA and optical transmitter and PMD receive fucntion between optical receiver and receive PMA.
Also add following lable between PMD transmit function and optical transmit "Sli"
Also add following lable between optical receive and PMD receive function "DLi"
PMD Signal_OK shold be connected to the PMD receive function.
Alternatively you could combine PMD TX function with optical TX and optical RX with PMD RX function.
In Figure 183-2 L0-L3 (left) at PMA input can be replaced with SL1-SL3 and L0-L3 (Right) with DL0-DL3.
Use lable L0-L3 or Symbol (Lamda0-Lamda3) at input and ouptut of the Mux/De-mux. If you change L0 to Lamda0 then also need to change lable in tbale 183-3

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #98 .

Cl **183** *SC* **183.6** *P* **455** *L* **40** # 113

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **TR** *Comment Status* **D** *ILT*

Add sentence describing where L0-L3 data are coming

SuggestedRemedy

L0 to L3 into the Mux data are sourced respectively from SL1 and Sl2. L0 to L3 de-mux output data propagate respectively to DL1 to DL3. Also add reference to Figure 183-2

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #98

ILT, mapping signals to connector pins
Comments 100, 101, 102, 108, 109, 110

Cl 180 SC 180.8.3.1.1 P 386 L 3 # 100
Ghiasi, Ali — Ghiasi Quantum/Marvell
Comment Type TR Comment Status D ILT
Add sentence describing where TX/RX data are coming

SuggestedRemedy
Tx1 and Tx2 data are sourced respectively from SL1 and SI2. Rx1 and Rx2 data propagate respectively to DL1 and DL2. Also add reference to Figure 180-2

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Background and proposed changes are provided in the "ILT" slides in following editorial presentation for CRG review.
URL/issenhuth_3dj_01_2409

Cl 180 SC 180.8.3.1.2 P 386 L 25 # 101
Ghiasi, Ali — Ghiasi Quantum/Marvell
Comment Type TR Comment Status D ILT
Add sentence describing where TX/RX data are coming

SuggestedRemedy
Tx1, Tx2, Tx3, and T4 data are sourced respectively from SL1, SL2, SL3, and SI4. Rx1, Rx2, Rx3, and Rx4 data propagate respectively to DL1, DL2, DL3, and DL4. Also add reference to Figure 180-2

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #100

Cl 180 SC 180.8.3.1.3 P 386 L 44 # 102
Ghiasi, Ali — Ghiasi Quantum/Marvell
Comment Type TR Comment Status D ILT
Add sentence describing where TX/RX data are coming

SuggestedRemedy
Tx1 to T8 data are sourced respectively from SL1 to SI8. Rx1 to Rx8 data propagate respectively to DL1 to DL8. Also add reference to Figure 180-2

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #100

Cl 182 SC 182.8.3.1.1 P 437 L 4 # 108
Ghiasi, Ali — Ghiasi Quantum/Marvell
Comment Type T Comment Status D ILT
Add sentence describing where TX/RX data are coming

SuggestedRemedy
Tx1 and Tx2 data are sourced respectively from SL1 and SI2. Rx1 and Rx2 data propagate respectively to DL1 and DL2. Also add reference to Figure 182-2

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #100.

Cl 182 SC 182.8.3.1.2 P 437 L 25 # 109
Ghiasi, Ali — Ghiasi Quantum/Marvell
Comment Type TR Comment Status D ILT
Add sentence describing where TX/RX data are coming

SuggestedRemedy
Tx1, Tx2, Tx3, and T4 data are sourced respectively from SL1, SL2, SL3, and SI4. Rx1, Rx2, Rx3, and Rx4 data propagate respectively to DL1, DL2, DL3, and DL4. Also add reference to Figure 182-2

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #100.

Cl 182 SC 182.8.3.1.3 P 437 L 44 # 110
Ghiasi, Ali — Ghiasi Quantum/Marvell
Comment Type TR Comment Status D ILT
Add sentence describing where TX/RX data are coming

SuggestedRemedy
Tx1 to T8 data are sourced respectively from SL1 to SI8. Rx1 to Rx8 data propagate respectively to DL1 to DL8. Also add reference to Figure 182-2

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #100.

These comments ask for text explicitly linking the each RX and TX lanes to a specific pin on each of the optical connector types.

The optical connectors currently specified for DRn/DRn-2 PMD/MDI

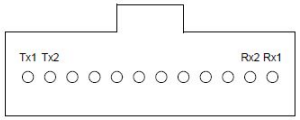


Figure 180–7—400GBASE-DR2 optical lane assignments

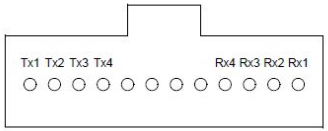


Figure 180–8—800GBASE-DR4 optical lane assignments

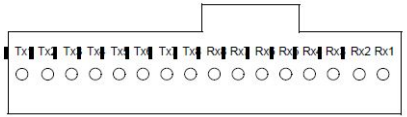


Figure 180–9—1.6TBASE-DR8 optical lane assignments

For 400GBASE-DR2/DR2-2, 800GBASE-DR4/DR4-2, and 1.6TBASE-DR/DR8-2, the connectors with fiber labelling are shown to the left.

A figure for the connector for 200GBASE-DR/DR-2 is not shown since (presumably) it is a single-fiber connector and thus lane assignment is obvious.

Test points
Comment 399

Cl 180 SC 180.5.1 P 376 L 30 # 399

Ran, Adee Cisco Systems, Inc.

Comment Type T *Comment Status* D *Test points*

"these test points will not typically be accessible in an implemented system"
"will" is improper here.

This sentence is inherited from older optical PMD clauses which implicitly assumed the PMD interface consists of analog signals (the diagrams showed the retimer as part of the PMA - see e.g. Figure 121-2).

Since this PMD's functional specification includes the retiming function (and its service interface consists of PAM4 symbols, not an analog signal), This sentence is not warranted anymore. These test points are typically quite accessible through the adjacent PMA that can inject test patterns and check the received symbols, and are useful for system testing as well as component testing. They are just not exposed to external testing.

SuggestedRemedy

Change to "these test points are typically not directly accessible in an implemented system"

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Test points TP0 and TP4 have no significance for the PMDs defined in 180, 181, 182, or 183.
Also, note that comment #98 proposes updates to Figure 180-2 that might be relevant to this comment.
Delete TP0 and TP4 labels in Figure 180-2, Figure 181-2, Figure 182-2, Figure 183-2.
In 180, 181, 182, 183 remove the text (or similar) "TP1<0:3> and TP4<0:3> are optional reference points that may be useful to implementors for testing components (these test points will not typically be accessible in an implemented system)."
[Editor's note: CC 180, 181, 182, 183]

This comment proposes changes to the text describing test points TP1 and TP4. However, the editorial team noted that these test points are never described and are not needed for any specifications for these new PMDs.

It is therefore proposed that test points TP1 and TP4 be deleted from the block diagram and that the related explanatory text be deleted as well.

Signal labelling used for electrical PMDs

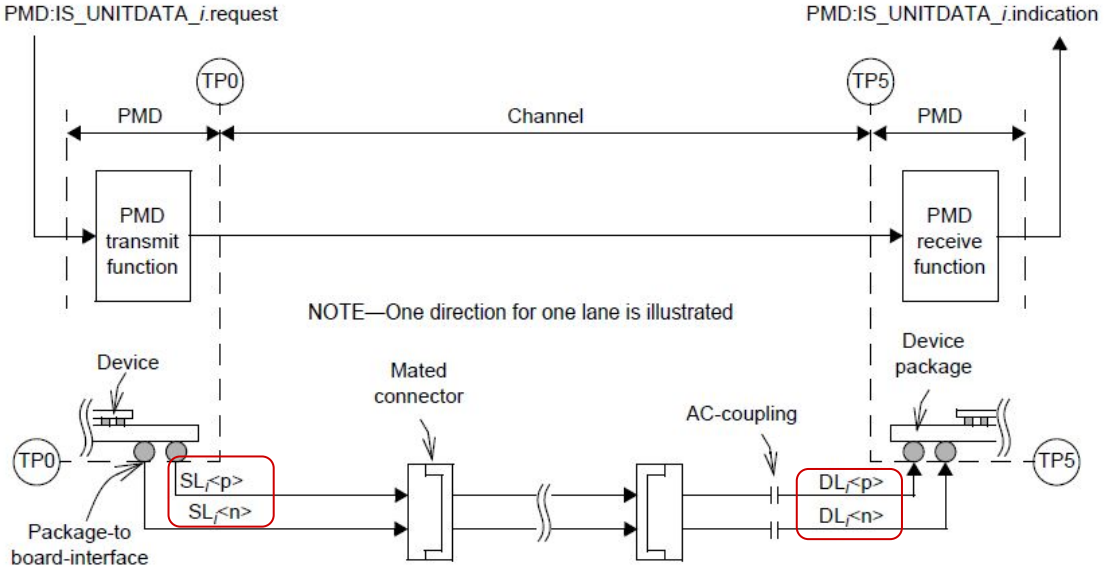


Figure 163–2—100GBASE-KR1, 200GBASE-KR2, or 400GBASE-KR4 link

Electrical PMDs (CR/KR) label the signals on each lane as SLi and DLi.
SLi is source lane number i, e.g., SL0 is source lane 0.
DLi is destination lane i, e.g., DL0 is destination lane 0.

SLi is associated with a transmitter.

DLi is associated with a receiver.

This labelling scheme can be used to label the optical signals on each lane.

Definition of optical PMD transmit function and receive function

180.5.2 PMD transmit function

The PMD Transmit function shall convert the *n* symbol streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_*n*-1.request into *n* separate optical signals. The *n* optical signals shall then be delivered to the MDI, which contains *n* parallel light paths for transmit, according to the transmit optical specifications in this clause. The highest optical power level in each signal shall correspond to tx_symbol = three and the lowest shall correspond to tx_symbol = zero.

180.5.3 PMD receive function

The PMD Receive function shall convert the *n* parallel optical signals received from the MDI into separate symbol streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_*n*-1.indication, all according to the receive optical specifications in this clause. The higher optical power level in each signal shall correspond to rx_symbol = three and the lowest shall correspond to rx_symbol = zero.

The PMD transmit function is defined as PAM4 symbols and optical signal out.

The PMD receiver function is defined as optical signal in and PAM4 symbols out.

The PMD subsumes the entire signal processing function, except that the for DRn-2, FR4, an DR4 the Inner FEC further processes the detected symbols.

SIGNAL_OK definition
Comment 478

180.3 Physical Medium Dependent (PMD) service interface

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.indication primitive corresponds to the variable training_status of the inter-sublayer training function, as defined in 176A.11.2.1. When SIGNAL_OK is either IN_PROGRESS or FAIL, the rx_symbol parameters of PMD:IS_UNITDATA_i.indication on all lanes are unspecified.

Editor's note: PMD:IS_SIGNAL.request(SIGNAL_OK) (transmit direction) as required by the ILT function needs to be defined. A proposal in this regard is encouraged.

Cl **178** *SC* **178.4** *P* **374** *L* **16** # 478

Brown, Matt — Alphawave Semi

Comment Type **T** *Comment Status* **D** *PMD service interface*

To support the necessary signaling for ILT PMD:IS_SIGNAL.request(SIGNAL_OK) is needed.

SuggestedRemedy

The SIGNAL_OK parameter of the PMD:IS_SIGNAL.request provides the status from ISLs above the PMD.
Similar for 179.4, 180.3, 181.3, 182.3, and 183.3.
Delete related editor's notes.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
[Editor's note: technically incomplete service interface]
[Editor's note: Changed page from 374 to 297]
[Editor's note: CC 178, 179, 180, 181, 182, 183]
Implement suggested remedy with editorial license.

The SIGNAL_OK parameter (indication, or receive direction) is no longer a function of the signal detect function. Instead it is based on the state of the ILT function. The signal detect state is indicated in management variable global_PMD_signal_detect.

In Draft 1.1, the SIGNAL OK parameter (request, or receive direction is missing per the editor's note).

Comment #478 will (common track ILT topic) resolves this.

But the optical blocks diagrams need to be updated to reflect the above details.

Issues with and suggestions for the current optical block diagrams Not at proposal

TP1 and TP4 is never defined in any of the optical clauses in 802.3dj and is not necessary. Should be deleted from diagram.

SIGNAL_OK signal is received from PMA or Inner FEC as is processed by the ILT function. Need to depict this.

Rather than labelling the inputs to the transmit function (these can be arbitrary) label the output so that mapping to MDI pins can be defined. Adopt signal labelling for KR/CR PMDs.

With adoption of ILT, SIGNAL_OK (sent to PMA or Inner FEC) is set by the ILT function, not the signal detect function.
Change SIGNAL_OK here to global_PMD_signal_detect.
Show SIGNAL_OK emanating from the ILT function.

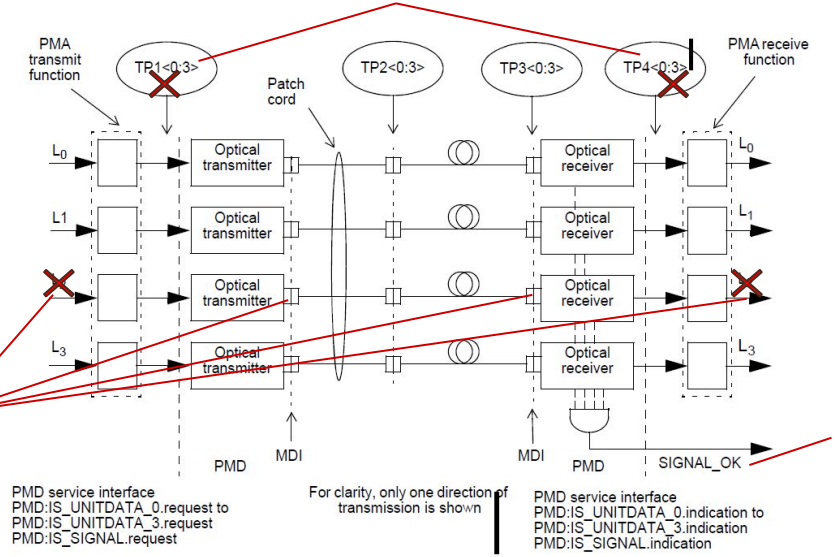
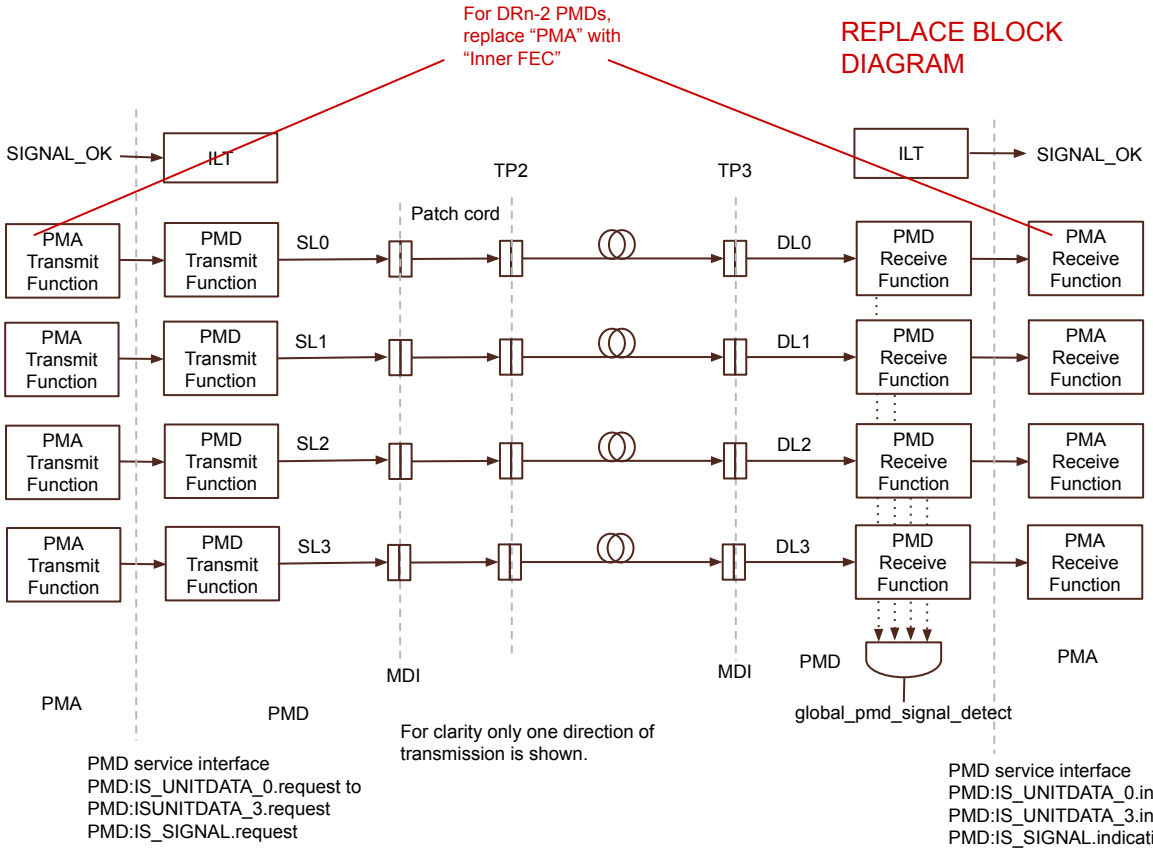


Figure 180–2—Block diagram for 800GBASE-DR4 transmit/receive paths

~~TP1<0:3> and TP4<0:3> are optional reference points that may be useful to implementors for testing components (these test points will not typically be accessible in an implemented system).~~

As above, TP1 and TP4 is never defined in any of the optical clauses in 802.3dj and is not necessary. This text should be deleted.

Proposal: The resulting diagram for xBASE-DRn/DRn-2



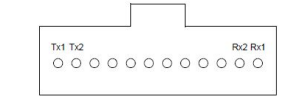


Figure 180–7—400GBASE-DR2 optical lane assignmei

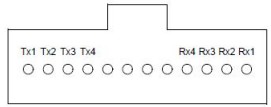


Figure 180–8—800GBASE-DR4 optical lane assignments

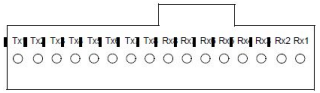
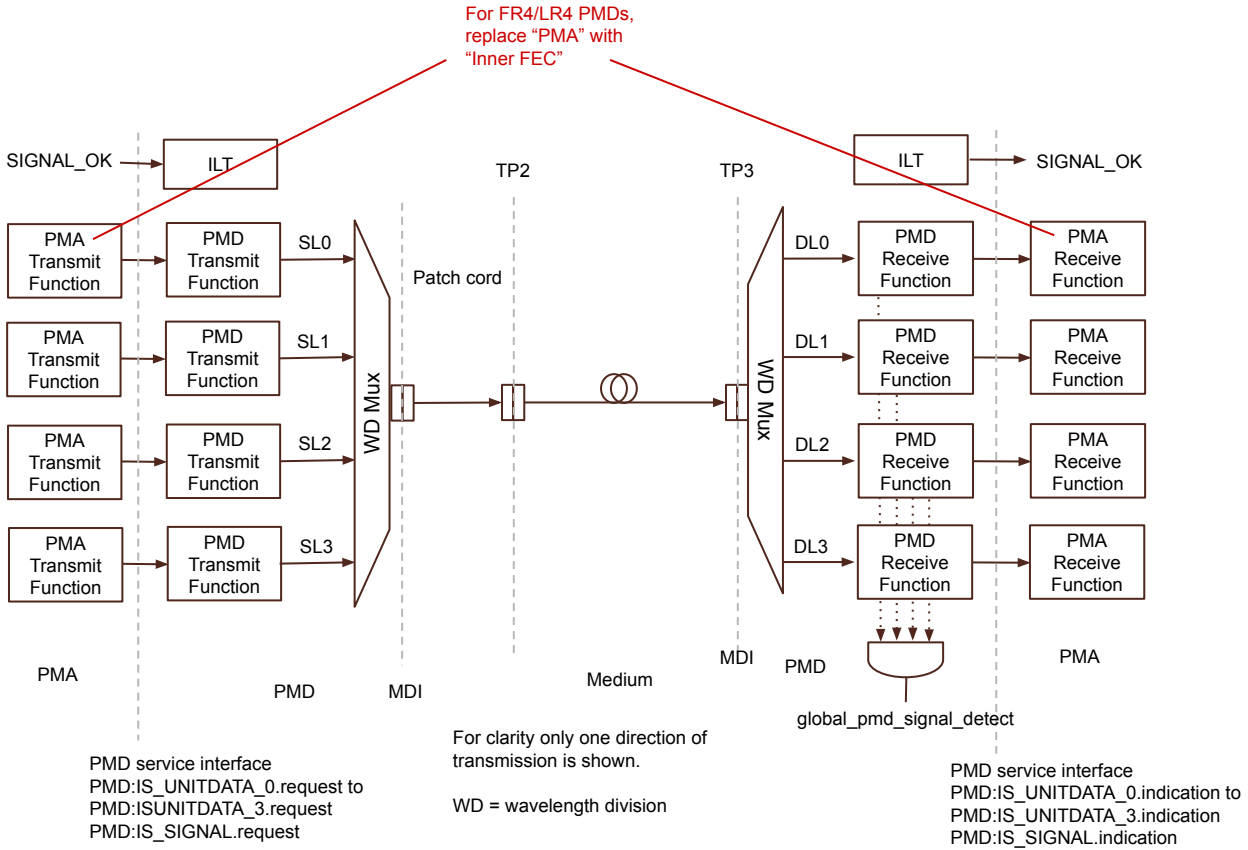


Figure 180–9—1.6TBASE-DR8 optical lane assignments

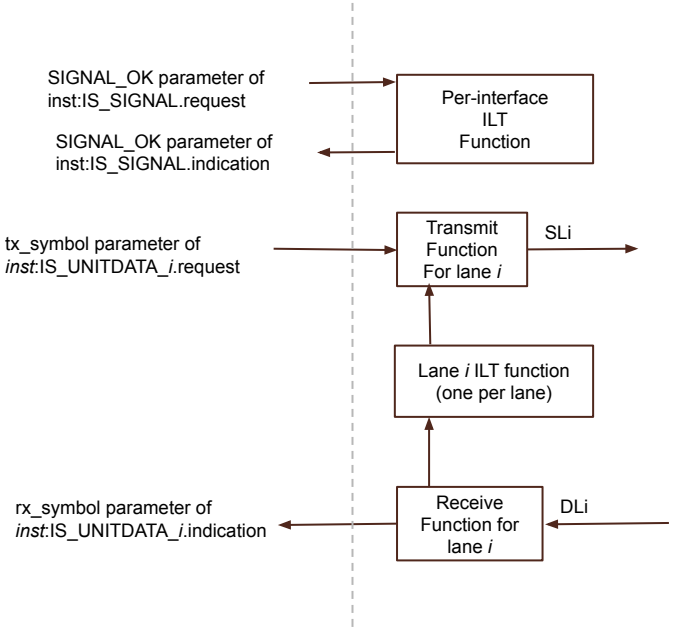
NEW TABLE

Table 180-x–Mapping PMD signals to MDI pins	
PMD signal	**MDI pin**
SL0	TX1
SL1	TX2
SL2	TX3
SL3	TX4
SL4	TX5
SL5	TX6
SL6	TX7
SL7	TX8
DL0	RX1
DL1	RX2
DL2	RX3
DL3	RX4
DL4	RX5
DL5	RX6
DL6	RX7
DL7	RX8

Proposal: The resulting diagram for 800GBASE-LR4/FR4/FR4-500



Proposal: per-interface and per lane (bidirectional) nature of link training



There is a piece missing from the optical block diagram (e.g., Figure 180-2), as well as the electrical block diagrams (e.g., Figure 163-2) relating to the bidirectional nature of ILT. This is relevant to electrical PMDs, optical PMDs, and AUI components.

The ILT signaling per lane is bidirectional. In other words, there is a function that acts on behalf of each transmitter-receiver pair on lane i.

There is also an ILT function that acts on the set of lanes for a PMD or AUI component.

The diagram on the left depicts this concept for a PMD or host side AUI component (for a network side AUI component the transmit/receive, tx/rx, and request/indication need to be swapped).

A diagram similar to this should be added to Annex 176A along with appropriate explanatory text. A reference to this figure and related explanation can be added to the ILT subclause for each PMD and AUI.

The per-lane ILT function manages the link training signaling between the partners and controls the local transmitter for one lane.

The per-interface manages the ILT state for the whole PMD or AUI component and provides the inter-sublayer signaling.

Suggestion to address breakout, per comments 341 and 342

Cl 180 SC 180.8.3.1 P 386 L 48 # 341

D'Ambrosia, John Futurewei, U.S. Subsidiary of Huawei

Comment Type T *Comment Status* D *MDI*

Any DR MDI is also capable of supporting any lower lane count DR interfaces than what it is specified for as applicable, as well as combinations. Clause 180.8.3.1.1 starts off specifying 400GBASE-DR2 with twelve total positions. It could support multiple ports of 200GBASE-DR1, or could support a combination of a single 400GBASE-DR2 with two ports of 200GBASE-DR1.

SuggestedRemedy

Add subclause before 180.8.3.1.1 - Optical lane assignments for 200GBASE-DR1.
Copy and modifiy text from 180.8.3.1.1 to reflect 200GBASE-DR1 with editorial license
Add - only a single instance of 200GBASE-DR1 is specified.
To: 180.8.3.1.1 - only a single instance of 400GBASE-D2 is specified.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.

The commenter has offered to provide a supporting presentation.

Pending CRG review of presentation and discussion.

Cl 182 SC 182.8.3.1.1 P 437 L 49 # 342

D'Ambrosia, John Futurewei, U.S. Subsidiary of Huawei

Comment Type T *Comment Status* D *MDI*

Any DRx-2 MDI is also capable of supporting any lower lane count DRx-2 interfaces than what it is specified for as applicable, as well as combinations. Clause 182.8.3.1.1 starts off specifying 400GBASE-DR2-2 with twelve total positions. It could support multiple ports of 200GBASE-DR1-2, or could support a combination of a single 400GBASE-DR2-2 with two ports of 200GBASE-DR1-2.

SuggestedRemedy

Add subclause before 182.8.3.1.1 - Optical lane assignments for 200GBASE-DR1-2.
Copy and modifiy text from 182.8.3.1.1 to reflect 200GBASE-DR1-2 with editorial license
Add - only a single instance of 200GBASE-DR1-2 is specified.
To: 182.8.3.1.1 - only a single instance of 400GBASE-D2-2 is specified.

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
The commenter has offered to provide a supporting presentation.
Pending CRG review of presentation and discussion.

The optical signal labels and mapping tables proposed on previous slides can be used to extend mapping of multiple PMDs to the same optical connector.

The default for a single PMD would be PMD #0.

This one table can be used for optical connectors widths with different numbers of pins, ignoring rows with pins not supported, e.g., for 12-pin connect ignore rows for TX7, TX8, RX7, RX8.

Table 180-x–Mapping PMD signals to MDI pins

PMD # : PMD signal				
200GBASE-DR1	**400GBASE-DR2**	**800GBASE-DR4**	**1.6T BASE-DR8**	**MDI pin**
0:SL0	0:SL0	0:SL0	SL0	TX1
1:SL0	0:SL1	0:SL1	SL1	TX2
2:SL0	1:SL0	0:SL2	SL2	TX3
3:SL0	1:SL1	0:SL3	SL3	TX4
4:SL0	2:SL0	1:SL0	SL4	TX5
5:SL0	2:SL1	1:SL1	SL5	TX6
6:SL0	3:SL0	1:SL2	SL6	TX7
7:SL0	3:SL1	1:SL3	SL7	TX8
0:DL0	0:DL0	0:DL0	DL0	RX1
1:DL0	0:DL1	0:DL1	DL1	RX2
2:DL0	1:DL0	0:DL2	DL2	RX3
3:DL0	1:DL1	0:DL3	DL3	RX4
4:DL0	2:DL0	1:DL0	DL4	RX5
5:DL0	2:DL1	1:DL1	DL5	RX6
6:DL0	3:DL0	1:DL2	DL6	RX7
7:DL0	3:DL1	1:DL3	DL7	RX8