Considerations on the testing methodology for 200G/L optical links --Relating comments 318,316,314,317

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Introduction

- In D1.1, two new metrics of error ratio were introduced for data reliability, i.e. block error ratio and FEC codeword error ratio.
- The two metrics are referenced in the definition of (stressed) receiver sensitivity in all IM-DD optical spec.
- However, how to apply these two metrics in the development of the specs of 200G/L optics are yet to be discussed by the task force.
- This contributions reviews the common method of optical spec, discusses the distinctions caused by the new metrics and offers suggestion on moving forward.

The metric system of PAM4 optical signaling Tx and Rx

What was used in 100G/L optics, and earlier generations



A stressed Tx signal + Rx. DUT depicts Stressed RS

Changes to 200G/L optics, and possible future generations



Starts from Changing BER (2) to Block Error Ratio (2)

Bit Error Ratio (2): pre-KP4, over single PMD lane. Simple translation to (1) (or to be more precise, BER at TP4) Block Error Ratio (2):

- post-KP4
- over all PCS lanes of one 800GE/1.6TE MAC, →we need to evaluate optical lanes individually (not discussed here
- with additional BER allocation for AUI links, \rightarrow need to be supported by equipment algorithms.
- no direct relation to (1) \rightarrow next page
- A equivalent metric FEC CW error ratio, may not be very handy for optical spec.

Changes to 200G/L optics, and possible future generations



Changes to 200G/L optics, and possible future generations



Practical Issues, some answered, some still hanging

Possible architectures of deploying 200G/L optics With Legacy 100G/L electrical links

May not be friendly to the new Metrics, Likely be the testing setup for next year or two



New Metrics describes the link between the two re-timers, what is the assumption of BER for the 100G/L AUI link?



Possible architectures of deploying 200G/L optics With 200G/L electrical links

In CL174A: A PMD is expected to meet the block error ratio specification in 174A.6 with BER_{added} equal to 4×10^{-5} BER_{added} represents the total random BER allocated to other physically instantiated inter-sublayer link in the PHY

✓ Confirmed by logical and electrical experts:

4x10⁻⁵ represents that of a two-part 200G/L AUI architecture at both ends of the link, i.e. the worst case possible



Consistency between new and legacy testing setup

Need feedback from Logical track





What was used in practical manufacturing





- Impractical to test Rx against multiple designs
- DUT self loopback/ Golden Tx was commonly used
- RS and SRS combined provide good margin to tolerate variations
- FEC bin are also tested
 - In design stage and some manufacturing cases
 - Helps to understand Error behavior
 - Helps to identify impairments
 - Possible to generate FEC bin Mask



- Vendor specific BER goal varies, 1e-6 being a typical value.
- RS in 802.3 holds to be the bar of interoperability
- The BER error floor
 - Not yet captured by the spec in 802.3
 - Commonly considered in the design of sub-systems
 - Incorporated in validation, qualification and manufacturing
 - Often mentioned in the discussion of 802.3 specs

Some more practical questions

802.3 standardized metrics

BER FEC bin

Block Error ratio FEC codeword Error

Vendor specific metrics

Enhanced BER Error Floor FEC bin mask – method dependent

Last and very importantly

What is the suggested data collection time? (how to calculate, should it be different for 800GE and 1.6TE

User habit will not change easily.

If This TF deems certain change necessary, we should work on it and advertise it fast, or we are writing things on paper without actual usage.

Suggestion

- This contribution raised a series of questions regarding the new metric of data reliability, hoping to advance understanding between the optics and the logic mathematics.
- The authors believes more discussions on the new metrics are needed when applying to 200G/L optical PMDs.
- Gap between new and legacy metric system of optical PMDs exists and needs to be written for reference, if the TF decide to follow through with new metrics

BACK UP SLIDES

Changes in 200G/L

One part AUI link



For Rx

- A typical module Tx commonly used in place of a reference Tx + the module Rx to be tested
- BERT needed. In practice, DSP could generate PRBS for testing convenience ← not sure if this still holds.
- Block Error Ratio(referred to as BlockER) defined in 174A.6. (not fully understand yet). But should be reported at (2).
 - Should the encoder and decoder of inner FEC in the module be turned on when recording BlockER ?
 - Does the BlockER require change of BERT or other equipment alike?
 - BlockER doesn't seem to have a straight forward relation to the target SER at ③ used in Tx. Is it so? ← how to correlate the Tx and Rx performance, so that we could say a Tx with TECQ=a & TDECQ=b is capable of closing the link.
- BlockER curve drawn using numbers reported at 2. Or FEC codeword error ratio at 2
 - Can module vendors later build some kind of relation between metric at ① and BlockER @ ② , so they could simplify the testing de debugging.
- Will there be inner FEC codeword error ratio at ④?
- Inner FEC bin counter defined at ④, will it be used to measure optical link performance? How? Normative or informative?
- KP4 FEC bin reported at 2

Changes in 200G/L

Two part AUI link



Target PAM4 SER at (3) to be discussed. Preferably one single value per FEC mode.

For Rx

- A typical module Tx commonly used in place of a reference Tx + the module Rx to be tested
- BERT needed. In practice, DSP could generate PRBS for testing convenience not sure if this still holds.
- Block Error Ratio reported at 2.
- BlockER curve drawn using BlockER reported at (2), not exactly pre-KP4 BER.
- Inner FEC bin counter defined at (4)
- KP4 FEC bin reported at (5)
- It seems Testing of BlockER need to assume certain 200G/L AUI link, correct? (applies to both one-part and two-part AUI link)

Changes in 200G/L, with 100G/L AUI



• Target PAM4 SER at (3) to be discussed. Preferably one single value per FEC mode.

For Rx: first of all, do we use 200G/L methodology or 100G/L pre-KP4 FEC

- A typical module Tx commonly used in place of a reference Tx + the module Rx to be tested
- BERT needed. In practice, DSP could generate PRBS for testing convenience not sure if this still holds.
- Block Error Ratio reported at (2), correct?
- BlockER curve drawn using BlockER reported at (2)
- Pre-KP4 BER as we know in 100G/L at (5)
- Inner FEC bin counter defined at ④
- KP4 FEC bin reported at (5)

	Sum = NT	Sum = NE
Bin0	903668687198	4816
Bin1	142901852	4816
Bin2	300529	4816
Bin3	3313	1352
Bin4	109	100
Bin5	7	7
Bin6	1	1
Bin7	0	0
Bin8	0	0
Bin9	0	0
Bin10	0	0
Bin11	0	0
Bin12	0	0
Bin13	0	0
Bin14	0	0
Bin15	0	0
Bin16+	0	0

Ref: https://arista.my.site.com/AristaCommunity/s/article/monitoring-link-quality-using-forwarderror-correction-fec-data-on-arista-switches

FEC CW Error Ratio = NE/NT

Assume Random Error,



Optics :Output at Optical Rx of interest



The missing Piece to connect Tx and Rx performance

To independently quantify the performance of Tx, Crucial for qualification and manufacturing

