Block error ratio using PCS-based measurements

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Introduction

- 174A.6.1 defines a block error ratio metric for inter-sublayer links (ISLs) in a PHY-to-PHY or extender path
- It is an estimate of the codeword error ratio that would be observed at the Reed-Solomon decoder at the end of the path
- It is based on errors observed at the receiver under test and it accounts for error ratio allocations made for ISLs that are not included in the test
- PMA-based error counters and the corresponding calculations are defined
- The procedure allows individual physical lanes to be tested one-at-a-time
- There are also provisions for the use of PCS-based measurements, but a complete test procedure is not defined
- This proposal addresses PCS-based measurements of block error ratio

Interesting questions...

Why are PCS-based measurements needed?

- PMA-based measurements can be made at the PMA adjacent to the PCS
- This contribution assumes it is desirable to have an alternative procedure based on PCS-level data

Why not measure the codeword error ratio directly?

- It would not include the impact of errors allocated to other ISLs (BER_{added})
- Receiver testing may be done one physical lane at a time and some level of post-processing is required to combine the results

Compare PMA- and PCS-based measurements

PMA-based measurements	PCS-based measurements
• Measured on an individual physical lane • Measurements of individual lanes are combined mathematically	• Measured across all PCS/physical lanes • Errors introduced on physical lanes other than the lane under test may need to be removed

Description	PMA counter	PCS counter
Total blocks	tbtcount	FEC_cw_counter (48-bit)
Error-free blocks	tbecount(0)	Mathematically derived [1]
Blocks with *k* errors	tbecount(*k*), *k* = 1 to 15	FEC_codeword_error_bin_*i*, *i* = 1 to 15 (32-bit)
Blocks with > 15 errors	tbecount(16)	FEC_uncorrected_cw_counter (32-bit)

[1] FEC_codeword_error_bin_0 = FEC_cw_counter – FEC_corrected_cw_counter – FEC_uncorrected_cw_counter

PCS-based measurement of block error ratio

- Define the measured error histogram $H_m(k)$ based on the PCS counters (using the mapping shown on slide 4)
- If individual physical lanes are tested one-at-a-time, the measurements are combined using the procedure on slide 7
- Add the error ratio allocation for ISLs not included in the test (BER_{added}) using steps c) and d) defined in 174A.6.1.4
- Compute the block error ratio as defined in step e) of 174A.6.1.4

Measurements of individual physical lanes

- Receiver testing includes the addition of stress (noise or jitter)
- Stress is sometimes added to only one lane of a multi-lane receiver due to equipment limitations, calibration complexities, etc.
- If stress can be added to all lanes simultaneously, the measured histogram can be used as is
- Otherwise, errors on unstressed lanes should be minimized since they will be (incorrectly) attributed to the lane under test

Combining measurements from individual physical lanes

1. Let $H_m^{(i)}(k)$ be the measured histogram with stress applied to lane i
2. Let $H_m^{(u)}(k)$ be the measured histogram with no stress applied to any lane
3. Initialize $H_m(k)$ to $H_m^{(0)}(k)$ and i to 1
4. Assign $H_m(k)$ the result of the following equation

$$H_m(k) = \sum_{j=0}^{k} H_m(j) H_m^{(i)}(k-j)$$

5. Optionally de-convolve $H_m^{(u)}(k)$ from $H_m(k)$ [1]
6. Increment i
7. If i < p (the number of lanes) then go to step 4

[1] This step removes errors from unstressed lanes from the result (p – 1 deconvolutions for p lanes)

A note about combining of error histograms

- To shorten the error histograms, $H(16)$ is defined to be the probability of more than 15 errors in a block

$$H(16) = \sum_{k>15} G(k) \quad \text{where } G(k) \text{ is the unshortened error histogram}$$

- The following equation is given for the combination of histograms $H_x(k)$ and $H_y(k)$ corresponding to independent error events

$$H(k) = \sum_{j=0}^{k} H_x(j) H_y(k-j) \qquad \text{Equation (174A−3)}$$

- This equation does not include all of the terms that will lead to more than 15 errors in a block when k = 16
- The result is expected to be close in normal circumstances but it can be made exact with an additive term

Possible adjustment to Equation (174A−3)

- No change for k = 0 to 15
- Modify equation for k = 16 as follows

$$H(16) = \underbrace{\sum_{j=0}^{16} H_x(j) H_y(16-j)}_{\text{Original equation}} + \underbrace{\sum_{j=1}^{16} H_x(j) \sum_{i=17-j}^{16} H_y(i)}_{\text{Adjustment to include missing terms}}$$

Summary

- Since there will always be a PMA adjacent to the PCS, a block error ratio measurement using PMA-level data is always an option
- A definition block error ratio using PCS-based measurements may not be necessary
- If is desirable to maintain this as an option, a definition of block error ratio using PCS-based measurements has been provided
- A small adjustment to the equation for the combination of error histograms should be considered for improved accuracy