

Addressing Clause 184 D1.2 text for 800GBASE-LR1

(Support contribution for Comments #420, 422, 423,
424, 425, 426)

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P802.3dj Plenary Meeting, Vancouver, Canada, Nov 2024

Comment #420: Naming of RX signals

- Comment:
 - ADC input signals in Figure 184-2 are labelled RX_Ai, RX_Aq, RX_Bi and RX_Bq. I think the labels A/B are used to highlight the fact that the polarization angle at the receiver is not necessarily aligned with the X/Y polarizations at the transmitter. However, A/B are somewhat arbitrary and do not clearly reflect the fact that those are orthogonal polarizations.
- Suggested Remedy:
 - Use H/V (for horizontal and vertical) instead of A/B because it is common to use these letters in coherent DSPs instead of X/Y to indicate orthogonal polarizations. i.e. use RX_Hi, RX_Hq, RX_Vi, RX_Vq. Same change would also apply to uses of these names in 184.5.1 on page 508, lines 45, 47 and 51 and in 184.5.2 on page 509, line 5 and 184.5.7 on page 510, line 10.

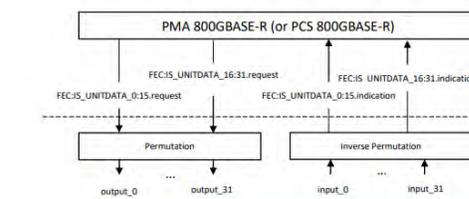
Comment #422/#423:

- **Background:** Permutation function prerequisites (updated):

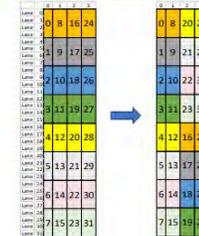
- 20bit RS(544,514) symbol alignment across lanes
- Partial lane reorder with lanes from 800GBASE-R PCS flow 0 in lanes 0-15 and lanes from flow 1 in lanes 16-31
- Complete lane reorder and lane de-skew to RS(544,514) codeword boundaries is optional

Motion #5 from July'23 Plenary: Move to adopt BCH FEC as defined in kota_3dj_01a_2307.pdf slides 6-18 as the baseline FEC specification for the single wavelength 10 km 800Gb/s optical PMD

Permutation/Inverse Permutation Functions



Pictorial Description of the permutation function



- Purpose: Provides 10bit symbols from 4 interleaved RS(544,514) codewords on each of 32 PCS lanes
- Prerequisites: 10bit symbol alignment across lanes. Lane reorder and FEC codeword deskew across lanes is optional
- Operates on 4 RS-symbol boundaries across 32 PCS lanes
- In the transmit direction, the permutation function maps the bits received on thirty-two PCS lanes through the FEC:IS_UNITDATA_0:31.request primitives and maps them to output lanes *output_0:31*
 - Denote the index of the PCSL as p ($p=0$ to 31), where the bits for the p^{th} lane are obtained through `FEC:IS_UNITDATA_p.request`
 - Denote the index of the aligned input 10-bit block across the PCSLs as i and the bit index within block i as j ($j=0$ to 9).
 - Denote the index of the output lanes as q ($q=0$ to 31)
 - The mapping between the bit sequences on the PCSL and the *output_q* is:
 - $output_q[10i + j] = PCSL[(q + 16\lfloor i/2 \rfloor)\%32, 10i + j]$
- In the receive direction, the inverse permutation function maps the bits received on input lanes *input_0:31* to thirty-two PCS lanes and provides this data through the `FEC:IS_UNITDATA_0:31.indication` primitives. Using similar definitions as the transmit, the mapping between the bit sequences on *input_q* lanes and the PCSL is:
 - $PCSL[(q + 16\lfloor i/2 \rfloor)\%32, 10i + j] = input_q[10i + j]$

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From [kota_3dj_01a_2307](#)

Comment #422/423 (contd)

Comment #423

- Clause 184.4.1 states:

“The alignment lock function shall be identical to that specified in 172.2.5.1.”

- However, clause 172.2.5.1 requires a complete deskew of all lanes
- This deskew is not required and undesirable for low complexity modules

Comment #422

- Clause 184.4.2 states:

“The lane reorder shall be identical to that specified in 172.2.5.2.”

- However, clause 172.2.5.2 requires a complete reorder of all PCS lanes
- This complete reorder is not required and undesirable for low complexity modules

Comment #422/423: Suggest remedy

- Change 184.4.1 to the following:

184.4.1 Alignment Lock and Deskew

The alignment lock and deskew function, when implemented, shall be identical to the processes specified in 172.2.5.1 except that only a deskew to 20-bit (i.e. dual RS(544,514) symbol) boundaries across all PCS lanes is required.

- Change 184.4.2 to the following:

184.4.2 Lane reorder

The lane reorder shall be identical to that specified in 172.2.5.2 except that only a partial reorder is required such that the lanes from PCS flow 0 are present in lanes 0-15 and the lanes from PCS flow 1 are present in lanes 16-31. Complete reorder of lanes within each flow is optional.

Comment #424

- In Clause 184.4.5
 - Text says "Define parity[15:0] to be the coefficients of the computed parity polynomial" where it is implied but not stated that parity[15] corresponds to p_{15} in Equation (184-2). This should be stated precisely to eliminate any ambiguity.
- Suggested Remedy:
 - Replace this text with: "Define parity[15:0] to be the coefficients of the computed parity polynomial where parity[15] corresponds to p_{15} in Equation (184-2) and so on."

Comment #425

- In 184.4.6
 - Text implies but does not state what the bits `circo[j]` should be for `j=110` to `125`.
- Suggested Remedy:
 - Add “`encodeo[j]` is assigned to `circo[j]` for `j=110` to `125`”

Thank you!