KEYSIGHT

# Jitter Transfer Function (JTF) analysis
## Version 1.0
## Presented to IEEE P802.3dj Task Force 11/11/2024

**Associated comments: 402,146,260,315, 316**

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**Based on draft release of IEEE P802.3dj™/D1.2 Comments**

**Abstract: The absence of a JTF operation (PLL corner frequency/peaking evaluation) in recent high speed Ethernet specs has led to un-constrained PLL behaviors that result in many of the recent observations around how the same TDECQ can lead to different pre and post FEC error observations. This presentation offers real data taken from available transceiver inventories and presents a case for inclusion of JTF as a method to correct some of these aberrant measurement results.**

## Supporters/Collaborators (Version 1.0)

**Karl Muth (Broadcom)**
**Ali Ghiasi (Ghiasi Quantum)**
**Steve Sekel (Wilder Technologies)**
**Geoff Zhang (AMD)**
**Ahmad El-Chayeb (Keysight Technologies)**

## Useful Related References:

IEEE 07/15/24 Contribution: Limiting output jitter in optical PMDs: Adee Ran, Cisco
OIF 08/05/24 Contribution: Transmitter Jitter vs EECQ/TDECQ vs Post-FEC Performance : Mazzini/Tang, Cisco
IEEE 09/16 Contribution: Jitter operations (179.9.4.7) at TP1a (33dB) : Calvin et al. , Keysight Technologies
IEEE 09/16 Contribution: VEC associated with high channel loss : Calvin et al. , Keysight Technologies

D. Dalton et al., "A 12.5 Mb/s to 2.7 Gb/s continuous-rate CDR with automatic frequency acquisition and data-rate readback," *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.*, San Francisco, CA, USA, 2005, pp. 230-595 Vol. 1, doi: 10.1109/ISSCC.2005.1493953.
keywords: {Automatic frequency control;Voltage-controlled oscillators;Clocks;Voltage control;Frequency conversion;Frequency locked loops;Detectors;Filters;Phase locked loops;Computational fluid dynamics},

# Overview

This contribution demonstrates that a modules Jitter Transfer Function (JTF) of retimed optical transceiver modules can be measured through the coordinated synchronization of a BERT Pattern Generator and a suitable Clock Recovery unit. This is achieved by generating a data pattern with a fixed SJ amplitude from the BERT and injecting it into the electrical Tx input of the transceiver module (TP1a). The SJ frequency is then swept between a min and max frequency, and at each sweep increment, the CDR unit will measure the Jitter Spectrum of the transceiver's optical output and track the sinusoidal input jitter tone. The jitter transfer jitter at that frequency is the ratio of the observed amplitude, divided by the injected SJ amplitude to determine the jitter transfer at that frequency. This is repeated at each SJ sweep increment to produce a Jitter Transfer Function plot. In this experiment, we measured the JTF of QSFP-DD 800G (53.125GBd PAM4) transceiver modules and swept SJ from 15kHz to 20MHz.

The JTF is partially validated in module receiver jitter tolerance tests, however overshoot is missed in this case. The compound effects of multiple re-timers will magnify overshoot and it needs to be constrained or serious jitter amplification can arise.

Through the process of performing these TP1a->TP2 or Electro-Optic JTF studies, un-expectedly low PLL corner frequencies were observed. This PLL behavior may be complicit in TDECQ/EECQ observation errors on record.

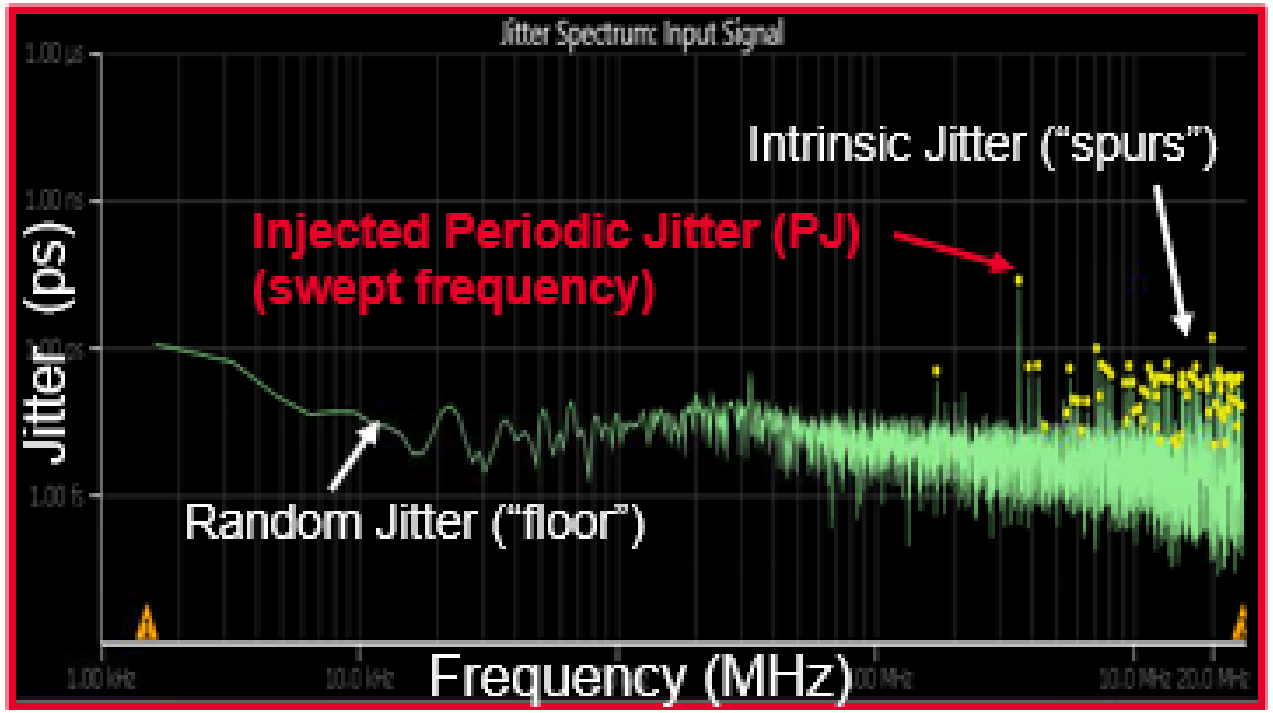
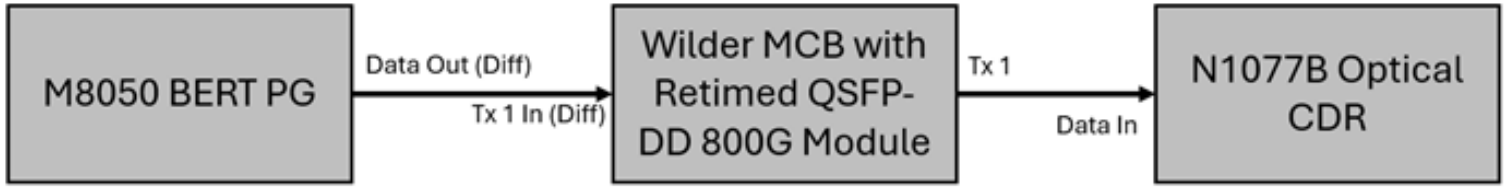



**Table 179–12—Receiver jitter tolerance parameters**

| Parameter | Case A | Case B | Case C | Case D | Case E | Case F | Units |
|---|---|---|---|---|---|---|---|
| Jitter frequency | 0.04 | 0.4 | 1.333 | 4 | 12 | 40 | MHz |
| Jitter amplitude (pk-pk) | 5 | 0.5 | 0.15 | 0.05 | 0.05 | 0.05 | UI |

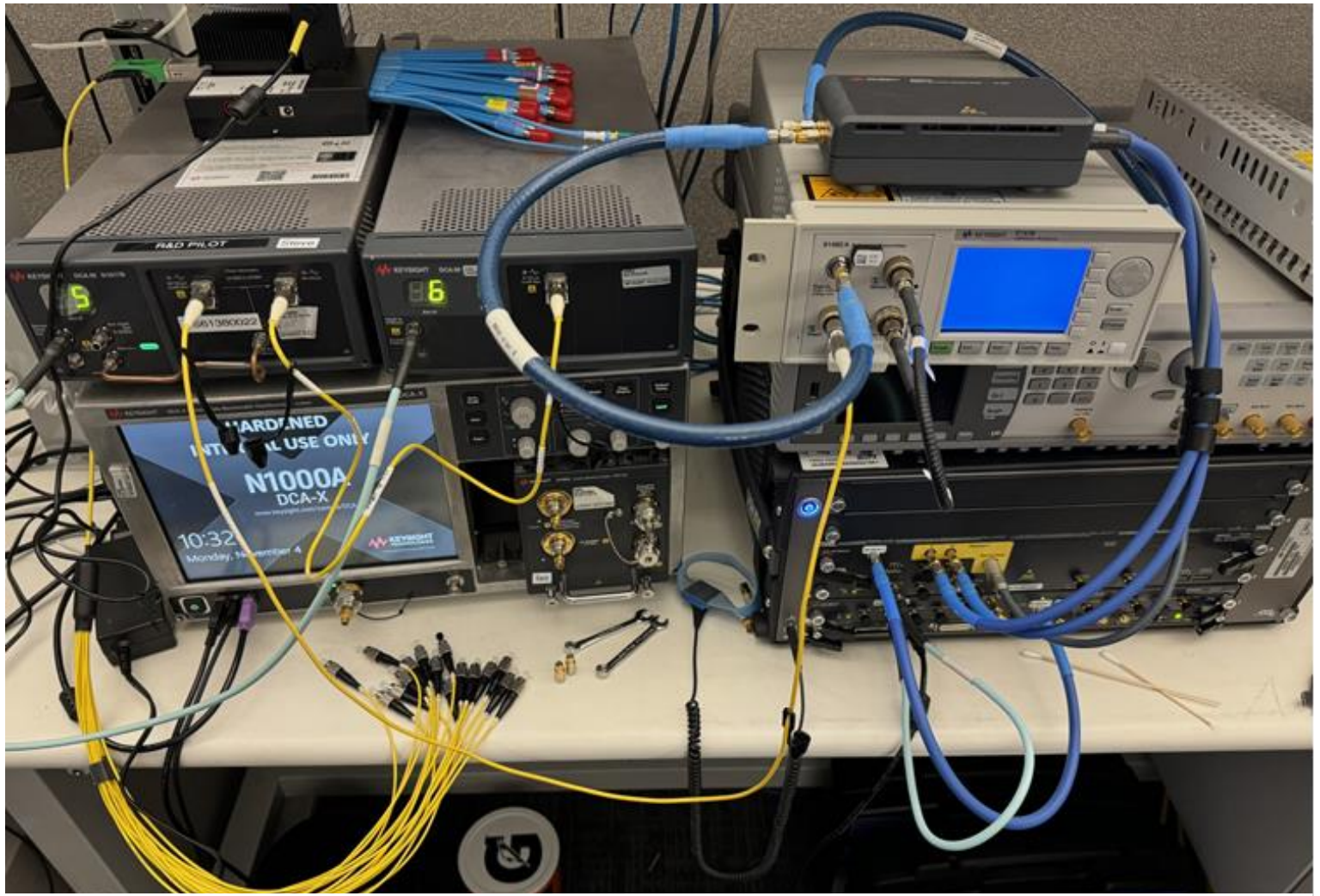
# Jitter Transfer Function setup

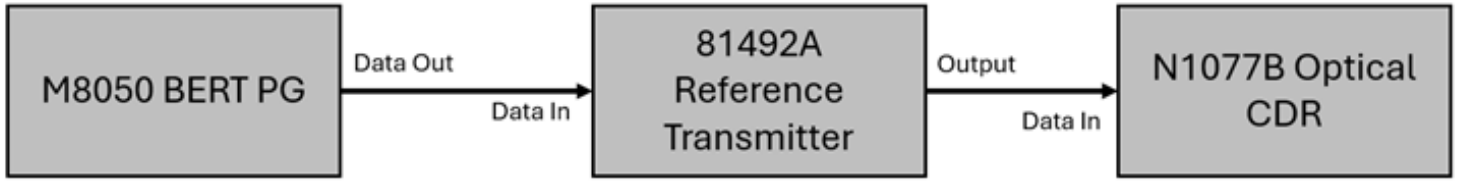
- Equipment in use for this contribution.
- BERT:  M8050 120GBd
- MCB:  QSFP-DD 800G
- CDR:  DCA-M

# Reference Transmitter Calibration

- Reference Tx E/O (Used for comparison): 81492A: 40 GHz @ 1310 nm (good up to 56GBd PAM4)

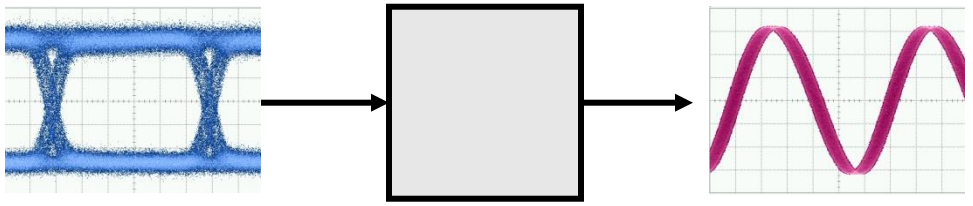


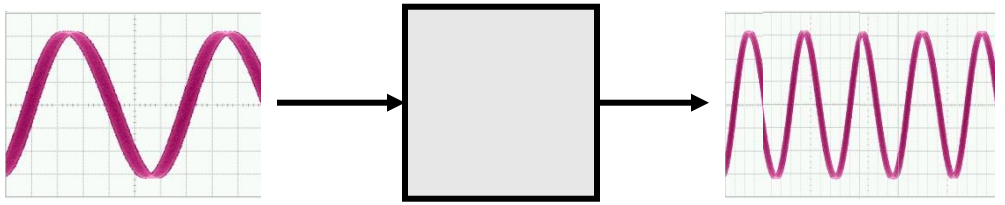
# Use Cases for PLLs

**PLLS are used in a variety of applications, and they also manage system jitter**

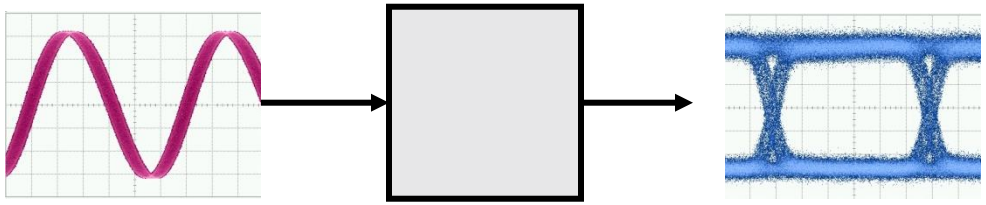
Clock recovery circuit
(data in, clock out)



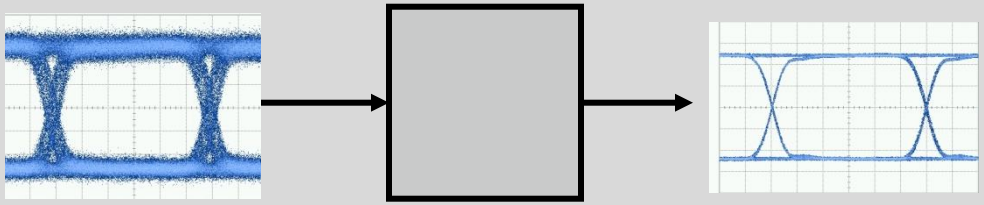
Clock multiplier circuit
(clock in, clock out)



Transmitter with ref. clock
(clock in, data out)



Repeater circuit
(data in, data out)



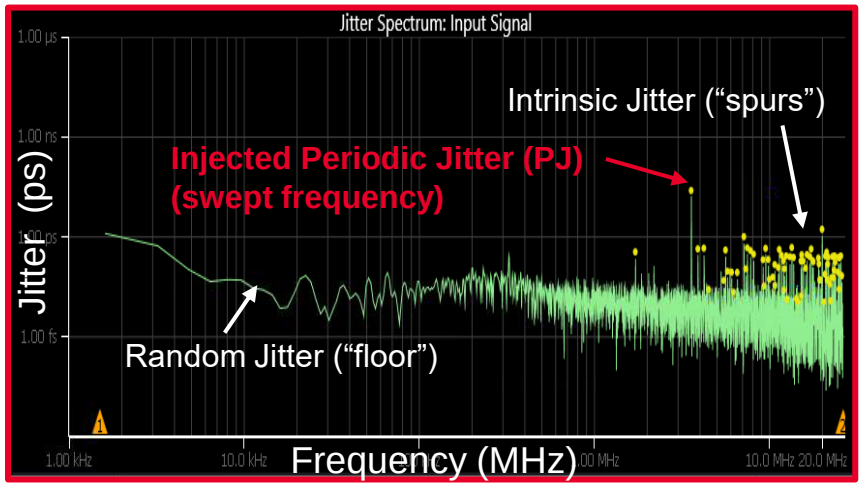
**(Today's Focus)**

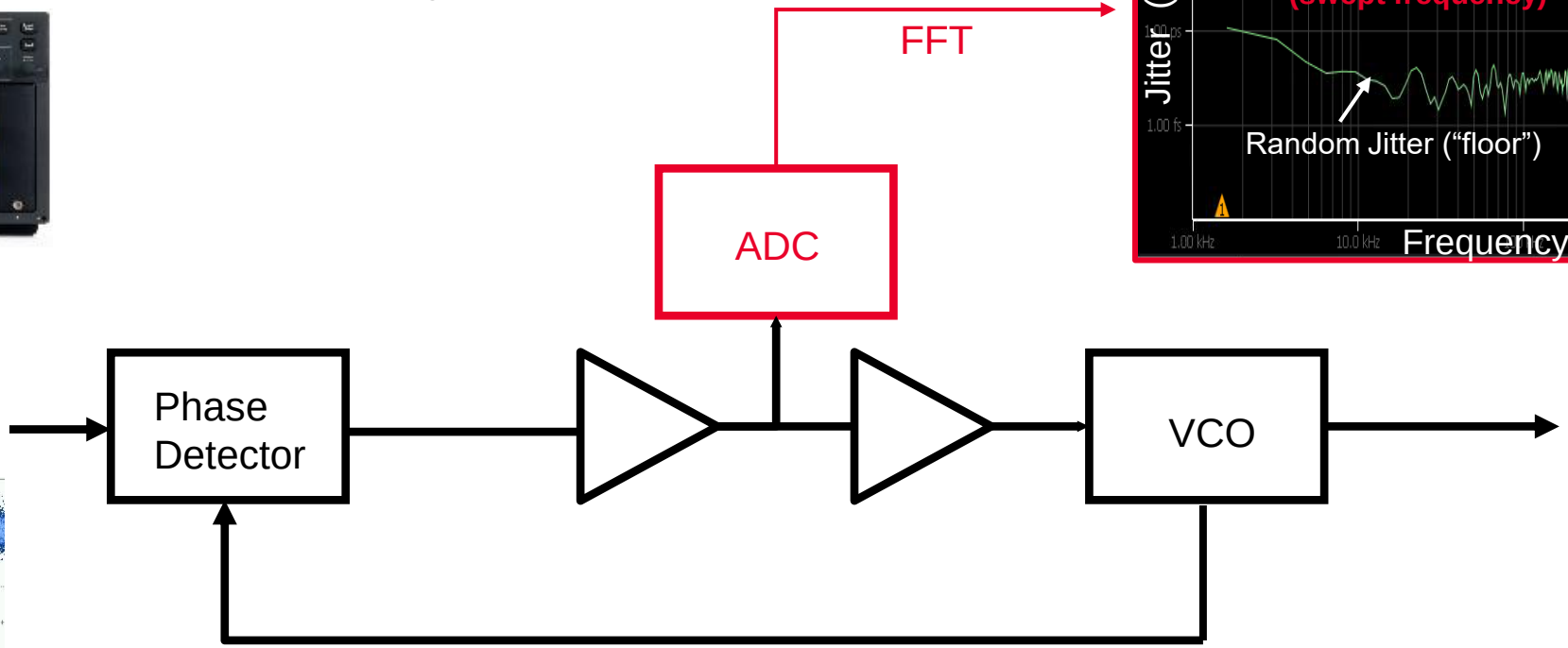
# Using a hardware clock recovery system we can observe the “jitter spectrum”

## Clock Recovery Receiver

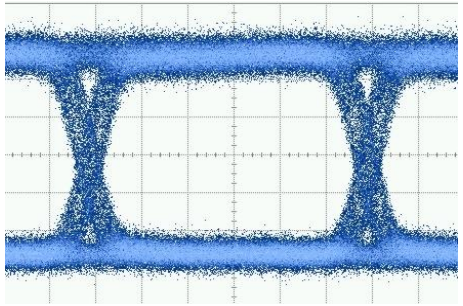
- N107X Clock Recovery with Option JSA
- N1000A+N1060A “MegaModule”

Jitter Spectrum Analysis (Option# JSA)




Data or Clock Input



No oscilloscope measurement channel is required (only CR circuit required).

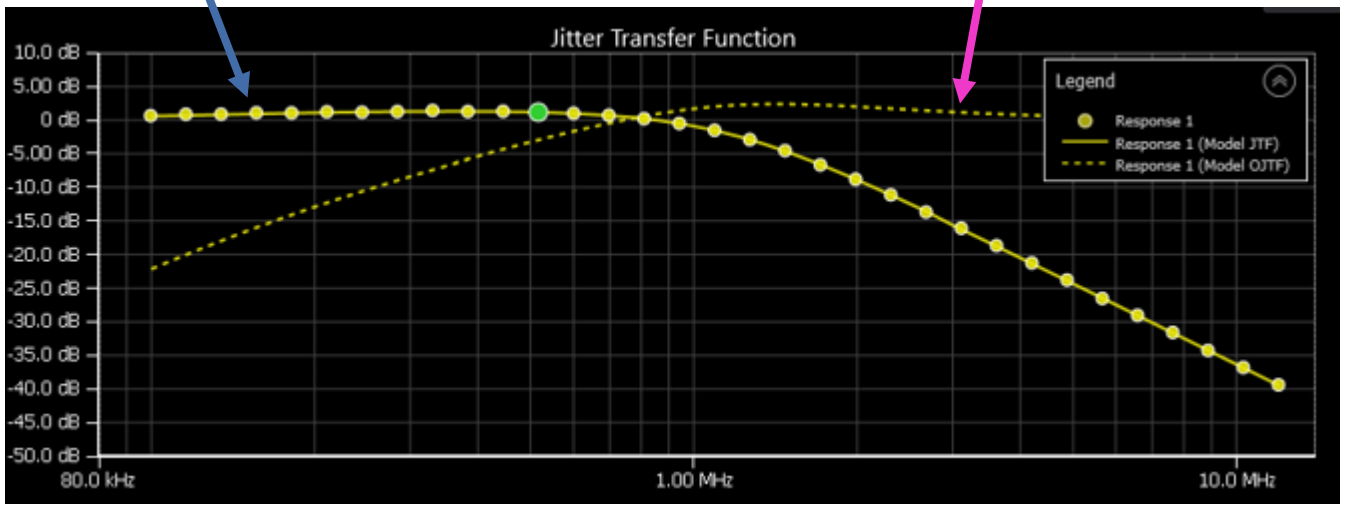
# Jitter Transfer Function (JTF)

**JTF is used to measure PLL bandwidth and peaking**

**PLL *"Jitter Transfer Function"* (JTF)**
- indicates how much of the jitter on the input signal is "transferred" to the recovered clock (output)
- low-pass filter function (LPF)
- JTF = Jitter Out / Jitter In

"Observed Jitter Transfer Function" (OJTF)
- indicates the jitter that is "observed" by the receiver (scope)
- high frequency jitter on the data stream is "transferred" to the receiver
- High-pass filter function (HPF)

$$\text{JTF} = \text{Closed loop gain}$$
$$= \frac{\phi_{out}}{\phi_{in}} = \frac{A(s)}{1+A(s)} = G(s) = |G(s)|e^{j\phi(s)}$$




$$\text{OJTF} = 1 - JTF$$
$$= 1 - G(s) = 1 - |G(s)|e^{j\phi(s)}$$

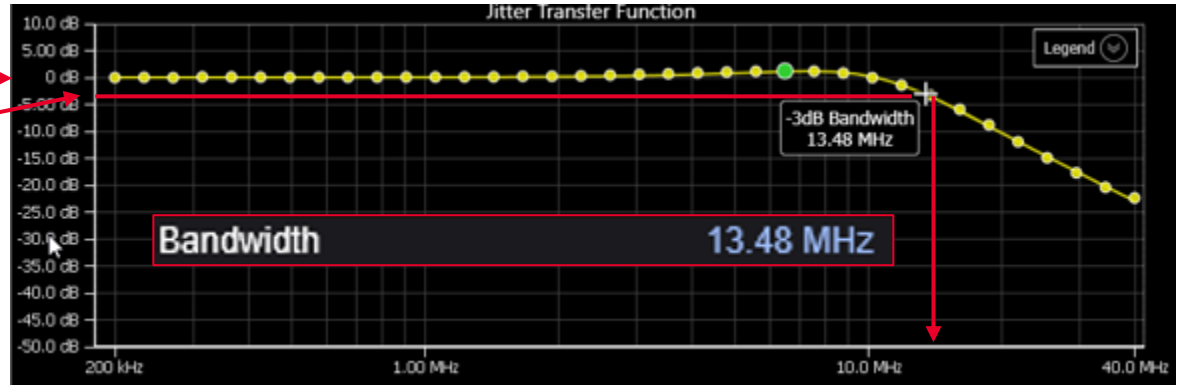
# PLL Bandwidth and Peaking

**Standards typically specify PLL bandwidth and peaking (measured on the Jitter Transfer Function)**

- PLL 3dB Bandwidth

0 dB Reference

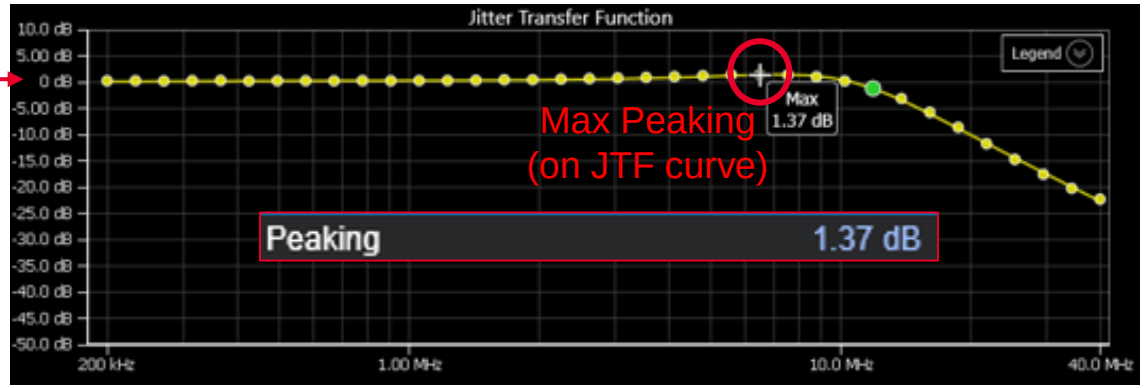
- 3 dB



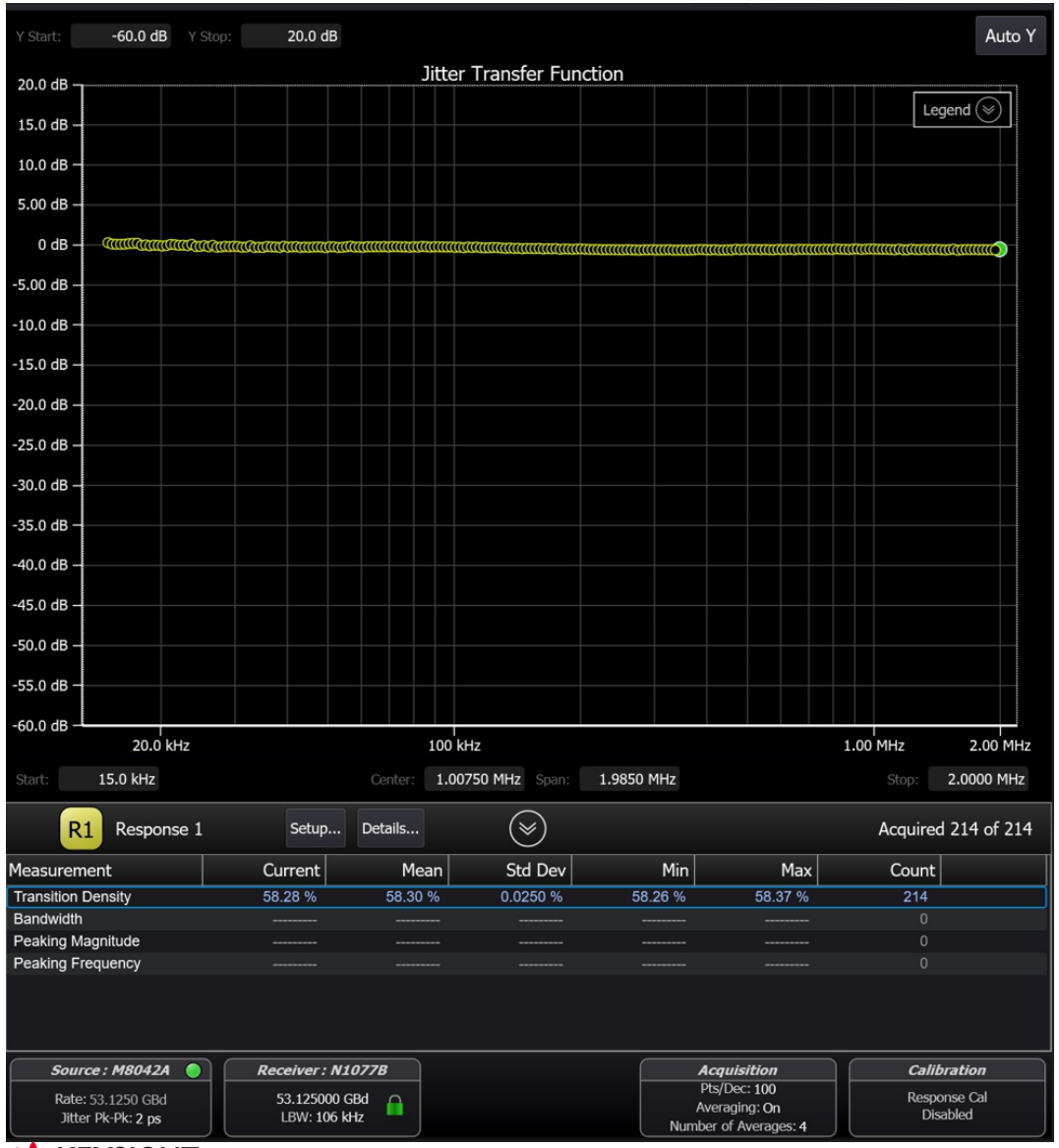

- 3 dB Bandwidth
(on JTF curve)

- PLL Peaking (max)

0 dB Reference



# JTF calibration via 81492A reference Tx (Used for comparison):




- The JTF of the Reference Transmitter setup is virtually flat. Knowing that the Reference Transmitter does not contribute to the system's JTF, this shows that the other components of the system (BERT and CDR) are not contributing to the JTF curve seen in the retimed module setup either.

# TP1a->TP2 (Electro-Optic) JTF is observed when the reference modulator is replaced with an actual 800G Transceiver.

- The JTF of a retimed module measured up to 2MHz showing the characteristic PLL response however at frequencies much lower than expected.
- PLL BW is 42Khz in this case. 2 decades lower than specs.
- Low frequency impairments are being directly transferred to the TP2 output. The “instrumentation” performing TDECQ at TP2 is performing analog equivalent 4MHz PLL operations and nominally blind to any impairments to the left of this PLL bandwidth. Discrepancies will be significant.

# Linear TP1a->TP2 JTF for comparison.


- The JTF of a linear module has no CDR/PLL (Linear only)
- As expected, the JTF is flat out to the bandwidth of the phase detector loop bandwidth limit. (~27MHz)

# Summary

- The retimed transceiver modules that were sampled in this experiment have a JTF curve with a relatively low -3dB corner frequency of approximately 40kHz.

- There are advantages to pushing the CDR's PLL to lower frequencies but doing so leads to a gap between what gets observed with instrument grade TDECQ/EECQ evaluations and what the receiver at TP5 (Post FEC BER) would be. More accurate PLL modeling in the test instrumentation will reduce the discrepancies between TEDECQ/EECQ and FLR.
- Solution: We should measure JTF and capture overshoot and bandwidth values. Ensuring these are within limit's before having confidence in TDECQ/EECQ and FLR alignment
- -or- do Optical Jitter operations.

Reviewers Comments:

"The module is using a dual loop design with a FIFO, it doesn't follow an analog PLL response"

"There is a digital clean-up PLL that filters the clock jitter"

# Thank you

# Backup: