“Full deskew” issue for Clause 177

Comment #54, #371

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Introduction

- This is a follow-up contribution of nicholl_3dj_optx_01_241017, addressing the issue when implementing “full deskew” for 800G/1.6T in Clause 177 (IMDD InnerFEC).

Background

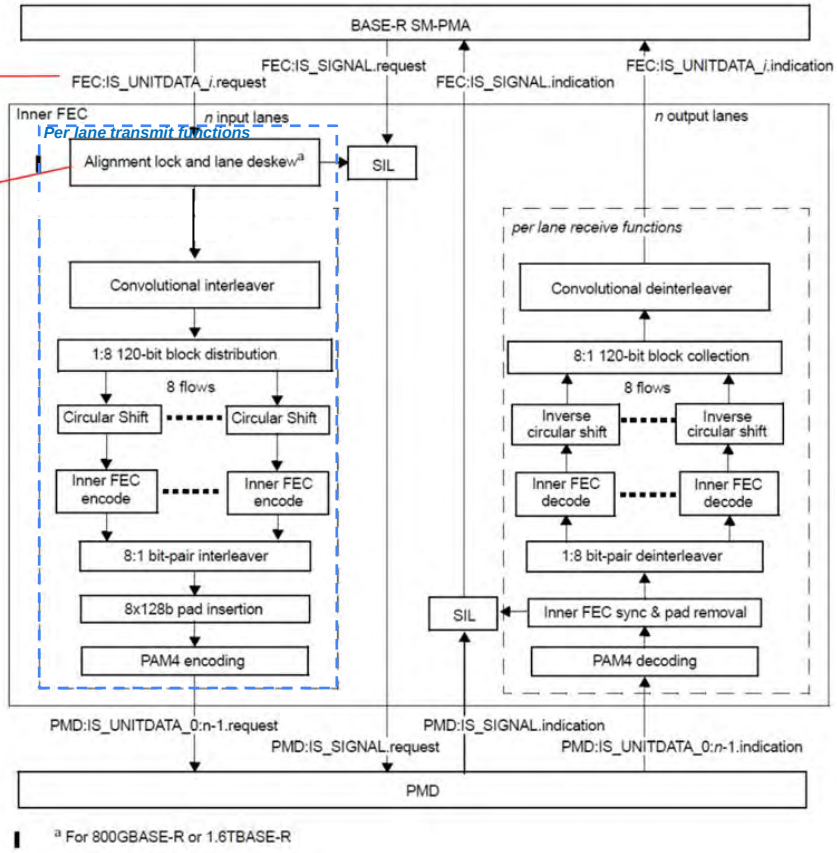
- A “deskew” function for Clause 177 was added to resolve comment #159 against D1.1, but was left intentionally vague, with editor’s note calling for more complete proposal (see next page).
- nicholl_3dj_optx_01_241017 explored ways to resolve the issue, and the first option matched original baseline better.
    - Provide a detailed description of the symbol-demuxing and symbol-muxing that is required to support the “alignment lock and deskew” function in 177.4.1 (perhaps by referencing the appropriate sections in Clause 176?)
    - Change to a PCSL based service interface for Clause 177 (similar to what was done for Clause 184).
    - Move the required PCS lane deskew function for 800G/1.6T into the SM-PMA (essentially option #3 in dudek_3dj_01_2407)
- This presentation is proposing a solution based on the first option above.

Functional Block Diagrams in D1.2

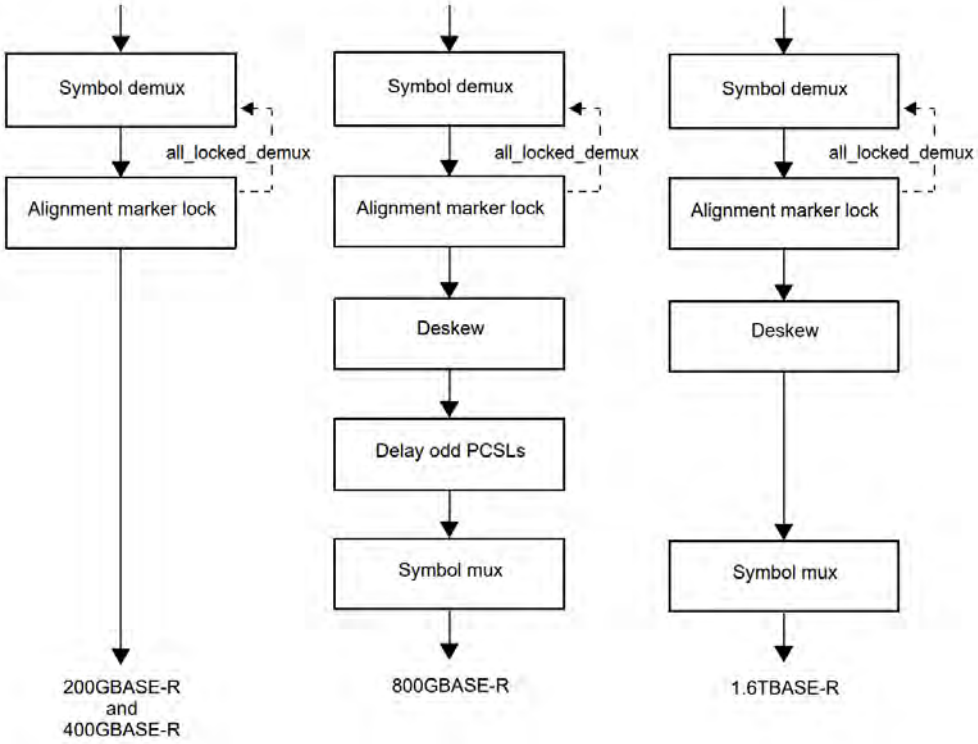
Incoming streams are 200G symbol-muxed (from the SM-PMA above)

Newly added “alignment lock and lane deskew” function (in response to comment #159).

- In order to perform the PCS lane deskew function the 200G input lanes would first have to be symbol-demuxed back to PCS lanes (essentially un-doing the symbol muxing of the SM-PMA layer above)
- Then deskew performed on the PCS lanes
- And finally, the PCS lanes symbol-muxed back to 200G lanes (repeating the function of the SM-PMA layer above).



Proposed New Functional Block Diagrams for 177.4.1



Three different processing flows are shown:

- For 200GBASE-R and 400GBASE-R, symbol-quartet boundary needs to be identified. However deskew and actual demux are not needed.
- For 800GBASE-R, alignment marker lock and deskew are needed, plus a 10-bit delay on odd lanes to remove the checkerboard pattern produced by PCS.
- For 1.6TBASE-R, alignment marker lock and deskew are needed.

Proposed Changes – New Text for 177.4.1

177.4.1 Alignment lock and deskew

In order to maintain the full 12 RS-FEC codeword interleaving depth for the convolutional interleaver, alignment marker lock and deskew is provided.

Alignment marker lock is required to determine the RS-FEC 4-symbol and codeword boundaries. In addition, 800GBASE-R and 1.6TBASE-R PHYs must also deskew PCS lanes within each input lane and recombine the PCSLs for proper operation of the convolutional interleaver.

177.4.1.1 Symbol demultiplexing

The symbol demux function is performed as defined in 176.4.3.2

177.4.1.2 Alignment marker lock

The alignment marker lock function is performed as defined in 176.4.3.3

For 200GBASE-R and 400GBASE-R, the result of the alignment marker lock function indicates the RS-FEC symbol and codeword boundaries which are needed by the convolutional interleaver. The data stream is not altered.

For 800GBASE-R and 1.6TBASE-R, in addition to indicating the RS-FEC symbol and codeword boundaries, the output of the alignment marker lock function separates an input data stream into 8 or 2 PCSLs, respectively, to be deskewed and re-combined by the symbol multiplexing process.

177.4.1.3 Deskew

For 800GBASE-R PHYs, after alignment marker lock is achieved on each of the eight PCSLs in an input stream, all inter-lane Skew within the input stream is removed by the PCS synchronization process as shown in Figure 172-5. The 800GBASE-R deskew function shall support a maximum Skew of TBD ns, and a maximum Skew Variation of TBD ns, between PCS lanes.

For 1.6TBASE-R PHYs, after alignment marker lock is achieved on each of the two PCSLs in an input stream, all inter-lane Skew is removed by the PCS synchronization process as shown in Figure 175-8. The 1.6TBASE-R deskew function shall support a maximum Skew of TBD ns, and a maximum Skew Variation of TBD ns, between PCS lanes.

177.4.1.4 Delay odd PCS lanes

This delay is performed only by the 800GBASE-R PHYs. The odd PCSLs are delayed by one RS-FEC symbol (10-bits) to remove the checkerboard pattern created by the distribution of RS-FEC symbols to PCS lanes. This is illustrated in Figure 176-4.

177.4.1.5 Symbol multiplexing

For 800GBASE-R PHYs, after aligning the PCS lanes to the alignment markers and delaying the odd PCSLs, eight PCLS are re-combined into a single data stream using the symbol-pair multiplexing function described in 176.4.2.5.1.

For 1.6TBASE-R PHYs, after aligning the PCS lanes to the alignment markers, two PCSLs are re-combined into a single data stream using the symbol-quartet multiplexing function described in 176.4.2.5.2

Thank you!