802.3dj D1.2 Comment Resolution Logic Track

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Introduction

- This slide package was assembled by the 802.3dj editorial team to provide background and detailed resolutions to aid in comment resolution.
- Specifically, these slides are for the logic track comments

Time Sync

Comments: 364, 365, 366, 367, 368, 369, 370

TimeSync
Comments 364, 365

Cl 177 SC 177.10 P306 L47 # 364

Slavick, Jeff Broadcom

Comment Type T *Comment Status* D *TimeSync*

Support of the "optional" path delay information should be presented as the first information of this section not the last.

SuggestedRemedy

Change 177.10 to be:
177.10 Path data delay (optional)
Support for the optional path data delay information is indicated by the status variables Inner_FEC_delay_ns_TX_ability, Inner_FEC_delay_subns_TX_ability, Inner_FEC_delay_ns_RX_ability, and Inner_FEC_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported, the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on the first symbol on FEC flow 0 after the 1024-bit pad insertion (see 177.4.7), corresponding to the longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:
— Inner_FEC_delay_ns_TX_max, Inner_FEC_delay_subns_TX_max
— Inner_FEC_delay_ns_TX_min, Inner_FEC_delay_subns_TX_min
— Inner_FEC_delay_ns_RX_max, Inner_FEC_delay_subns_RX_max
— Inner_FEC_delay_ns_RX_min, Inner_FEC_delay_subns_RX_min

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Pending task force discussion.
[Editor's note: CC 171, 175, 176, 177, 184, 186]

Cl 184 SC 184.8 P516 L31 # 365

Slavick, Jeff Broadcom

Comment Type T *Comment Status* D *TimeSync*

Support of the "optional" path delay information should be presented as the first information of this section not the last.

SuggestedRemedy

Change 184.8 to be:
184.8 Path data delay (optional)
Support for the optional path data delay information is indicated by the status variables Inner_FEC_delay_ns_TX_ability, Inner_FEC_delay_subns_TX_ability, Inner_FEC_delay_ns_RX_ability, and Inner_FEC_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported, the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on dspfo[3,1894] (see 184.4.10), corresponding to the longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:
— Inner_FEC_delay_ns_TX_max, Inner_FEC_delay_subns_TX_max
— Inner_FEC_delay_ns_TX_min, Inner_FEC_delay_subns_TX_min
— Inner_FEC_delay_ns_RX_max, Inner_FEC_delay_subns_RX_max
— Inner_FEC_delay_ns_RX_min, Inner_FEC_delay_subns_RX_min

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Pending task force discussion.
[Editor's note: CC 171, 175, 176, 177, 184, 186]

TimeSync
Comments 366, 367

Cl **186** *SC* **186.6.1** *P* **586** *L* **5** # **366**

Slavick, Jeff — Broadcom

Comment Type **T** *Comment Status* **D** *TimeSync*

Support of the "optional" path delay information should be presented as the first information of this section not the last.

SuggestedRemedy

Change 186.6.1 to be:
186.6.1 PCS path data delay (optional)
Support for the optional path data delay information is indicated by the PCS status variables PCS_delay_ns_TX_ability, PCS_delay_subns_TX_ability, PCS_delay_ns_RX_ability, and PCS_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported, the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on the start of the first non-fixed-stuff 257-bit GMP word of the tributary 0 multi-frame, where the start of the 800GBASE-ER1 tributary frame is also the start of a FEC frame, taking into account the maximum (transmit) and minimum (recieve) data delay through the GMP mechanism. This corresponds to the PCS's longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:
— PCS_delay_ns_TX_max, PCS_delay_subns_TX_max
— PCS_delay_ns_TX_min, PCS_delay_subns_TX_min
— PCS_delay_ns_RX_max, PCS_delay_subns_RX_max
— PCS_delay_ns_RX_min, PCS_delay_subns_RX_min

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Pending task force discussion.
[Editor's note: CC 171, 175, 176, 177, 184, 186]

Cl **186** *SC* **186.6.2** *P* **586** *L* **25** # **367**

Slavick, Jeff — Broadcom

Comment Type **T** *Comment Status* **D** *TimeSync*

Support of the "optional" path delay information should be presented as the first information of this section not the last.

SuggestedRemedy

Change 186.6.2 to be:
186.6.2 PMA path data delay (optional)
Support for the optional path data delay information is indicated by the PMA status variables PMA_delay_ns_TX_ability, PMA_delay_subns_TX_ability, PMA_delay_ns_RX_ability, and PMA_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported, the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on the first data symbol of the PMA frame S<0>, corresponding to the longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:
— PMA_delay_ns_TX_max, PMA_delay_subns_TX_max
— PMA_delay_ns_TX_min, PMA_delay_subns_TX_min
— PMA_delay_ns_RX_max, PMA_delay_subns_RX_max
— PMA_delay_ns_RX_min, PMA_delay_subns_RX_min

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Pending task force discussion.
[Editor's note: CC 171, 175, 176, 177, 184, 186]

TimeSync
Comments 368, 369, 370

Cl 171 SC 171.6b P184 L47 # 368

Slavick, Jeff Broadcom

Comment Type T *Comment Status* D *TimeSync*

Support of the "optional" path delay information should be presented as the first information of this section not the last.

SuggestedRemedy

Change 171.6b to be:
171.6b Path data delay (optional)
171.6b.1 PHY XS path data delay
Support for the optional path data delay information is indicated by the PHY XS status variables PHY_XS_delay_ns_TX_ability, PHY_XS_delay_subns_TX_ability, PHY_XS_delay_ns_RX_ability, and PHY_XS_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported and the PCS_timesync_multilane_ability variableis true (see 90.7.1), the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) is the start of the set of interleaved RS-FEC codewords, corresponding to the longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:
— PHY_XS_delay_ns_TX_max, PHY_XS_delay_subns_TX_max
— PHY_XS_delay_ns_TX_min, PHY_XS_delay_subns_TX_min
— PHY_XS_delay_ns_RX_max, PHY_XS_delay_subns_RX_max
— PHY_XS_delay_ns_RX_min, PHY_XS_delay_subns_RX_min

171.6b.2 DTE XS path data delay
Support for the optional path data delay information is indicated by the DTE XS status variables DTE_XS_delay_ns_TX_ability, DTE_XS_delay_subns_TX_ability, DTE_XS_delay_ns_RX_ability, and DTE_XS_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported and the PCS_timesync_multilane_ability variableis true (see 90.7.1), the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) is the start of the set of interleaved RS-FEC codewords, corresponding to the longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:
— DTE_XS_delay_ns_TX_max, DTE_XS_delay_subns_TX_max
— DTE_XS_delay_ns_TX_min, DTE_XS_delay_subns_TX_min
— DTE_XS_delay_ns_RX_max, DTE_XS_delay_subns_RX_max
— DTE_XS_delay_ns_RX_min, DTE_XS_delay_subns_RX_min

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Pending task force discussion.

Cl 175 SC 175.6 P244 L10 # 369

Slavick, Jeff Broadcom

Comment Type T *Comment Status* D *TimeSync*

Support of the "optional" path delay information should be presented as the first information of this section not the last.

SuggestedRemedy

Change 175.6 to be:
175.6 Path data delay (optional)
Support for the optional path data delay information is indicated by the status variables PCS_delay_ns_TX_ability, PCS_delay_subns_TX_ability, PCS_delay_ns_RX_ability, and PCS_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported and the PCS_timesync_multilane_ability variableis true (see 90.7.1), the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) is at the start of the set of four interleaved RS-FEC codewords, longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:
— PCS_delay_ns_TX_max, PCS_delay_subns_TX_max
— PCS_delay_ns_TX_min, PCS_delay_subns_TX_min
— PCS_delay_ns_RX_max, PCS_delay_subns_RX_max
— PCS_delay_ns_RX_min, PCS_delay_subns_RX_min

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Pending task force discussion.
[Editor's note: CC 171, 175, 176, 177, 184, 186]

Cl 176 SC 176.10 P281 L60 # 370

Slavick, Jeff Broadcom

Comment Type T *Comment Status* D *TimeSync*

Support of the "optional" path delay information should be presented as the first information of this section not the last.

SuggestedRemedy

Change 176.10 to be:
176.10 Path data delay (optional)
Support for the optional path data delay information is indicated by the PMA status variables PMA_delay_ns_TX_ability, PMA_delay_subns_TX_ability, PMA_delay_ns_RX_ability, and PMA_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported, the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on an odd PCS lane, corresponding to the longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:
— PMA_delay_ns_TX_max, PMA_delay_subns_TX_max
— PMA_delay_ns_TX_min, PMA_delay_subns_TX_min
— PMA_delay_ns_RX_max, PMA_delay_subns_RX_max
— PMA_delay_ns_RX_min, PMA_delay_subns_RX_min

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
Pending task force discussion.
[Editor's note: CC 171, 175, 176, 177, 184, 186]

TimeSync
Subclause 177.10

Comment 364 - Suggest Remedy

177.10 Path data delay for time synchronization

When the Inner FEC is part of a Physical Layer that supports time synchronization (see Clause 90), transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on the first symbol on FEC flow 0 after the 1024-bit pad insertion, corresponding to the longest delay for transmit and the shortest delay for receive.

Four separate delays are reported in the following eight path data delay status variables:

— Inner_FEC_delay_ns_TX_max, Inner_FEC_delay_subns_TX_max
— Inner_FEC_delay_ns_TX_min, Inner_FEC_delay_subns_TX_min
— Inner_FEC_delay_ns_RX_max, Inner_FEC_delay_subns_RX_max
— Inner_FEC_delay_ns_RX_min, Inner_FEC_delay_subns_RX_min

Support for the optional path data delay information is indicated by the status variables Inner_FEC_delay_ns_TX_ability, Inner_FEC_delay_subns_TX_ability, Inner_FEC_delay_ns_RX_ability, and Inner_FEC_delay_subns_RX_ability. See 90.6 for more information

Change 177.10 to be:

177.10 Path data delay (optional)

Support for the optional path data delay information is indicated by the status variables Inner_FEC_delay_ns_TX_ability, Inner_FEC_delay_subns_TX_ability, Inner_FEC_delay_ns_RX_ability, and Inner_FEC_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported, the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on the first symbol on FEC flow 0 after the 1024-bit pad insertion (see 177.4.7) corresponding to the longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:
— Inner_FEC_delay_ns_TX_max, Inner_FEC_delay_subns_TX_max
— Inner_FEC_delay_ns_TX_min, Inner_FEC_delay_subns_TX_min
— Inner_FEC_delay_ns_RX_max, Inner_FEC_delay_subns_RX_max
— Inner_FEC_delay_ns_RX_min, Inner_FEC_delay_subns_RX_min

Suggested remedy:

1. Change to the subclause title - emphasis on *optional*
2. Move the last paragraph to the beginning and add one sentence with reference to Clause 90.
3. Next paragraph adds cross-references to 177.4.7 and 90.7

Comment # 364
Suggested Changes to 177.10

177.10 Path data delay for time synchronization

The InnerFEC sublayer optionally provides path data delay information for time synchronization (see Clause 90).

InnerFEC path data delays are available when the variables Inner_FEC_delay_ns_TX_ability, Inner_FEC_delay_subns_TX_ability, Inner_FEC_delay_ns_RX_ability, and Inner_FEC_delay_subns_RX_ability are asserted as defined in 45.2.1.175.

The transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on the first symbol on FEC flow 0 after the 1024-bit pad insertion (see 177.4.7), corresponding to the longest delay for transmit and the shortest delay for receive (see 90.7)

Four separate delays are reported in the following eight path data delay status variables:

— Inner_FEC_delay_ns_TX_max and Inner_FEC_delay_subns_TX_max
— Inner_FEC_delay_ns_TX_min and Inner_FEC_delay_subns_TX_min
— Inner_FEC_delay_ns_RX_max and Inner_FEC_delay_subns_RX_max
— Inner_FEC_delay_ns_RX_min and Inner_FEC_delay_subns_RX_min

Suggested changes:

- Keep title the same
  - Path data delay is only used for time sync.
- Add an introductory sentence
  - Emphasize time sync support is optional, and link to CL 90.
- Move last paragraph with ability bits up to beginning of subclause and add link to the the definition of ability bits.
- Clean up some wording and add informative cross-refs (from suggested remedy and new ones)

Comment # 365
Suggested Changes to 184.8

184.8 Path data delay for time synchronization

The InnerFEC sublayer optionally provides path data delay information for time synchronization (see Clause 90).

InnerFEC path data delays are available when the variables Inner_FEC_delay_ns_TX_ability, Inner_FEC_delay_subns_TX_ability, Inner_FEC_delay_ns_RX_ability, and Inner_FEC_delay_subns_RX_ability are asserted as defined in 45.2.1.175.

The transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on dspfo[3,1894] (see 184.4.10), corresponding to the longest delay for transmit and the shortest delay for receive (see 90.7).

Four separate delays are reported in the following eight path data delay status variables:

— Inner_FEC_delay_ns_TX_max and Inner_FEC_delay_subns_TX_max
— Inner_FEC_delay_ns_TX_min and Inner_FEC_delay_subns_TX_min
— Inner_FEC_delay_ns_RX_max and Inner_FEC_delay_subns_RX_max
— Inner_FEC_delay_ns_RX_min and Inner_FEC_delay_subns_RX_min

Comment # 366
Suggested Changes to 186.6.1

186.6.1 PCS path data delay for time synchronization

The PCS sublayer optionally provides path data delay information for time synchronization (see Clause 90).

PCS path data delays are available when the variables PCS_delay_ns_TX_ability, PCS_delay_subns_TX_ability, PCS_delay_ns_RX_ability, and PCS_delay_subns_RX_ability are asserted as defined in 45.2.3.67.

The transmit and receive path data delay values are reported as if the data delay measurement point (DDMP) occurs on the start of the first non-fixed-stuff 257-bit GMP word of the tributary 0 multi-frame, where the start of the 800GBASEER1 tributary frame is also the start of a FEC frame, taking into account the maximum (transmit) and minimum (receive) data delay through the GMP mechanism. This corresponds to the longest delay through the transmit PCS and shortest delay through the receive PCS (see 90.7).

Four separate delays are reported in the following eight path data delay status variables:

— PCS_delay_ns_TX_max and PCS_delay_subns_TX_max
— PCS_delay_ns_TX_min and PCS_delay_subns_TX_min
— PCS_delay_ns_RX_max and PCS_delay_subns_RX_max
— PCS_delay_ns_RX_min and PCS_delay_subns_RX_min

Comment # 367
Suggested Changes to 186.6.2

186.6.2 PMA path data delay for time synchronization

The PMA sublayer optionally provides path data delay information for time synchronization (see Clause 90).

PMA path data delays are available when the variables PMA_delay_ns_TX_ability, PMA_delay_subns_TX_ability, PMA_delay_ns_RX_ability, and PMA_delay_subns_RX_ability are asserted as defined in 45.2.1.175.

The transmit and receive path data delay values are reported as if the DDMP occurs on the first data symbol of the PMA frame S<0>, corresponding to the maximum delay for transmit and minimum delay for receive (See 90.7).

Four separate delays are reported in the following eight path data delay status variables:

— PMA_delay_ns_TX_max and PMA_delay_subns_TX_max
— PMA_delay_ns_TX_min and PMA_delay_subns_TX_min
— PMA_delay_ns_RX_max and PMA_delay_subns_RX_max
— PMA_delay_ns_RX_min and PMA_delay_subns_RX_min

Comment # 368
Suggested Changes to 171.6b

171.6b Path data delay for time synchronization

The PHY XS sublayer optionally provides path data delay information for time synchronization (see Clause 90).

PHY XS path data delays are available when the variables PHY_XS_delay_ns_TX_ability, PHY_XS_delay_subns_TX_ability, PHY_XS_delay_ns_RX_ability, and PHY_XS_delay_subns_RX_ability are asserted as defined in 45.2.4.28.

The PHY XS transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) is at the start of the set of interleaved RS-FEC codewords (see 90.7).

Four separate delays are reported in the following eight path data delay status variables:

— PHY_XS_delay_ns_TX_max and PHY_XS_delay_subns_TX_max
— PHY_XS_delay_ns_TX_min and PHY_XS_delay_subns_TX_min
— PHY_XS_delay_ns_RX_max and PHY_XS_delay_subns_RX_max
— PHY_XS_delay_ns_RX_min and PHY_XS_delay_subns_RX_min

Comment # 368
Suggested Changes to 171.6b (continued)

The DTE XS sublayer optionally provides path data delay information for time synchronization (see Clause 90).

DTE XS path data delays are available when the variables DTE_XS_delay_ns_TX_ability, DTE_XS_delay_subns_TX_ability, DTE_XS_delay_ns_RX_ability, and DTE_XS_delay_subns_RX_ability are asserted as defined in 45.2.5.28.

The DTE XS transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) is at the start of the set of interleaved RS-FEC codewords (see 90.7).

Four separate delays are reported in the following eight path data delay status variables:

— DTE_XS_delay_ns_TX_max and DTE_XS_delay_subns_TX_max
— DTE_XS_delay_ns_TX_min and DTE_XS_delay_subns_TX_min
— DTE_XS_delay_ns_RX_max and DTE_XS_delay_subns_RX_max
— DTE_XS_delay_ns_RX_min and DTE_XS_delay_subns_RX_min

Comment # 369
Suggested Changes to 175.6

175.6 Path data delay for time synchronization

The PCS sublayer optionally provides path data delay information for time synchronization (see Clause 90).

PCS path data delays are available when the variables PCS_delay_ns_TX_ability, PCS_delay_subns_TX_ability, PCS_delay_ns_RX_ability, and PCS_delay_subns_RX_ability are asserted as defined in 45.2.3.67.

The transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) is at the start of the set of four interleaved RS-FEC codewords (see 90.7), and the PCS_timesync_mutlilane_ability variable is asserted.

Four separate delays are reported in the following eight path data delay status variables:

— PCS_delay_ns_TX_max and PCS_delay_subns_TX_max
— PCS_delay_ns_TX_min and PCS_delay_subns_TX_min
— PCS_delay_ns_RX_max and PCS_delay_subns_RX_max
— PCS_delay_ns_RX_min and PCS_delay_subns_RX_min

Comment # 370
Suggested Changes to 176.10

176.10 Path data delay for time synchronization

The SM-PMA sublayer optionally provides path data delay information for time synchronization (see Clause 90).

SM-PMA path data delays are available when the variables PMA_delay_ns_TX_ability, PMA_delay_subns_TX_ability, PMA_delay_ns_RX_ability, and PMA_delay_subns_RX_ability are asserted as defined in 45.2.1.175.

The transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on an odd PCS lane (see 90.7).

Four separate delays are reported in the following eight path data delay status variables:

— PMA_delay_ns_TX_max and PMA_delay_subns_TX_max
— PMA_delay_ns_TX_min and PMA_delay_subns_TX_min
— PMA_delay_ns_RX_max and PMA_delay_subns_RX_max
— PMA_delay_ns_RX_min and PMA_delay_subns_RX_min

PTP Accuracy

Comments: 12, 167, 382

Enhanced PTP accuracy AML field Comment 12

Cl 186 SC 186.2.3.6.10 P 556 L 26 # 12

Bruckman, Leon Nvidia

Comment Type TR *Comment Status* X

Pointers like the AML are prone to wrong interpretation

SuggestedRemedy

Add an example of the AML value. It can either be a figure, or just text that says: "If the removed AM was located immediately before the Nth 66B block in the GMP payload, then the value of the AML will be 0xXX"

Proposed Response *Response Status* O

Editor's view:

The example text in the suggested remedy is misunderstanding the intended behavior. The intent is that the PCS maintains a counter that counts 66b blocks between AMs. The TAML signal (indicating where AMs were) resets that counter. The AML overhead in each GMP frame contains the value of the counter corresponding to the first non-stuff block in the payload area of the frame (indicating how far it is from the last AM/until the next AM), as the highlighted text from 186.2.3.6.10 says:

… the TAML signal in the PCS service interface indicates that 800GBASE-R PCS alignment markers were removed by an adjacent PHY 800G XS sublayer immediately before the MII transaction for which TAML is asserted. The 800GBASE-ER1 PCS uses this indication to reset a counter of 66B blocks between consecutive sets of 800GBASE-R PCS alignment markers, with the first 66B block after the 800GBASE-R PCS alignment markers in flow 0 being block 1. The value of this counter corresponding to the first 66B block that is mapped into the payload area of the 800GBASE-ER1 tributary multi-frame is encoded into the AML field.

Enhanced PTP accuracy AML field
Comment 12 - Proposal

Editor's proposal:

Add a sentence with an example to the end of the text in 186.2.3.6.10, as shown in the highlighted text:

… the TAML signal in the PCS service interface indicates that 800GBASE-R PCS alignment markers were removed by an adjacent PHY 800G XS sublayer immediately before the MII transaction for which TAML is asserted. The 800GBASE-ER1 PCS uses this indication to reset a counter of 66B blocks between consecutive sets of 800GBASE-R PCS alignment markers, with the first 66B block after the 800GBASE-R PCS alignment markers in flow 0 being block 1. The value of this counter corresponding to the first 66B block that is mapped into the payload area of the 800GBASE-ER1 tributary multi-frame is encoded into the AML field. For example, if the first non-stuff block in the GMP frame happens to be the tenth block after AMs were removed, the AML field would contain the value 10.

Delay constraints

Comment: #165

Delay Constraints for Inner FEC

Inner FEC delay estimation:

- Convolutional interleaver:

Rate	d (RS symbol)	P	Q	Depth	Latency ns
1.6TE	4	3	24	12x RS	27.1
800GE	4	3	48	12x RS	54.2
400GE	4*	3	96	12x RS	108.4
200GE	4*	3	192	12x RS	216.8

ieee802.org/3/dj/public/23_07/he_3dj_01_2307.pdf

- SD decoder: 51.2ns as a conservative estimation.
- Misc.: 5ns
  - 120-b distribution, circular shift, 8:1 interleaving…

- Adding them together:

Rate	Est. Delay	In pause_quanta, rounding up	Proposed value (pause_quanta)
1.6TE	83.3	261	270
800GE	110.4	173	190
400GE	164.6	129	150
200GE	273	107	130

Proposed changes to draft

Remove the editor's note

Update TBDs in Table 177-5 as below:

177.8 Delay constraints

The maximum delay contributed by the Inner FEC (sum of transmit and receive delays at one end of the link) shall be no more than the values provided in Table 177–5. A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 169.4 and its references.

Editor's Note (to be removed prior to D2.0 or if updated with proposed values):
Need proposal for delay constraints.

Table 177–5—Delay constraints

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
200GBASE-R Inner FEC	TBD	TBD	TBD
400GBASE-R Inner FEC	TBD	TBD	TBD
800GBASE-R Inner FEC	TBD	TBD	TBD
1.6TBASE-R Inner FEC	TBD	TBD	TBD

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Maximum (ns)
200GBASE-R Inner FEC	66560	130	332.8
400GBASE-R Inner FEC	76800	150	192
800GBASE-R Inner FEC	97280	190	121.6
1.6TBASE-R Inner FEC	138240	270	86.4

Inner FEC sync

Comments: #363, #389

Frame Sequence Checking: Optional or Mandatory? Comments #363

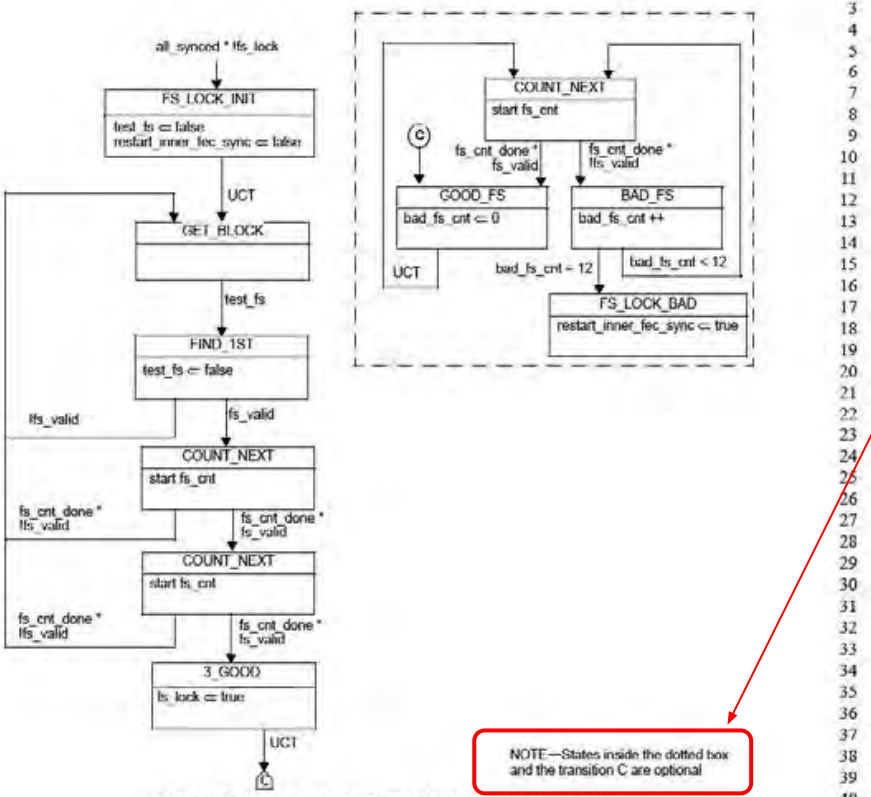

Figure 177–10—Inner FEC pad detection state diagram

The dotted box continuously checks for valid frame sequence payloads at the correct location after the initial fs_lock is set in state 3_GOOD.

Why optional? Why not make it mandatory?

Editors recommendation: ACCEPT IN PRINCIPLE.
Pending task force discussion.

CL 177 Inner FEC state diagram restart condition reset Comments #389

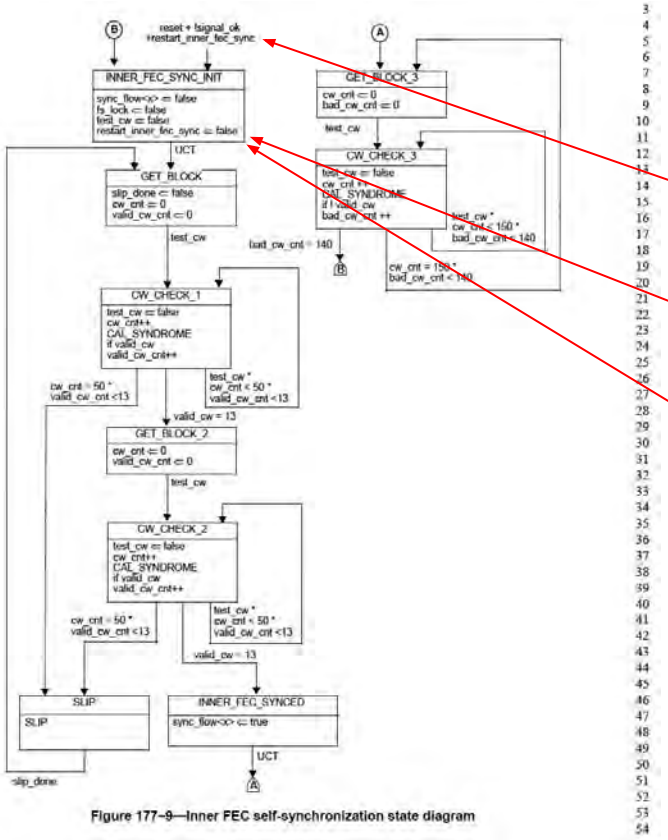

Figure 177–9—Inner FEC self-synchronization state diagram

restart_inner_fec_sync is set true in FS_LOCK_BAD state

It forces Fig. 177-9 to restart. Note there are 8 of these, one per inner fec flow.

restart_inner_fec_sync is reset in two (actually 9) places.

Suggested remedy is to remove the reset (set to false) in INNER_FEC_SYNC_INIT.

Reset of fs_lock in INNER_FEC_SYNC_INIT should cause Fig.177-10 go to FS_LOCK_INIT, but only after all 8 flows again achieve sync and all_synced is true. However, this won't happen immediately and Fig. 177-9 gets stuck in INNER_FEC_SYNC_INIT state.

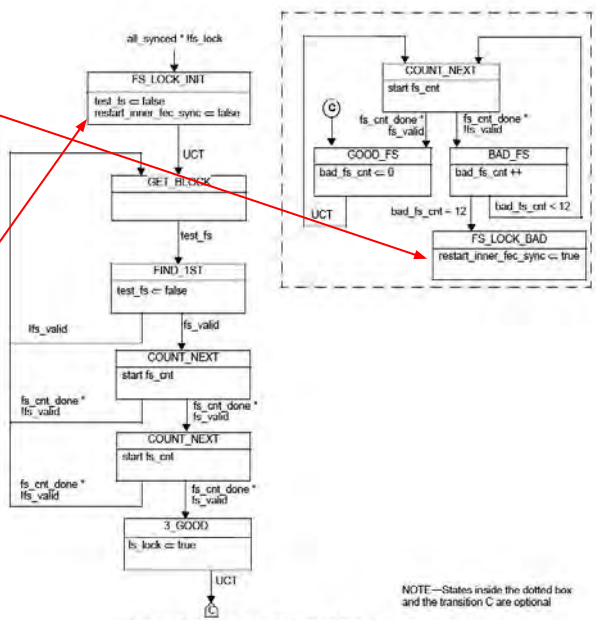

Figure 177–10—Inner FEC pad detection state diagram

Editors recommendation: ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license

CL 177 Inner FEC state machine interaction Comments #389 - full fix.

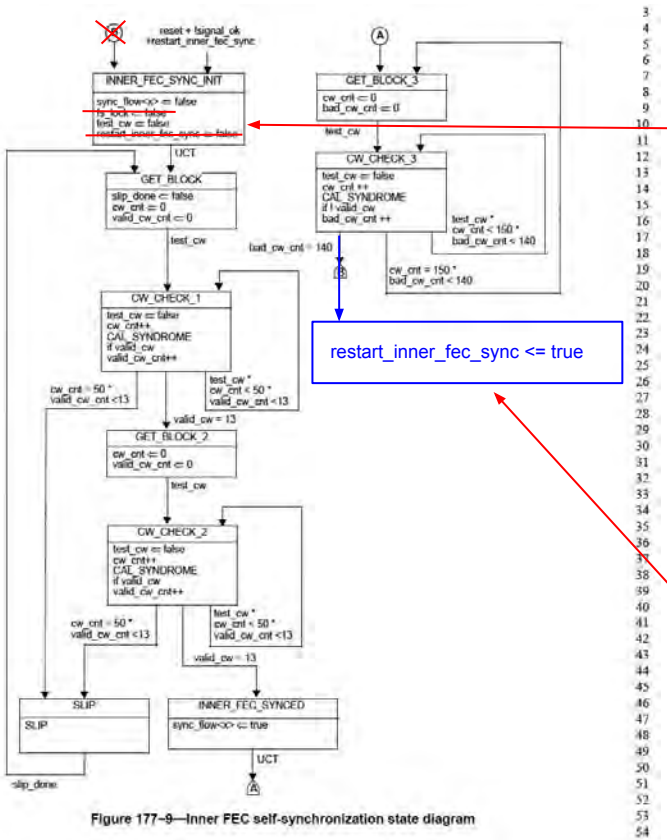

Figure 177–9—Inner FEC self-synchronization state diagram

Remove restart_inner_fec_sync and fs_lock from INNER_FEC_SYNC_INIT state

Change entry to FS_LOCK_INIT from (all_synced *!fs_lock) to: Reset + !signal_ok + restart_inner_fec_sync

In FS_LOCK_INIT, add: "fs_lock <= false"

Change transition out of FS_LOCK_INIT from UCT to: "all_synced".

Add a new state out of CW_CHECK_3 to set: restart_inner_fec_sync <= true to restart both state diagrams.

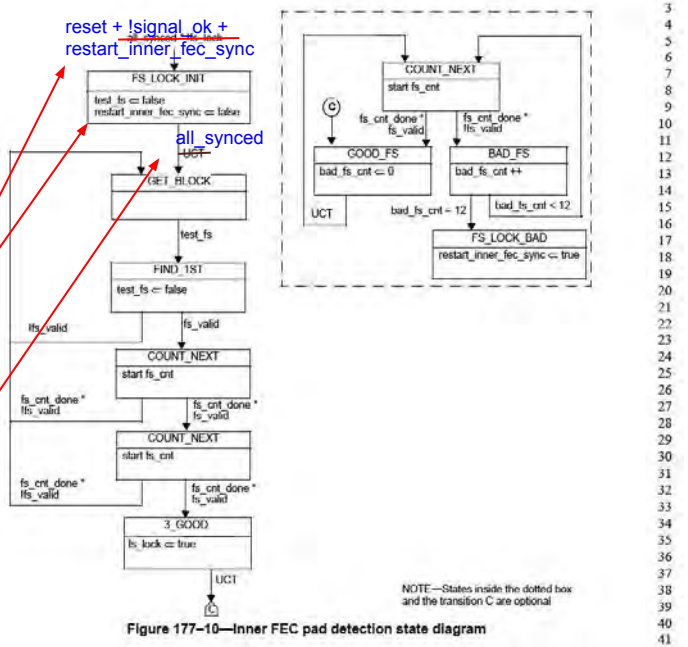

Figure 177–10—Inner FEC pad detection state diagram

800GBASE-ER1 PCS/PMA

Comments: #10, 17

Alignment Mechanism field Comment 10

Cl **186** *SC* **186.2.3.5.1** *P* **553** *L* **31** # **10**

Bruckman, Leon Nvidia

Comment Type **TR** *Comment Status* **X**

The acronym AM is ovreloaded and creates confusion

SuggestedRemedy

Change the name of the AM field to: GMP Alignment Marker, abreviated as GAM

Proposed Response *Response Status* **O**

Editor's proposal:
The PCS frame format is reusing a frame structure that is defined in Recommendation ITU-T G.709.1 and reused in OIF 800ZR, both of which call the field "AM", which G.709.1 defines as "Alignment Mechanism" to differentiate it from "Alignment Marker" as 802.3 uses. For consistency with the base documents, it is better to retain the field name as is. However, it would be beneficial to spell out the name of the field in the text:

In 186.2.3.5: Change the title to "Alignment Mechanism and Pad", change the text to "This clause specifies the Alignment Mechanism (AM) and Pad fields…"

In 186.2.3.5.1: "The Alignment Mechanism (AM) field is used to provide…"

Note that in 186.2.3.6.10, where Ethernet AMs are mentioned, the existing text uses "800GBASE-R PCS alignment markers" to refer to the actual Ethernet AMs to avoid ambiguity.

Handling overhead when the FEC frame CRC check fails Comment 17

Cl 186 SC 186.2.4.4 P 561 L 19 # 17

Bruckman, Leon Nvidia

Comment Type TR *Comment Status* X

it is not clear how shall the OH fields be handled if CRC-32 erros are detected in their row

SuggestedRemedy

Add specification that OH fields shall be ingored if a CRC32 error was detected in their row.

Proposed Response *Response Status* O

Editor's view:
The intended behavior is indeed not clear, and the existing text stating that all payload blocks in the GMP frame should be replaced with /E/ blocks is not correct. The GMP overhead has to be processed whether or not there are CRC32 errors, since that is what differentiates stuff blocks from payload blocks. The GMP encoding of the GMP overhead takes advantage of the fact that the number of data blocks changes in small increments to provide additional resilience against transmission errors. The intent of the CRC-32 in the OFEC frame is to enable error marking of the Ethernet data, not the entire GMP frame.

Proposal: Revise 186.2.4.4 to state that the blocks that correspond to payload blocks in the GMP frame are replaced with /E/ blocks when the CRC32 is failed.