

# Addressing Clause 184 comments against D1.3 for 800GBASE-LR1

(Support contribution for Comments #472, 473)

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# Comment #472

Cl 184

SC 184.4.1

P 519

L 5

# 472

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*Comment Type* **TR**

*Comment Status* **X**

Lane deskew has been changed from the adopted baseline requirement of RS(544,514) symbol alignment to a full RS(544,514) codeword alignment without any supporting data. Symbol alignment (instead of codeword alignment) for 800GBASE-LR1 has been studied in the past and determined to have a burst tolerance which exceeds the 400ZR burst tolerance of 1024b which is considered acceptable for this interface. Specifically, lane alignment lock in D1.3 refers to 172.2.5.1 for deskew. However, 172.2.5.1 specifies a complete de-skew of all the PCS lanes. The permutation function only requires a partial deskew of 20-bits (i.e. dual 10-bit RS symbol boundaries). A full deskew places an unreasonable burden on implementations which are targeted at low-power applications

*Suggested Remedy*

Change the text to reflect the intention from the baseline adopted at Berlin meeting and ensure consistency with the 20-bit alignment adopted in the OIF 800LR IA. Supporting presentation to be provided.

*Proposed Response*

*Response Status* **O**

# Comment #472: Problem statement

- Clause 184.4.1 states:

“The alignment lock function shall be identical to that specified in 172.2.5.1.”

- However, clause 172.2.5.1 requires a complete de-skew of all lanes
- This de-skew is not required and undesirable for low complexity modules

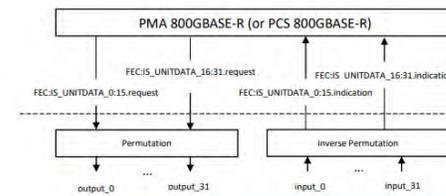
# Comment #472:

## • **Background:** Permutation function prerequisites (updated):

- 20bit RS(544,514) symbol alignment across lanes
- Complete lane de-skew to RS(544,514) codeword boundaries is optional

Motion #5 from July'23 Plenary: Move to adopt BCH FEC as defined in kota\_3dj\_01a\_2307.pdf slides 6-18 as the baseline FEC specification for the single wavelength 10 km 800Gb/s optical PMD

## Permutation/Inverse Permutation Functions



Pictorial Description of the permutation function



- Purpose: Provides 10bit symbols from 4 interleaved RS(544,514) codewords on each of 32 PCS lanes
- Prerequisites: 10bit symbol alignment across lanes. Lane reorder and FEC codeword deskew across lanes is optional
- Operates on 4 RS-symbol boundaries across 32 PCS lanes
- In the transmit direction, the permutation function maps the bits received on thirty-two PCS lanes through the FEC:IS\_UNITDATA\_0:31.request primitives and maps them to output lanes *output\_0:31*
  - Denote the index of the PCSL as  $p$  ( $p=0$  to  $31$ ), where the bits for the  $p^{\text{th}}$  lane are obtained through `FEC:IS_UNITDATA_p.request`
  - Denote the index of the aligned input 10-bit block across the PCSLs as  $i$  and the bit index within block  $i$  as  $j$  ( $j=0$  to  $9$ ).
  - Denote the index of the output lanes as  $q$  ( $q=0$  to  $31$ )
  - The mapping between the bit sequences on the PCSL and the *output\_q* is:
    - $output\_q[10i + j] = PCSL[(q + 16[i/2])\%32, 10i + j]$
- In the receive direction, the inverse permutation function maps the bits received on input lanes *input\_0:31* to thirty-two PCS lanes and provides this data through the `FEC:IS_UNITDATA_0:31.indication` primitives. Using similar definitions as the transmit, the mapping between the bit sequences on *input\_q* lanes and the PCSL is:
  - $PCSL[(q + 16[i/2])\%32, 10i + j] = input\_q[10i + j]$

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From [kota\\_3dj\\_01a\\_2307](#)

# Isolated Burst Tolerance

- Definition and assumptions:
  - Burst is isolated
  - Consecutive DP-QAM16 symbols are affected
  - All 8 bits of each DP-QAM16 symbol assumed to be in error
  - Inner BCH does not correct (or add) errors
  - All errors are corrected by outer KP4
- Burst tolerance results previously reported in OIF Q4'22 meeting.
  - Reference: [oif2022.419](#)
  - Compared all cases including fully de-skewed and partially de-skewed cases
  - Random lane order within each 400G flow and random deskew to 20b RS symbol boundaries provides at least **1200bit** burst tolerance
  - For comparison, 400ZR C-FEC provides a burst capability of ~1024bits (see [lyubomirsky 3cn 02a 1118](#))

# Comment #472: Suggested remedy

- Change 184.4.1 to the following:

## 184.4.1 Alignment Lock and Deskew

The alignment lock and deskew function, when implemented, shall be identical to the processes specified in 172.2.5.1 except that only a deskew to 20-bit (i.e. dual RS(544,514) symbol) boundaries across all PCS lanes is required.

# Comment #473

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CI 184      SC 184.5.7.2      P 528      L 20      # 473

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*Comment Type*    **TR**      *Comment Status*    **X**

This section defines an uncorrected codeword as "An uncorrected FEC codeword is a codeword that contains errors that were not corrected, including FEC codewords that may have been miscorrected or not completely corrected". However, codewords which are miscorrected are not detectable as uncorrected codewords.

*Suggested Remedy*

Update the definition to something similar to: "An uncorrected FEC codeword is a codeword with errors which are detectable at the decoder, but the decoder is unable to correct."

*Proposed Response*

*Response Status*    **O**

# Comment #473

- The requirement to count all uncorrected codewords is unreasonable
  - Some error patterns are undetectable. For e.g., when the result of errors is another valid codeword, the parity checks will not indicate any errors and therefore the errors cannot be detected or corrected.
  - Some error patterns can be mis-corrected. This can happen when the decoder is able to find an incorrect codeword which satisfies all other criterion

# Comment #473: Proposed remedy

- Update the definition of uncorrectable codewords to the following or equivalent:
  - “An uncorrected FEC codeword is a codeword with errors which are detectable at the decoder, but the decoder is unable to correct.”

Thank you!