

MPI Penalty for Optical PMDs

(Addressing comments 231, 232, 233, 234, 235)

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IEEE 802.3dj Interim Meeting

Phoenix

January 20, 2025

Overview

- ❑ **Discrepancy in MPI penalty**
- ❑ **Background on DGD penalty**
- ❑ **MPI penalty clause 180**
- ❑ **MPI penalty clause 181**
- ❑ **MPI penalty clause 182**
 - Some options to reduce 200GBASE-DR-2 MPI Penalty
- ❑ **MPI penalty clause 183**
- ❑ **Summary.**

Discrepancy in the MPI/DGD Penalties

- ❑ **Clause 180.7.3 supports 4 connectors at reflectance value listed below allocation of MPI/DGD penalty is 0.1 dB**
 - With 4 connectors, maximum discreet reflectance -35 dB for 200GBASE-DR1 and -45 dB for 400GBASE-DR2/800GBASE-DR4/1.6TBASE-DR8
 - Optical return loss (min) 27 dB for 200GBASE-DR1 and 37 dB for 400GBASE-DR2/800GBASE-DR4/1.6TBASE-DR8
- ❑ **Clause 181.7.3 at supports 4 connectors at reflectance value listed below and allocation of MPI/DGD penalty is 0.5 dB**
 - With 4 connectors maximum discreet reflectance -35 dB
 - Optical return loss (min) 27 dB
- ❑ **Clause 182.7.3 allocation of MPI/DGD penalty is 0.4 dB**
 - Supports 6 connectors, maximum discreet reflectance -35 dB for 200GBASE-DR1-2 and -45 dB for 400GBASE-DR2-2/800GBASE-DR4-2/1.6TBASE-DR8-2
 - Optical return loss (min) 25 dB for 200GBASE-DR1-2 and 37 dB for 400GBASE-DR2-2/800GBASE-DR4-2/1.6TBASE-DR8-2
- ❑ **Clause 183.7.3 allocation of MPI/DGD penalty is 0.5 dB for 800GBASE-FR4, 0.4 dB MPI and 0.7 dB DGD for 800GBASE-LR4**
 - With 6 connectors maximum discreet reflectance -38 dB for 800GBASE-FR4, and -35 dB for 800GBASE-LR4
 - Optical return loss (min) 25 dB for 800GBASE-FR4 and 22 dB for 800GBASE-LR4
- ❑ **MPI penalty based on statistical model proposed by [King 01a 01116 smf](#) developed in 802.3bs has been adopted widely adopted for MPI penalty estimation.**

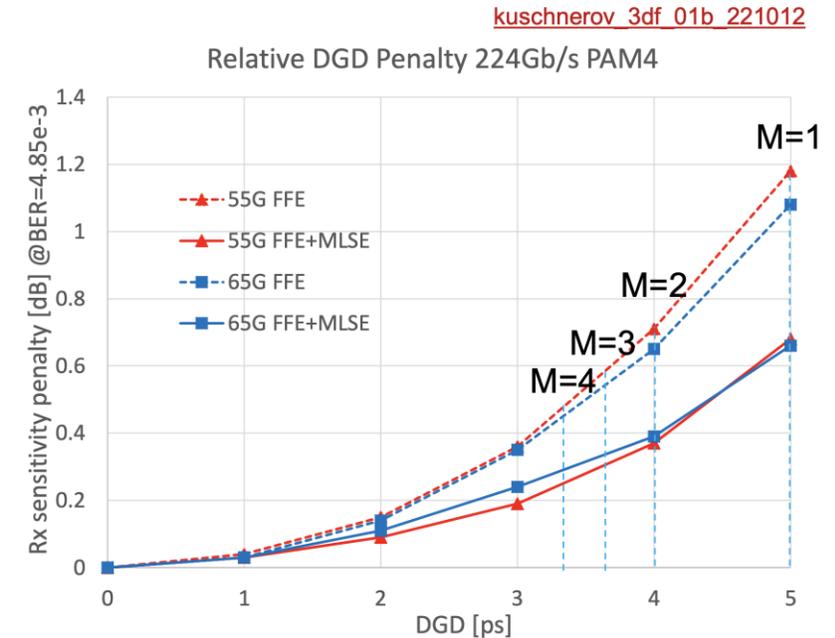
DGD Penalty for Clauses 180-183

□ [kuschnerov_3dj_optx_01_230829](#) show worst case DGD penalty of 0.7 dB for clause 183 800GBASE-LR4 PMD for max DGD of 4 ps

- 800GBASE-FR4 with max DGD of 2.3 ps has ~0.18 dB penalty
- 800GBASE-FR4/DRx-2 with max DGD of 2.3 ps has ~0.18 dB penalty
- 800GBASE-FR4-500/DRx with max DGD of 2.24 ps has ~0.18 dB penalty

DGD penalty for varying number of segments M

- The original single segment (M=1) PMD penalty was based on a FFE+MLSE receiver (0.7dB)
- Assuming multiple segments, a linear equalizer would be sufficient to achieve acceptable performance
- Given the available data and pending further discussion by the industry M=4 seems to be a reasonable assumption
- M=4 can achieve a penalty of ≤ 0.5 dB with an linear FFE equalizer

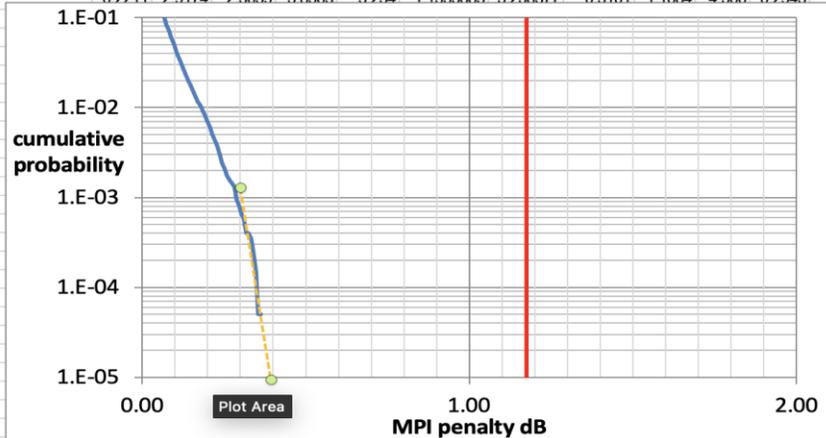


MPI Penalty for Clause 180

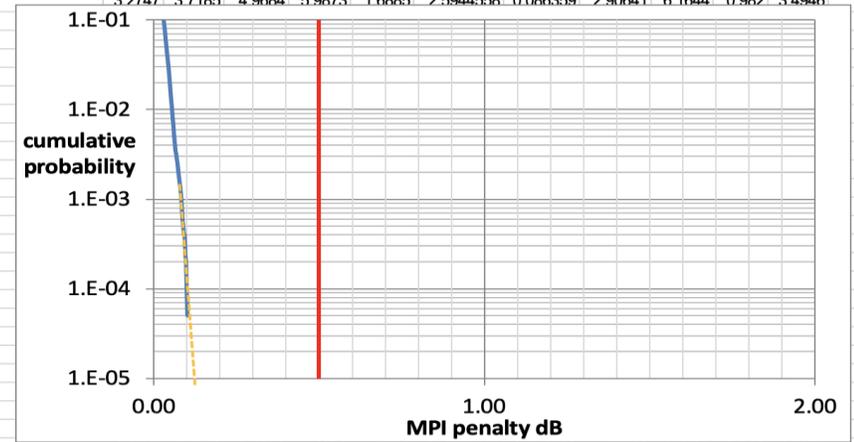
Use 4 connectors with discrete reflectance of -35 dB for 200GBASE-DR and -45 dB for 400GBASE-DR2, 800GBASE-DR4, and 1.6TBASE-DR8 for mid-span channel IL=1.5 dB

- 200GBASE-DR MPI penalty is ~0.4 dB +0.18 dB DGD, total penalty=0.58 dB, D1.3 MPI/DGP penalty= 0.1 dB
- 400GBASE-DR2, 800GBASE-DR4, and 1.6TBASE-DR8 penalty is ~0.12 dB +0.18 dB DGD, total penalty=0.3 dB, D1.3 MPI/DGP penalty= 0.1 dB.

Random phase between reflectors, random selection of modulation levels Polarization assumed aligned												
Baseline BER	average phase= 3.1418											
2.28E-04	PMD											
	R 1	R 2	R 3	R 4	R 5	R 6	R 7	R 8	R 9	R 10	R 11	R 12
Reflection level inputs->	-26	-55	-55	-55	-35	-35	-35	-35	-55	-55	-55	-26
N/C phases row:	0	0	0	0	0	0	0	0	0	0	0	0
L dB	0	0	0	0	0	0	0	0	0	0	0	0
1* adds distrib'd IL, 0 adds none	0	0	0	0	0	0	0	0	0	0	0	0
2xcum IL dB	0	0	0	0	0	0	-3	-3	-3	-3	-3	-3
Random phases =>	0.2211	2.9174	2.3659	3.8563	3.234	1.1355885	3.238377	0.3101	1.1684	4.566	0.2945	



Random phase between reflectors, random selection of modulation levels Polarization assumed aligned												
Baseline BER	average phase= 3.1441											
2.28E-04	PMD											
	R 1	R 2	R 3	R 4	R 5	R 6	R 7	R 8	R 9	R 10	R 11	R 12
Reflection level inputs->	-26	-55	-55	-55	-45	-45	-45	-45	-55	-55	-55	-26
N/C phases row:	0	0	0	0	0	0	0	0	0	0	0	0
L dB	0	0	0	0	0	0	0	0	0	0	0	0
1* adds distrib'd IL, 0 adds none	0	0	0	0	0	0	0	0	0	0	0	0
2xcum IL dB	0	0	0	0	0	0	0	0	-3	-3	-3	-3
Random phases =>	3.2747	3.7185	4.9684	5.9873	1.6885	2.5944558	0.086359	2.90641	6.1644	0.982	3.4946	



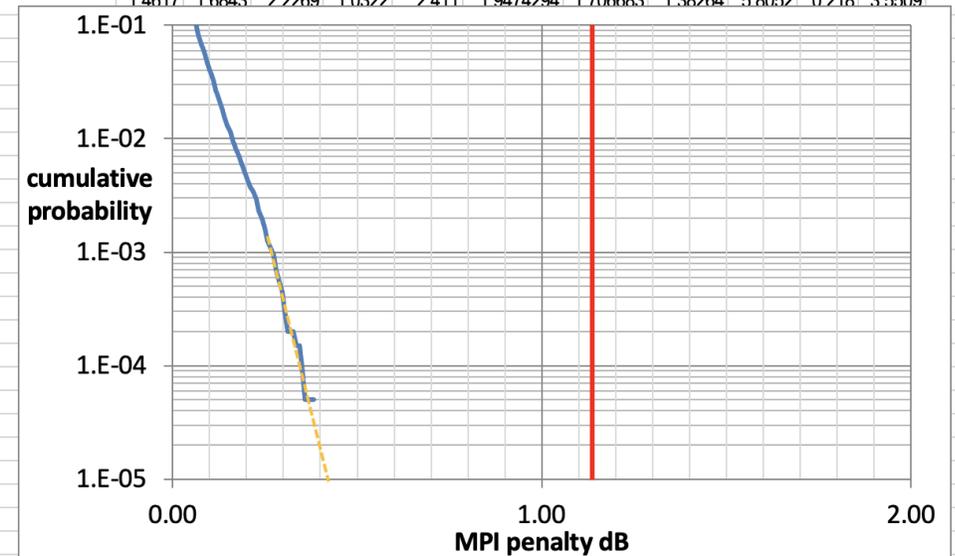
MPI Penalty for Clause 181

□ Use 4 connectors with discrete reflectance of -35 dB for 800GBASE-FR4-500 for mid-span channel IL=1.75 dB

- MPI penalty is ~0.41 dB with addition of 0.18 dB DGD penalty total penalty 0.59 dB
- In the D1.3 MPI/DGD penalty= 0.5 dB

Random phase between reflectors, random selection of modulation levels
Polarization assumed aligned

	PAM-N												ER	dER
	N= 4												3.5	0.447
Baseline BER	average phase= 3.1379													
	PMD													
	R 1	R 2	R 3	R 4	R 5	R 6	R 7	R 8	R 9	R 10	R 11	R 12		
	Rpmd	RconF	RconG	RconG	RconH	RconK	RconK	RconH	RconG	RconG	RconF	Rpmd		
Reflection level inputs->	-26	-55	-55	-55	-35	-35	-35	-35	-55	-55	-55	-26		
	phase b phase b phase be -1.10 phase be phase betwe phase betw phase bet phase between													
	int1-int2 int2-int3 int3-int4 int4-int5 int5-int6 int6-int7 int7-int8 int8-int9 int9-int10 int10-int11 int11-int12													
W/C phases row:	0 0 0 0 0 0 0 0 0 0 0 0 0 0													
	mid-span IL													
IL dB	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1' adds distrib'd IL, 0 adds none	0													
2xcum IL dB	0	0	0	0	0	0	0	-3.5	-3.5	-3.5	-3.5	-3.5	-3.5	-3.5
Random phases =>	1.4617	1.6843	2.2269	1.0322	2.411	1.9474	2.94	1.7066	83	1.3826	4	5.8052	0.218	3.5509

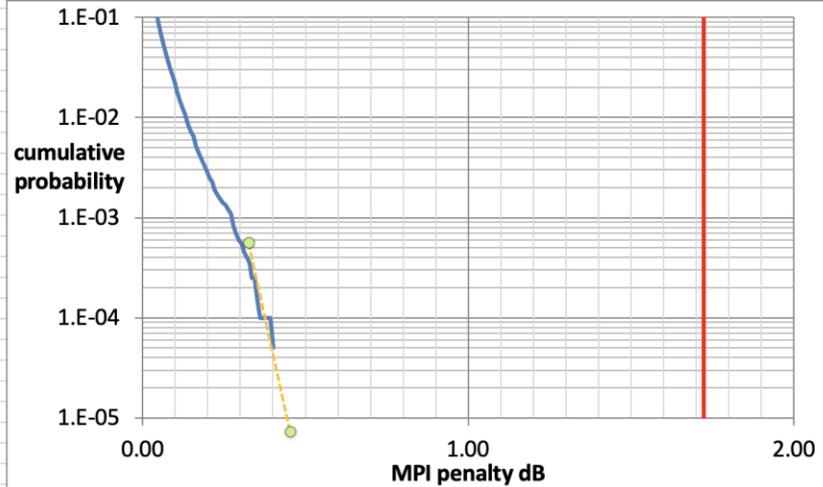


MPI Penalty for Clause 182

- Use 6 connectors with discrete reflectance of -35 dB for 200GBASE-DR-2 and -45 dB for 400GBASE-DR2-2, 800GBASE-DR4-2, and 1.6TBASE-DR8-2 with mid-span loss of 2 dB
 - 200GBASE-DR-2 MPI penalty is ~ 0.45 dB + 0.18 dB DGD total penalty = 0.63 dB, D1.3 MPI/DGD penalty = 0.4 dB
 - 400GBASE-DR2-2, 800GBASE-DR4-2, and 1.6TBASE-DR8-2 penalty is ~ 0.1 dB + 0.18 dB DGD total penalty = 0.28 dB, D1.3 MPI/DGD penalty = 0.4 dB.

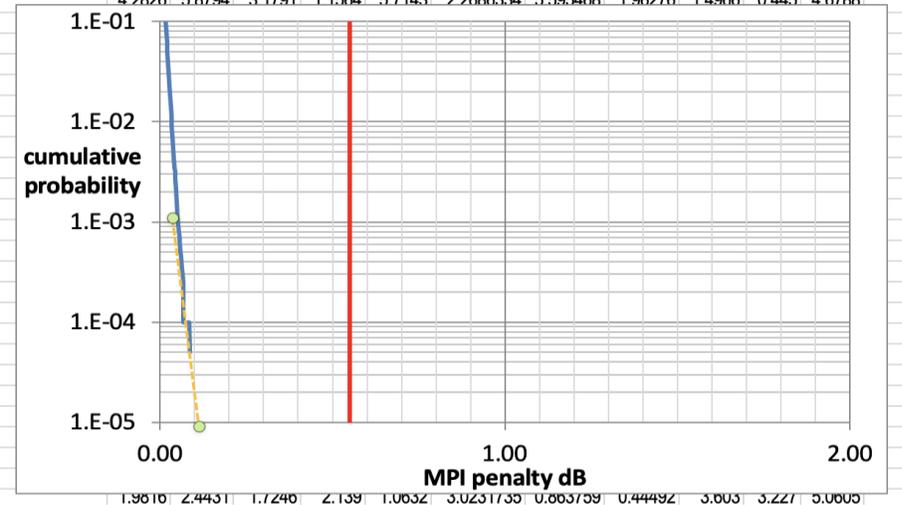
Random phase between reflectors, random selection of modulation levels
Polarization assumed aligned

Baseline BER	average phase=	PAM-N											ER	dER
4.80E-03	3.1383	N= 4											3.5	0.4
	PMD												PMD	
	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12		
	RpmD	RconF	RconG	RconG	RconH	RconK	RconK	RconH	RconG	RconG	RconF	RpmD		
Reflection level inputs->	-26	-35	-55	-55	-35	-35	-35	-35	-55	-55	-35	-26		
	phase b	phase b	phase b	-110	phase b	phase betw	phase betw	phase bet	phase between	phase bet	phase between			
	int1-int2	int2-int3	int3-int4	int4-int5	int5-int6	int6-int7	int7-int8	int8-int9	int9-int10	int10-int11	int11-int12			
W/C phases row:	0	0	0	0	0	0	0	0	0	0	0	0	0	0
						mid-span IL								
IL dB	0	0	0	0	0	2	0	0	0	0	0	0	0	0
1' adds distrib'd IL, 0 adds none	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2xcum IL dB	0	0	0	0	0	0	-4	-4	-4	-4	-4	-4	-4	-4
Random phases =>	5.3074	1.1371	3.5226	4.254	0.3127	1.1663455	1.61584	6.11508	5.6816	3.015	0.8901			



Random phase between reflectors, random selection of modulation levels
Polarization assumed aligned

Baseline BER	average phase=	PAM-N												ER	dER
4.80E-03	3.1448	N= 4												3.5	0.447
	PMD													PMD	
	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12			
	RpmD	RconF	RconG	RconG	RconH	RconK	RconK	RconH	RconG	RconG	RconF	RpmD			
Reflection level inputs->	-26	-45	-55	-55	-45	-45	-45	-45	-55	-55	-45	-26			
	phase b	phase b	phase b	-110	phase b	phase betw	phase betw	phase bet	phase between	phase bet	phase between				
	int1-int2	int2-int3	int3-int4	int4-int5	int5-int6	int6-int7	int7-int8	int8-int9	int9-int10	int10-int11	int11-int12				
W/C phases row:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
						mid-span IL									
IL dB	0	0	0	0	0	2	0	0	0	0	0	0	0	0	
1' adds distrib'd IL, 0 adds none	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
2xcum IL dB	0	0	0	0	0	0	-4	-4	-4	-4	-4	-4	-4	-4	
Random phases =>	4.2826	5.8794	3.1791	1.1564	5.7143	2.2686334	5.595468	1.96276	1.4966	0.445	4.6788				



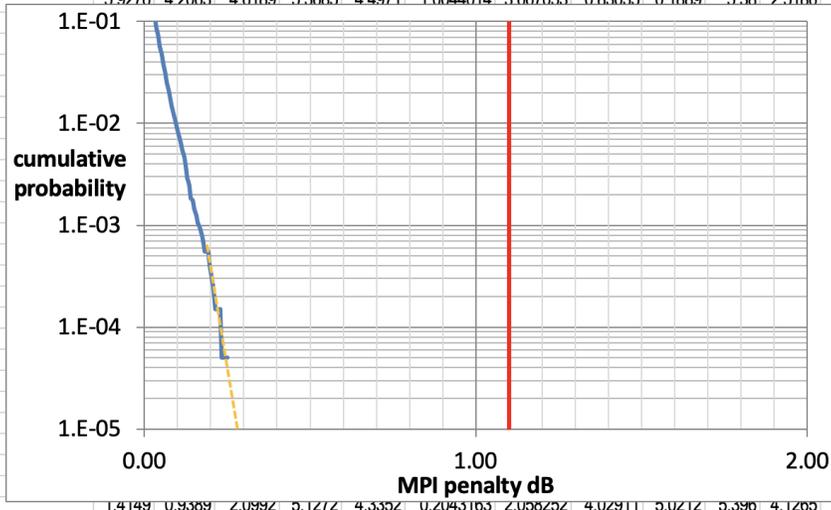
Some Options to Reduce 200GBASE-DR-2 MPI Penalty

Options reducing MPI penalty such that total penalty meets current 0.4 dB

- Supporting 4 connectors at -35 dB then MPI penalty reduced to 0.28 dB with 0.18 dB DGD total penalty=0.46 dB
- Supporting 4 connectors at -38 dB then MPI penalty reduced to 0.17 dB with 0.18 dB DGD total penalty=0.36 dB

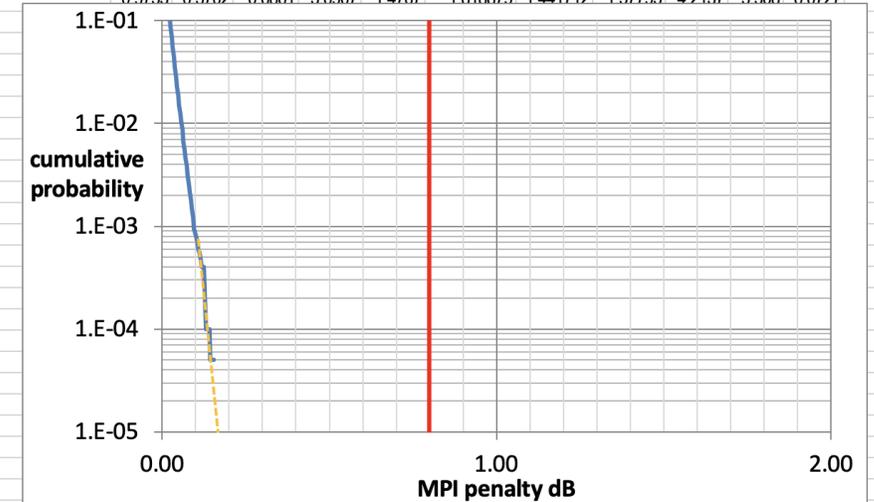
Random phase between reflectors, random selection of modulation levels
Polarization assumed aligned

Baseline BER	average phase=	PAM-N												ER	dER	1/1-dER
4.80E-03	3.1386	N= 4												3.5	0.447	1.8072842
PMD																
	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	PMD			
	Rpmd	RconF	RconG	RconG	RconH	RconK	RconK	RconH	RconG	RconG	RconF	Rpmd				
Reflection level inputs->	-26	-55	-55	-55	-35	-35	-35	-55	-55	-55	-26					
phase b phase b phase be -110 phase b phase betwe phase bet phase bet phase between																
int1-int2 int2-int3 int3-int4 int4-int5 int5-int6 int6-int7 int7-int8 int8-int9 int9-int10 int10-int11-int12																
W/C phases row:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	w/c
IL dB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Tot IL=
1' adds distrib'd IL, 0 adds none	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1.99
2xcum IL dB	0	0	0	0	0	0	-3.98	-3.98	-3.98	-3.98	-3.98	-3.98	-3.98	-3.98	-3.98	1.99
Random phases =>	5.9276	4.2063	4.6189	5.3685	4.4971	1.0044	0.14	3.6670	5.3	0.83035	0.1889	5.38	2.5186			



Random phase between reflectors, random selection of modulation levels
Polarization assumed aligned

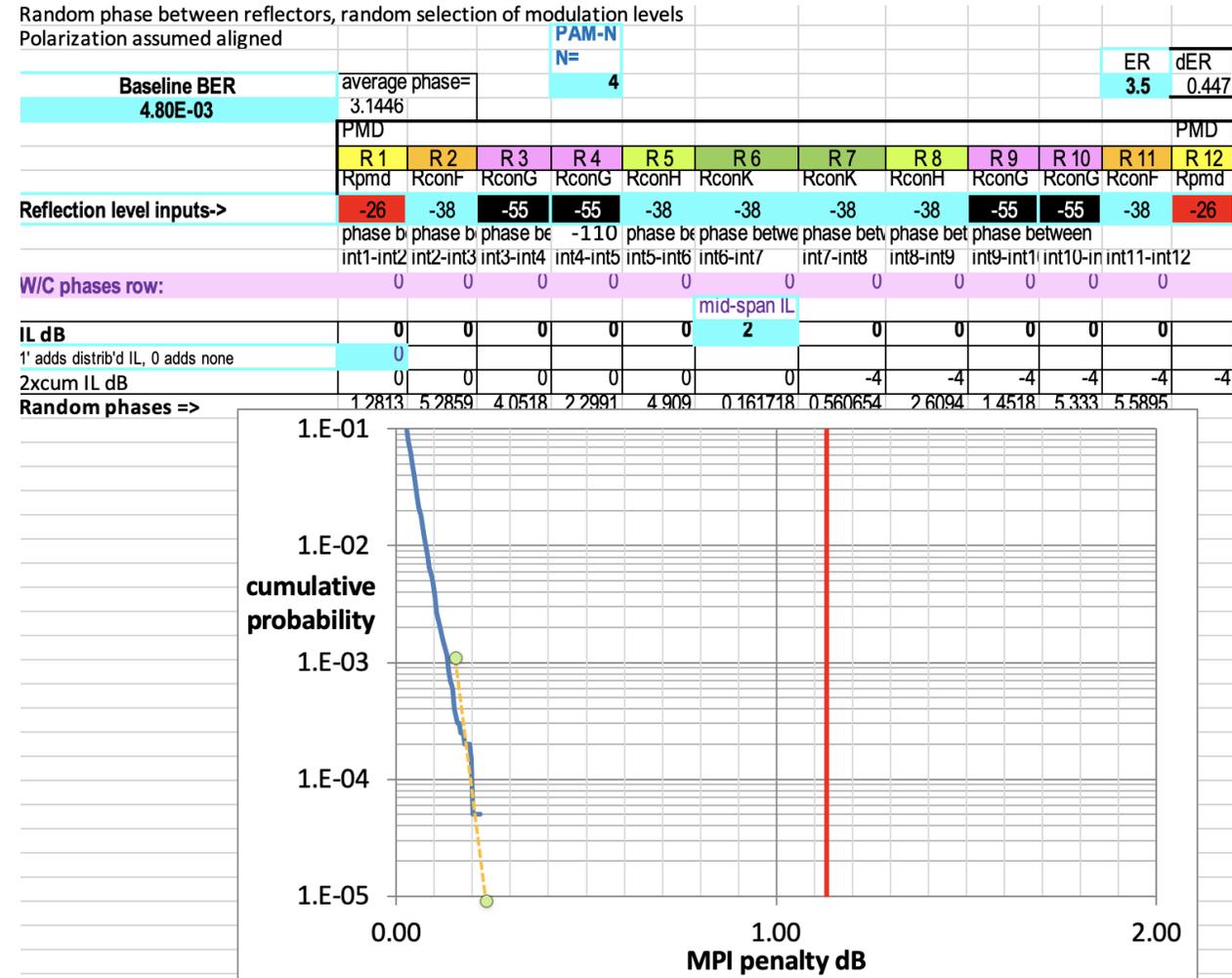
Baseline BER	average phase=	PAM-N												ER	dER	1/1-dER
4.80E-03	3.1401	N= 4												3.5	0.447	1.8072842
PMD																
	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	PMD			
	Rpmd	RconF	RconG	RconG	RconH	RconK	RconK	RconH	RconG	RconG	RconF	Rpmd				
Reflection level inputs->	-26	-55	-55	-55	-38	-38	-38	-38	-55	-55	-26					
phase b phase b phase be -110 phase b phase betwe phase bet phase bet phase between																
int1-int2 int2-int3 int3-int4 int4-int5 int5-int6 int6-int7 int7-int8 int8-int9 int9-int10 int10-int11-int12																
W/C phases row:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	w/c
IL dB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Tot IL=
1' adds distrib'd IL, 0 adds none	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1.99
2xcum IL dB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1.99
Random phases =>	0.9753	0.5702	0.6861	3.6907	1.4767	1.818879	1.441712	1.57795	4.2137	5.508	6.0727					



MPI Penalty for Clause 183 800GBASE-FR4

□ Use 6 connectors with discrete reflectance of -38 dB for mid-span channel IL=2 dB

- MPI penalty is ~0.23 dB with addition of 0.18 dB DGD penalty total penalty 0.41 dB
- In the D1.3 MPI/DGD penalty= 0.5 dB



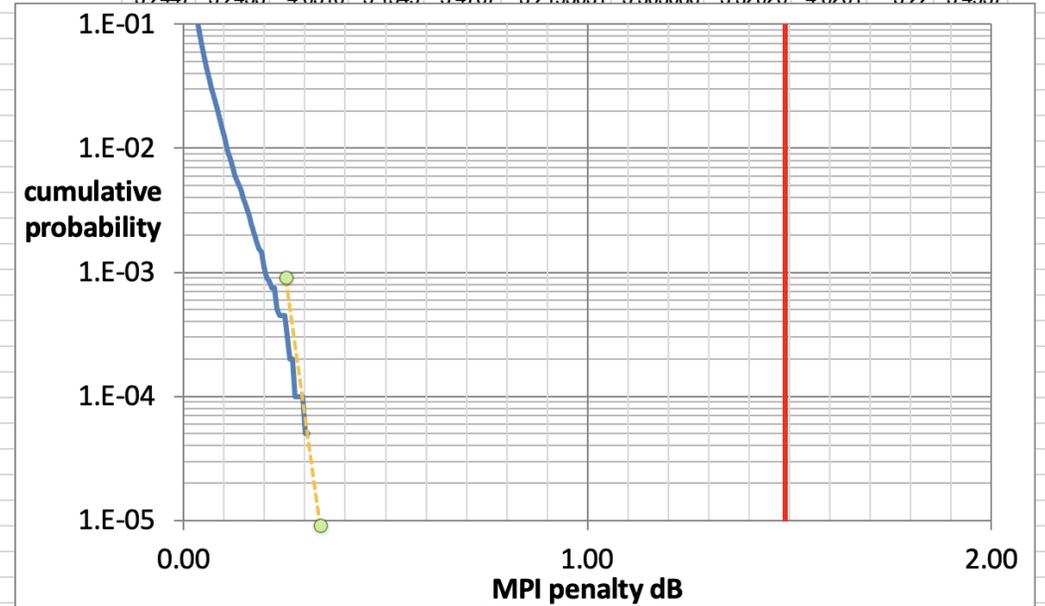
MPI Penalty for Clause 183 800GBASE-LR4

Use 6 connectors with discrete reflectance of -35 dB for mid-span channel IL=3.2 dB

- MPI penalty is ~0.32 dB
- In the D1.3 MPI penalty= 0.4 dB

random phase between reflectors, random selection of modulation levels
polarization assumed aligned

Baseline BER 4.80E-03	average phase= 3.1373	PAM-N N= 4										ER 3.5	dER 0.447	
PMD													PMD	
	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12		
	Rpmd	RconF	RconG	RconG	RconH	RconK	RconK	RconH	RconG	RconG	RconF	Rpmd		
Reflection level inputs->	-26	-35	-55	-55	-35	-35	-35	-35	-55	-55	-35	-26		
	phase b	phase b	phase b	-110	phase b	phase between	phase bet	phase bet	phase between					
	int1-int2	int2-int3	int3-int4	int4-int5	int5-int6	int6-int7	int7-int8	int8-int9	int9-int10	int10-int11	int11-int12			
C phases row:	0	0	0	0	0	0	0	0	0	0	0	0		
dB	0	0	0	0	0	3.2	0	0	0	0	0	0		
dds distrib'd IL, 0 adds none	0													
cum IL dB	0	0	0	0	0	0	-6.4	-6.4	-6.4	-6.4	-6.4	-6.4		
random phases =>	3.2447	3.2453	4.6316	5.1549	5.4767	3.2195051	5.503086	3.32026	4.6201	3.22	3.4957			



Summary

- ❑ **The biggest issue in D1.3 is associated with 200GBASE-DR and 200GBASE-DR-2 as these PMDs use connectors with lower return losses and current MPI allocation is not sufficient**
 - With 35 dB connector return loss need to limit the number of connectors to 4, then only make a slight adjustment to the MPI penalty
 - MPI penalty for 400GBASE-DR2, 800GBASE-DR4, and 1.6TBASE-DR8 need to increase by ~ 0.1 dB
 - MPI penalty for 800GBASE-FR4-500 also need to increase by ~ 0.1 dB
- ❑ **Clause 182 400GBASE-DR2-2, 800GBASE-DR4-2, and 1.6TBASE-DR8-2 allocated MPI penalty is slightly larger than needed for of $SER=9.6E-3$, MPI can be reduced by ~ 0.1 dB**
 - Keeping the current 0.4 dB MPI penalty for 400GBASE-DR2-2, 800GBASE-DR4-2, and 1.6TBASE-DR8-2 is a better option
 - Allows to reconcile with 200GBASE-DR-2 as 0.4 dB MPI penalty is sufficient for this PMD if the # of connectors are reduced to 4
- ❑ **Clause 183 allocated MPI/DGD slightly larger than needed at $SER=9.6E-3$ and MPI can be reduced by ~ 0.1 dB.**

Thank You!