PHY transmitter block error ratio

Draft 1.3 comment #8

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Supporters

Introduction

- In Draft 1.3, test methods and limits are provided to measure and constrain the block error ratio for a PHY receiver.
- This method takes into account errors that might be added by the PHY transmitter at the other end of a link.
- An analogous method is not provided to test and constrain a PHY transmitter.
- This contribution proposes a methodology and constraints for a PHY transmitter
- Addresses Draft 1.3 comment #8.

Comment

Cl **174A**	*SC* **174A.6.2**	*P* **739**	*L* **15**	# 8

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Comment Type **T** *Comment Status* **X**

Residual errors are permitted at a C2M component output or PMD transmit output when part of a PHY. This residual error ratio must be constrained in the same way errors generated by a PHY transmitter are constrained.

SuggestedRemedy

Add frame loss error ratio and block error ratio constraints for the transmitter output of a complete PHY. Methodology may need to be added in 174A. A contribution will provide more details.
New specifications are need in each of PMD clauses: 178 through 183.

Proposed Response *Response Status* **O**

The transmit path on an PHY has errors due to the AUIs as follows:

For electrical PHYs a single C2C AUI is permitted up to 0.08E-4.

For optical PHYs a combination of C2C and C2M AUI is permitted up to 0.32E-4 combined.

There are no normative specifications to mandate this nor a related test method.

Table 174A–1—Error ratio allocations for optical PHYs

Sublayer or interface	Frame loss ratio for entire PHY	Codeword error ratio for entire PHY	BER for entire PHY (BER_{total})	BER per sublayer in a PHY
xAUI-n C2C[a]				0.08×10^{-4}
xAUI-n C2M	6×10^{-11}	1.45×10^{-11}	2.92×10^{-4}	0.24×10^{-4}
PMD-to-PMD				2.28×10^{-4}
xAUI-n C2M				0.24×10^{-4}
xAUI-n C2C				0.08×10^{-4}

[a] If the PMD is a type defined in Clause 180, Clause 181, Clause 182, or Clause 183 (i.e., 200 Gb/s per lane), and xAUI-n C2C is a type defined in Annex 120D (i.e., 50 Gb/s per lane) or Annex 120F (i.e., 100 Gb/s per lane), the xAUI-n C2C is expected to meet at the BER allocations in this table.

Table 174A–2—Error ratio allocations for electrical PHYs

Sublayer or interface	Frame loss ratio for entire PHY	Codeword error ratio for entire PHY	BER for entire PHY (BER_{total})	BER per sublayer in a PHY
xAUI-n C2C[a]				0.08×10^{-4}
PMD-to-PMD	6×10^{-11}	1.45×10^{-11}	2.92×10^{-4}	2.76×10^{-4}
xAUI-n C2C				0.08×10^{-4}

[a] If the PMD is a type defined in Clause 178 or Clause 179 (i.e., 200 Gb/s per lane) and xAUI-n C2C is a type defined in Annex 120D (i.e., 50 Gb/s per lane) or Annex 120F (i.e., 100 Gb/s per lane), the xAUI-n C2C is expected to meet the BER allocations in this table.

Test for PHY Rx

174A.7 provides a test methodology to constrain the error contributions from a PHY receiver.

A similar approach can be adopted for measuring and constraining the error ratio at the PHY transmitter.

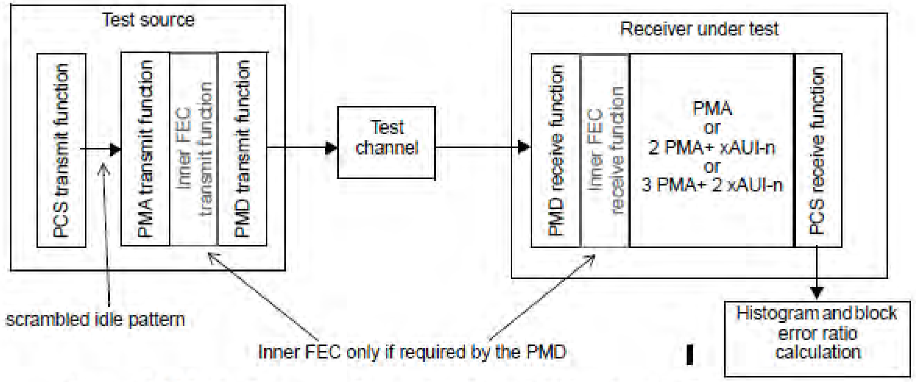

Figure 174A–4—Test configuration for a PHY using PCS counters

178.2 Error ratio allocation

A complete PHY is expected to meet the frame loss ratio specifications in 174A.5.

A PMD is expected to meet the block error ratio specifications in 174A.6, measured at the PMA adjacent to the PMD, with BER_{added} equal to 1.6×10^{-5}.

A PHY is expected to meet the block error ratio specifications in 174A.7, measured at the PCS, with BER_{added} equal to 8×10^{-6}.

This is specifically for the PHY receive path

180.2 Error ratio allocation

A complete PHY is expected to meet the frame loss ratio specifications in 174A.5.

A PMD is expected to meet the block error ratio specifications in 174A.6, measured at the PMA adjacent to the PMD, with BER_{added} equal to 6.4×10^{-5}.

A PHY is expected to meet the block error ratio specifications in 174A.7, measured at the PCS, with BER_{added} equal to 3.2×10^{-5}.

174A.7 Error ratio tests for a PCS-to-PCS path and PHY

This subclause defines a test method for a PCS-to-PCS path which includes 200 Gb/s per lane signaling on one or more ISLs.

The test method may be used to verify that the error ratio over the PCS-to-PCS path is within the error ratio allocation for the PHY. This method utilizes the term BER_{added} defined in 174A.6.

174A.7.1 Block error ratio method using PCS-based measurements

This test method permits measurement of the performance of all physical lanes in a PHY as a group using FEC error counters in the PCS. If this test passes, then PHY will meet the expected codeword error ratio.

174A.7.1.1 Test configuration

The configuration for a PHY test using the PCS is illustrated in Figure 174A–4.

174A.7.1.2 PCS Error Counters

The following defined PCS counters are utilized

— FEC_cw_counter: total codewords

— FEC_codeword_error_bin_k: codewords

— FEC_uncorrected_cw_counter: codewor

— FEC_corrected_cw_counter: codewords

A counter for codewords with no symbol errors FEC_cw_counter – FEC_corrected_cw_counter

174A.7.1.3 PCS error histogram measurement

An error histogram using PCS counters is measured using the following method:

a) At the transmitting device generate a scrambled idle test pattern in the PCS.

b) At the receiving PCS measure symbol errors using the defined PCS counters. The total number of codewords analyzed, FEC_cw_counter, should be sufficiently large to reliably verify that the expected block error ratio is met, either by direct measurement or statistical projection. The projection should provide an accurate prediction of the value of $H_m(k)$ that would be observed over longer-term testing or at least provide an upper bound on the value.

c) Calculate the measured histogram $H_m(k)$.

A measured error histogram $H_m(k)$ is calculated as follows:

— For k in the range 0 to 15, $H_m(k)$ = FEC_codeword_error_bin_k / FEC_cw_counter

— $H_m(16)$ = FEC_uncorrected_cw_counter / FEC_cw_counter

174A.7.1.4 PCS block error ratio method

The following method is used to calculate the block error ratio using FEC bin counters provided in the PCS.

a) Measure the error histogram $H_{mu}(k)$ with no stress applied to any lane.

b) Measure the error histogram $H_{ms}^{(i)}(k)$ for each lane i with stress applied only to lane i.

c) Calculate the composite error histogram $H_{ms}(k)$ as follows.

d) Initialize $H_{ms}(k)$ to $H_{ms}^{(0)}(k)$.

e) Iteratively, for each lane $i > 0$, assign the result of Equation (174A–5) and Equation (174A–6) to $H_{ms}(k)$ substituting $H_{ms}(k)$ for $H_x(k)$ for $H_{ms}^{(i)}(k)$ for $H_y(k)$, and optionally (for better accuracy) deconvolve $H_{mu}(k)$ from $H_{ms}(k)$.

f) Calculate the error histogram $H_a(k)$ for the added BER using Equation (174A–3) with $\mathrm{BER} = \mathrm{BER}_{added}$.

g) Assign the result of Equation (174A–5) and Equation (174A–6) to $H_{ms}(k)$ substituting $H_{ms}(k)$ for $H_x(k)$ and $H_a(k)$ for $H_y(k)$.

h) The measured block error ratio is equal to $H_{ms}(16)$.

The measured codeword error ratio is expected be less than 1.45×10^{-11}.

Proposed updates to Annex 174A

A test for a PHY transmitter can be defined largely based upon the test for the PHY receiver.

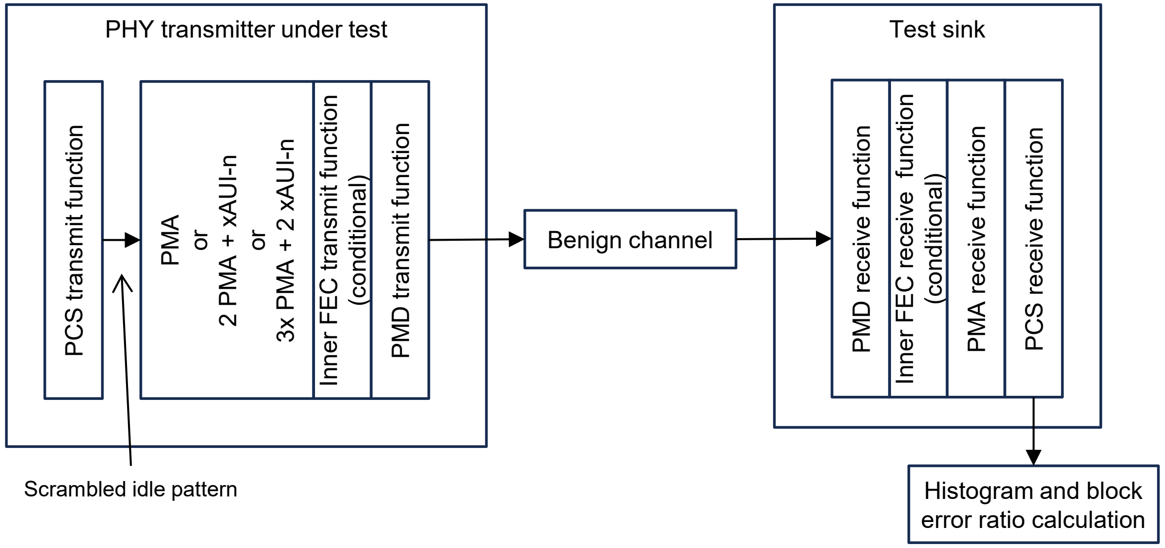

Figure 174A-x—Test configuration for a PHY transmitter

The figure to the left may be added to represent the test configuration for a PHY transmitter. The method below can be added for measurement of block error ratio for a PHY transmitter.

174A.7.1.5 PCS block error ratio test method for PHY transmitter

The following method is used to calculate the block error ratio for a PHY transmitter using FEC bin counters provided in the PCS.

a) Measure the error histogram $H_m(k)$ using the method defined in 174A.7.1.3.
b) Calculate the histogram $H_a(k)$ for the added BER using Equation (174A–3) with BER = BER_{added}.
g) Assign the result of Equation (174A–5) and Equation (174A–6) to $H_m(k)$ substituting $H_m(k)$ for $H_x(k)$ and $H_a(k)$ for $H_y(k)$.
h) The measured block error ratio is equal to $H_m(16)$.

The measured block error ratio is expected be less than 1.45×10^{-11}.

Proposed updates to PMD clauses

Change 178.2 and 179.2 as follows:

178.2 Error ratio allocation

…

A PHY receiver is expected to meet the block error ratio specifications in 174A.7, measured at the PCS, with BER_{added} equal to 8×10^{-6}.

A PHY transmitter is expected to meet the block error ratio specifications in 174A.7, measured at the PCS, with BER_{added} equal to 2.84×10^{-4}.

Change 180.2, 181.2, 182.2, 183.2, and 185.2 as follows:

180.2 Error ratio allocation

…

A PHY receiver is expected to meet the block error ratio specifications in 174A.7, measured at the PCS, with BER_{added} equal to 3.2×10^{-5}.

A PHY transmitter is expected to meet the block error ratio specifications in 174A.7, measured at the PCS, with BER_{added} equal to 2.6×10^{-4}.

Thanks