Partial Channel Model Impacts on COM for CR Channels

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Related to comments #393 and 466

Supporters

- TBD

Cl 179 *SC* 179.11.7.1 *P* 394 *L* 27 # 466

Kocsis, Sam Amphenol

Comment Type T *Comment Status* X

The partial host channel model parameters unnecessarily degrade COM perofmance. C0 is the same value as the previous specification generation.

SuggestedRemedy

Set to 0, OR remove C0 and C1 parameters

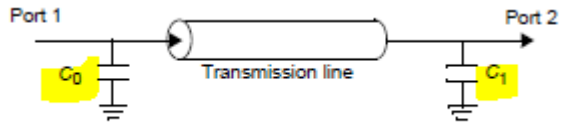
Proposed Response *Response Status* O

Background

- The partial host channel model parameters for CR compliance (COM), are specified in Table 179-16

Table 179–16—Host model parameters

Partial host channel model			
Single-ended package capacitance at port 1	C_0	2.9×10^{-5}	nF
Transmission line parameter γ_0	$\gamma_0^{(h)}$	0	1/mm
Transmission line parameter a_1	$a_1^{(h)}$	5.95×10^{-4}	$ns^{1/2}/mm$
Transmission line parameter a_2	$a_2^{(h)}$	2.6×10^{-5}	ns/mm
Transmission line parameter τ	$\tau^{(h)}$	5.79×10^{-3}	ns/mm
Transmission line characteristic impedance	$Z_c^{(h)}$	92.5	Ω
Transmission line length	$z_p^{(h)}$	See Table 179–17	mm
Single-ended package capacitance at port 2	C_1	1×10^{-5}	nF



Background

- Partial host channel is only required* for CR compliance (COM)

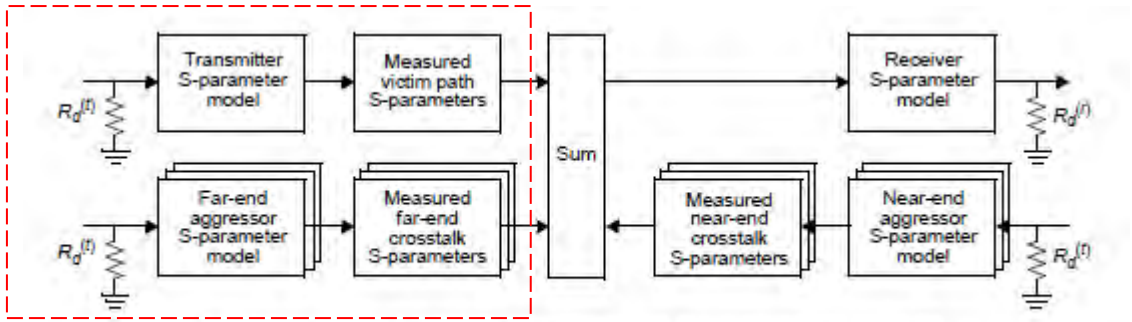
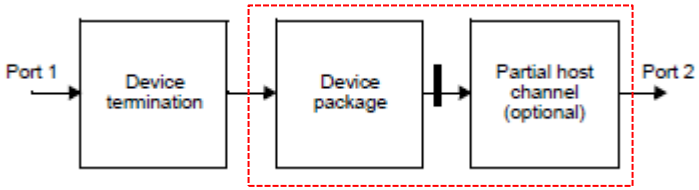
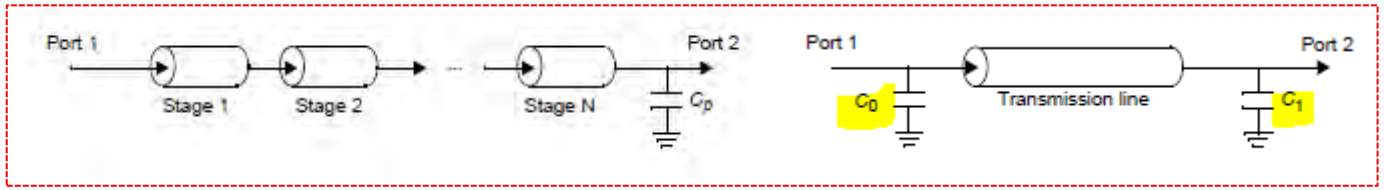


Figure 178A–1—Channel considered for the calculation of COM



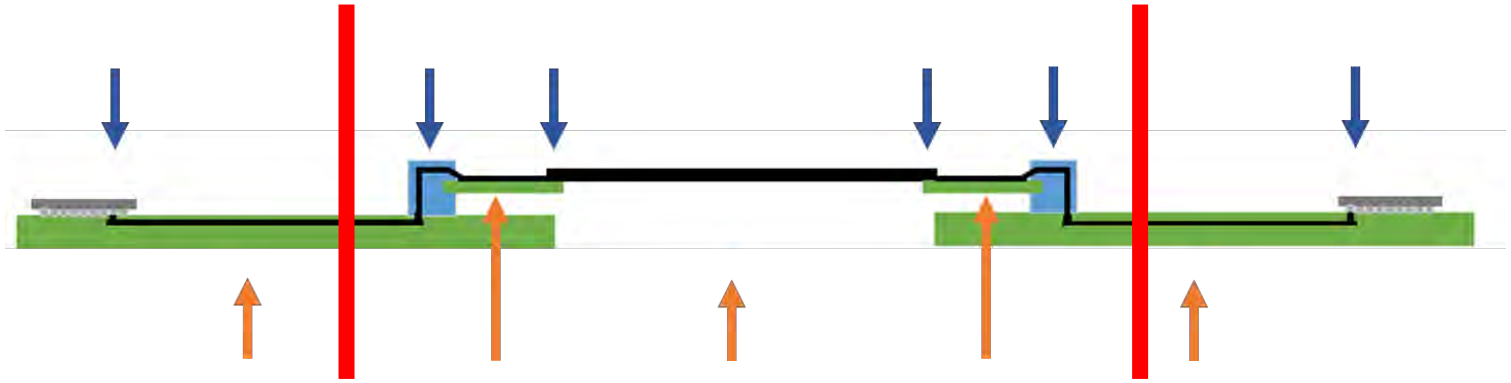
C0 is physically abutted next to Cp

C1 is physically abutted next to TP1



Motivation

- There are currently (0) models posted to the TF page for CR (TP1-TP4)
- Lim_3dj_01a_2409 was used define the partial host channel model
- The decision was justified, but failed to correctly look at C0 and C1
  - If C0 is a package parameter, it should be compliance parameter setting applied for TX, RX, and KR testing
  - C1 is neither a package parameter, nor explicitly a “connector via”
  - If C0 and C1 are to remain only normative for CR (TP1-TP4) tests, the decision should take into the impact on TP1-TP4 data



Supporting Data

- COM v4.70 (configuration file below)
- ERL for all > 8.7dB (8.25dB)
  - With no test fixture delay applied (Tfx)
- COM results for both CA-B and CA-C
  - Crosstalk not included

Table 179–13—Cable assembly characteristics summary

Description	Reference	Value	Unit
Insertion loss at 53.125 GHz, *ILdd* (max)	179.11.2		
CA-A		19	dB
CA-B		24	dB
CA-C		29	dB
CA-D		34	dB
Insertion loss at 53.125 GHz, *ILdd* (min)	179.11.2	16	dB
Minimum cable assembly ERL[a]	179.11.3	8.25	dB

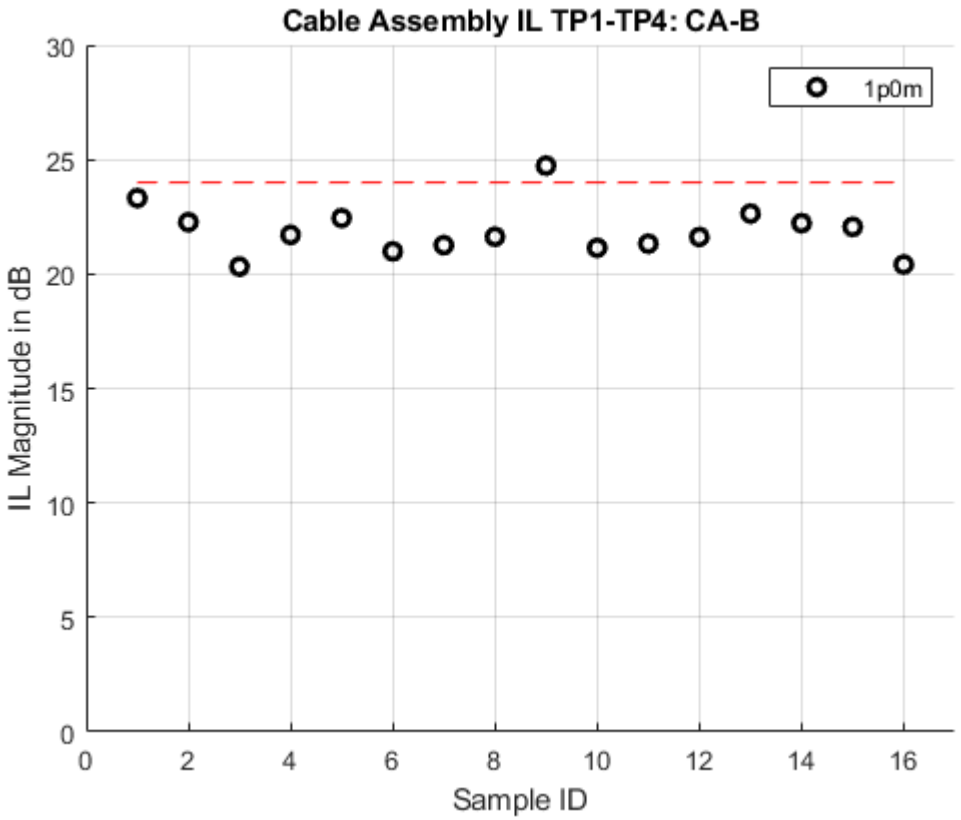
Table 179–15—Cable assembly class and host model valid combinations

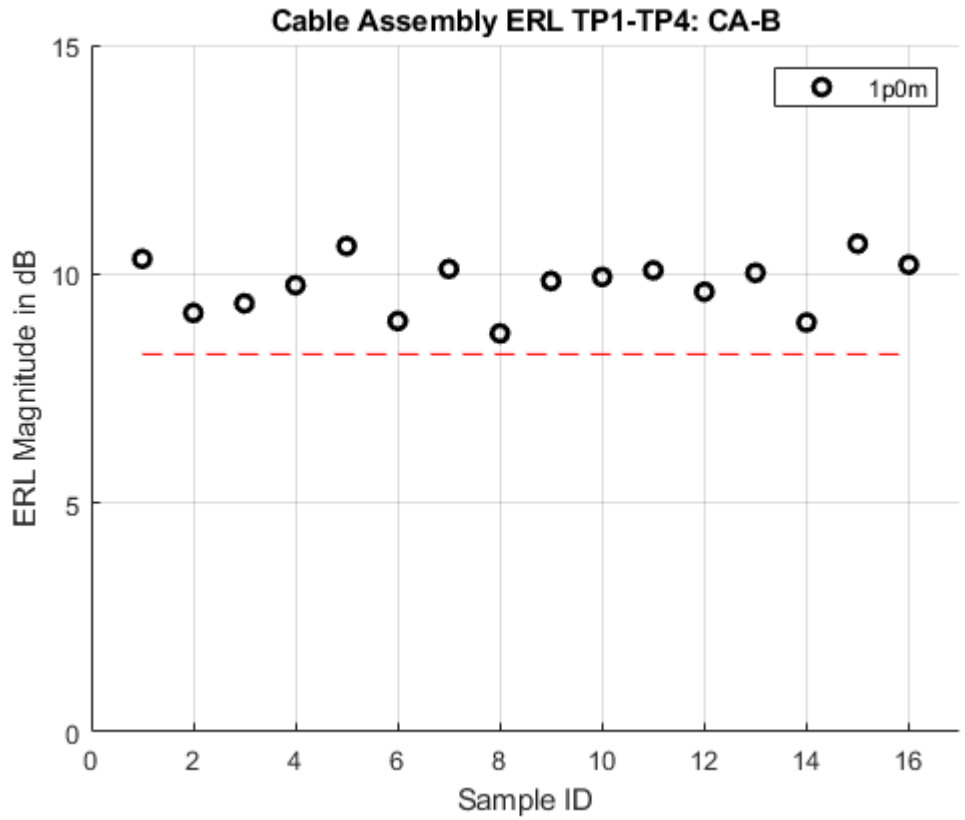
Cable assembly class	Host classes, transmitter side	Host classes, receiver side	Number of combinations
CA-A	HN or HL	HL, HN, or HH	6
	HH	HL or HN	2
CA-B	HL	HL, HN, or HH	3
	HN	HL or HN	2
	HH	HL	1
CA-C	HL	HL or HN	2
	HN	HL	1
CA-D	HL	HL	1

Table 179–17—Partial host channel model parameters per Host class

Parameter	Host class			Units
	HL	HN	HH	
Package class	A	B	B	—
Package transmission line 1 length, $z_p^{(1)}$	8	15	45	mm
Partial host PCB transmission line length, $z_p^{(h)}$	9	70	60	mm

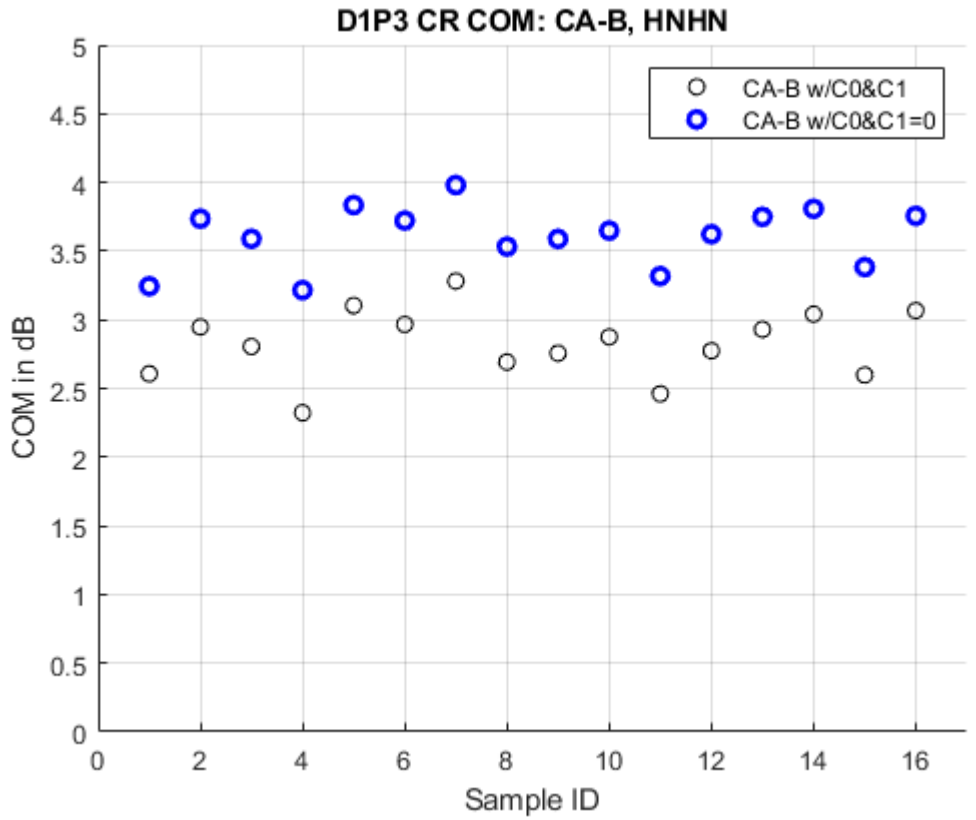
Supporting Data (CA-B)





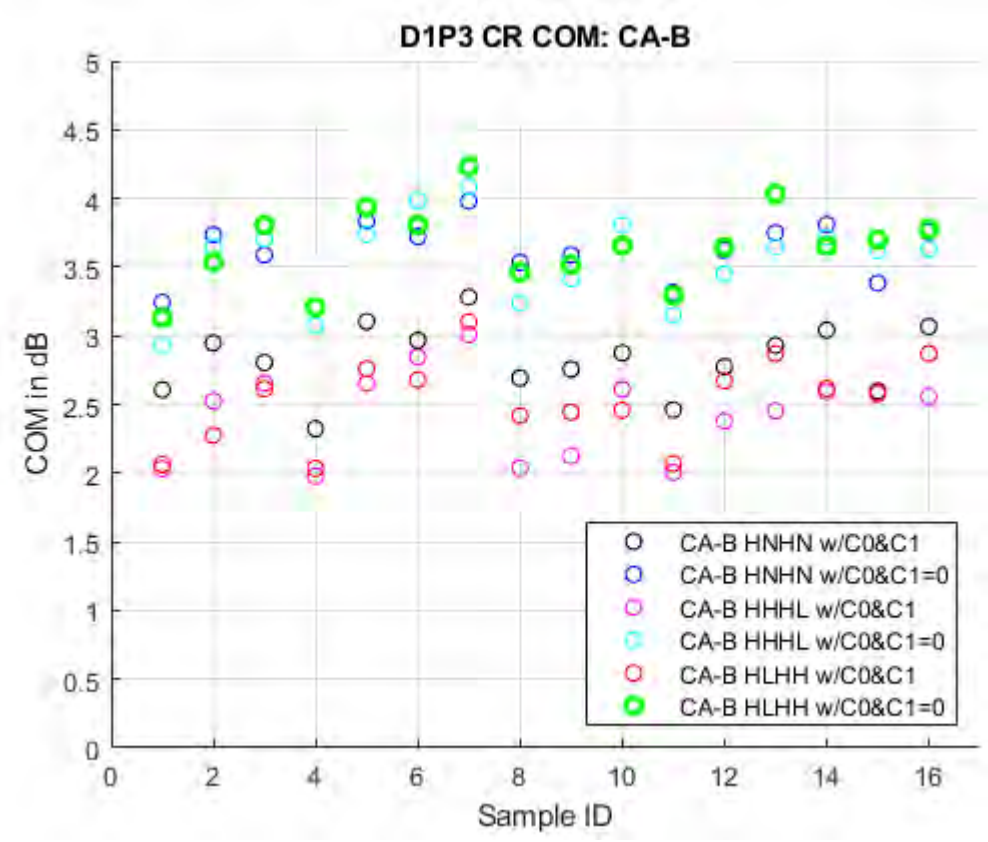
Nominal 1.0m measurements @TP1-TP4 across an entire port (octal)

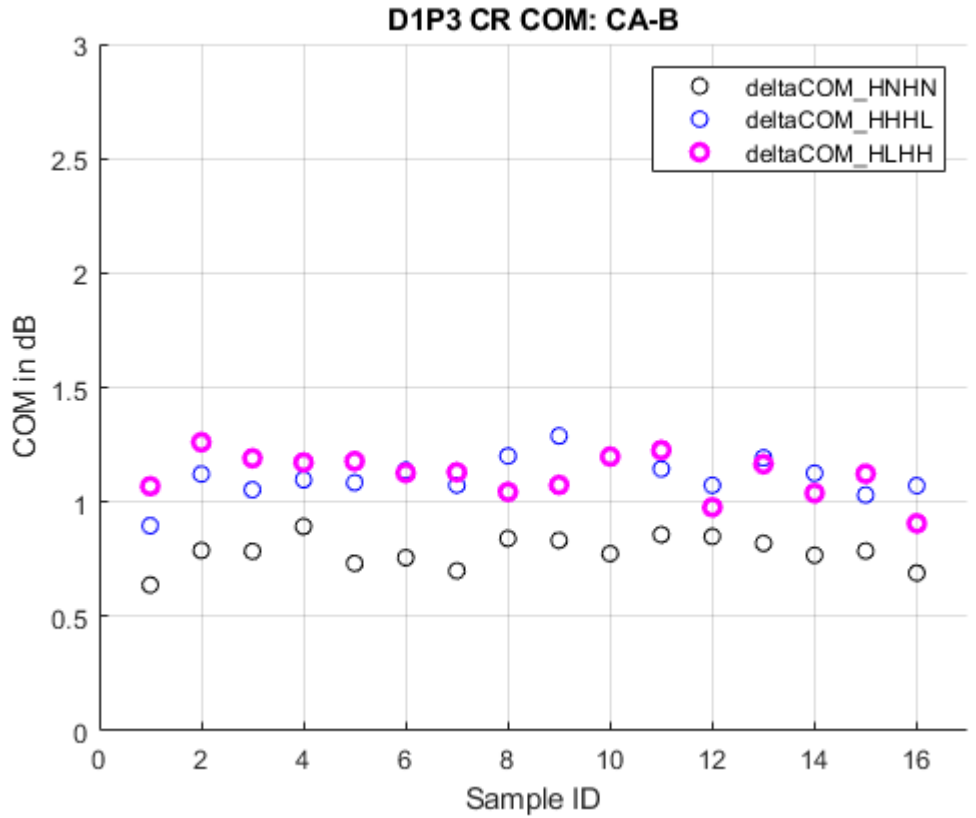
Supporting Data (CA-B)



C0 and C1 parameters changed, all other parameters remain same

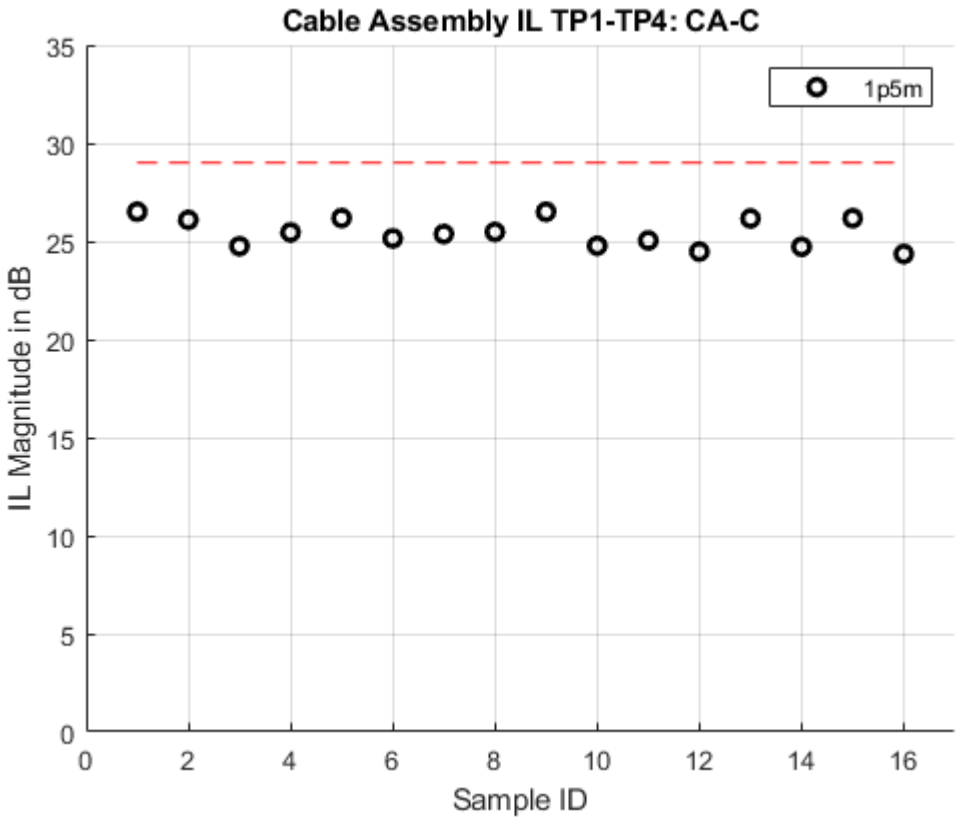
Supporting Data (CA-B)

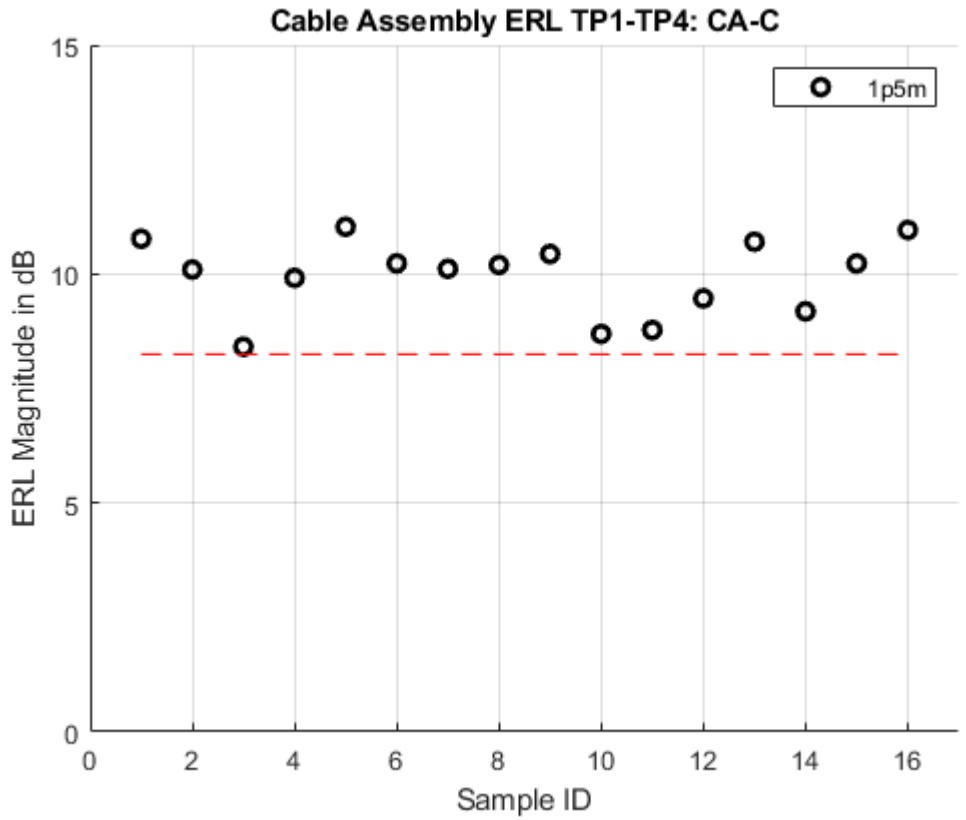




Delta COM is highest for the asymmetric cases

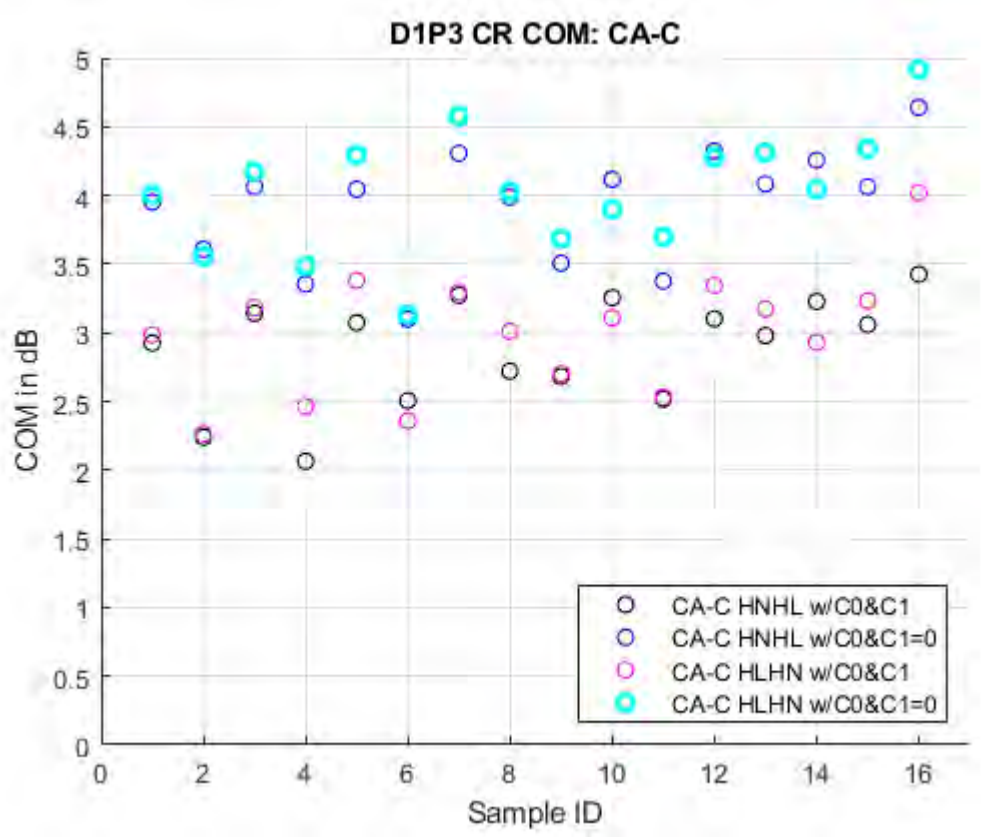
Supporting Data (CA-C)

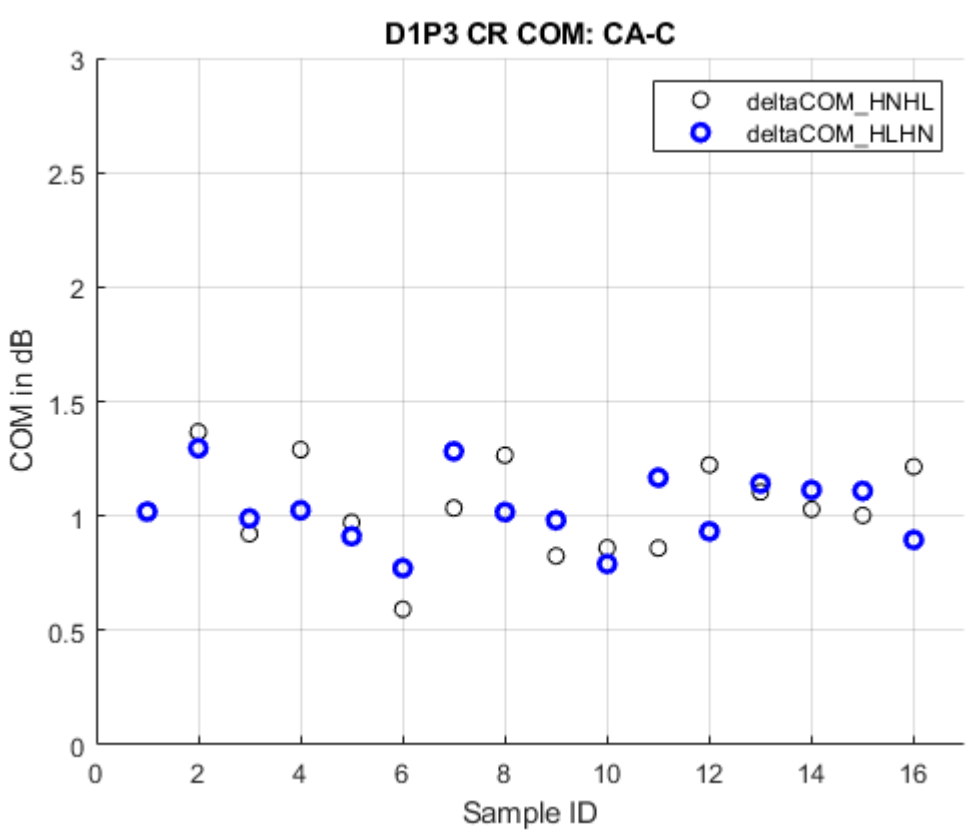




Nominal 1.5m measurements @TP1-TP4 across an entire port (octal)

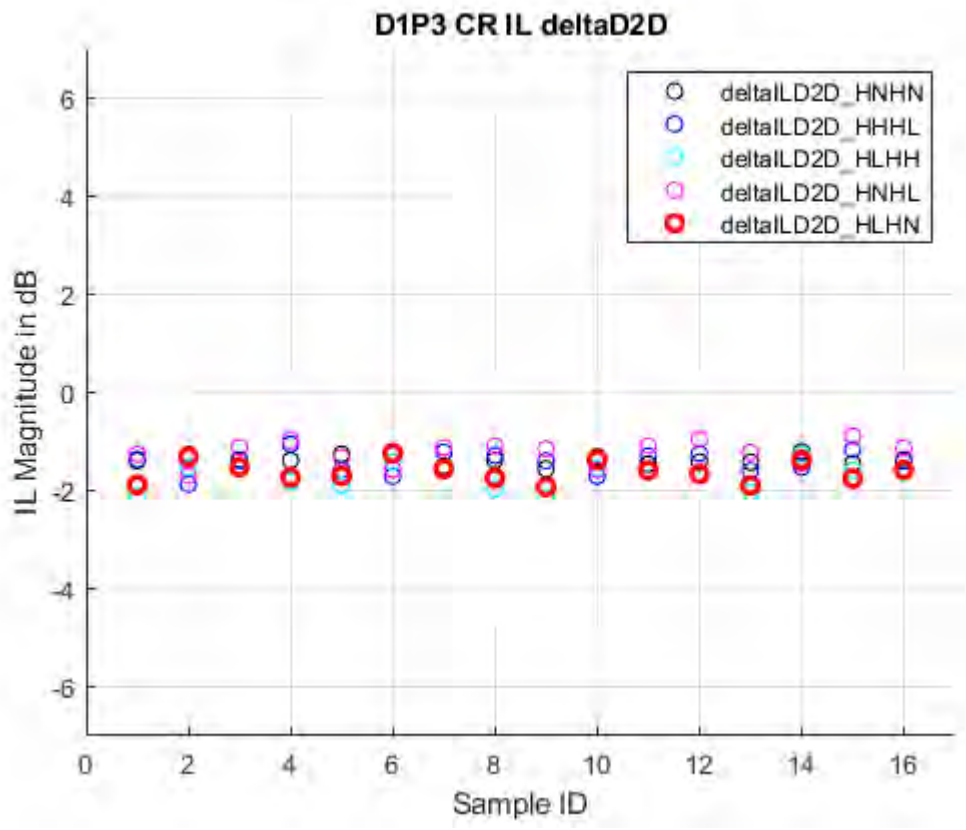
Supporting Data (CA-C)





Delta COM is trend is similar for physically longer CA types

Supporting Data (Conclusions)



The impact of C0 and C1 is not consistent across lanes

Changing C0 and C1 values will likely lead to a change for the partial host channel model parameters, *below*

Table 179–17—Partial host channel model parameters per Host class

Parameter	Host class			Units
	HL	HN	HH	
Package class	A	B	B	—
Package transmission line 1 length, $z_p^{(1)}$	8	15	45	mm
Partial host PCB transmission line length, $z_p^{(h)}$	9	70	60	mm

For cases where C0,C1=0, ILD2D is <40dB

Summary

- There are no cases where C0 and C1 “help” CR COM results
  - As defined in D1P3
- C0 and C1 are poorly defined in D1P3 and unequally stress CR (versus KR) and asymmetric (versus symmetric) test cases
- Further work needs to be done to determine the right allocations between package IL (mm), PCB IL (mm) for cases HL, HN, and HH
  - And continue to address more CA types, channel combinations, and settings
- **Propose to set C0 and C1 = 0 and let future drafts update other parameters as necessary, as written in comment 466**

Back-up

COM Configuration (v4.70)

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[46.25 46.25]	Ohm	[TX RX]
PKG_NAME	PKG_HiR_CLASS_CRHN PKG_HiR_CLASS_CRHN		TX RX
A_v	0.385	V	
A_fe	0.385	V	
A_ne	0.481	V	
z_p select	[1]		
L	4		
M	32		
filter and Eq			
f_r	0.55	*fb	
c(0)	1		min
c(-1)	0		[min:step:max]
c(-2)	0		[min:step:max]
c(-3)	0		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	0		[min:step:max]
N_b	1	UI	
b_max(1)	0.85		As/dffe1
b_max(2..N_b)	0		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	-0.15	S	As/dfe2..N_b
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	42.50	GHz	
f_p1	42.50	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
Butterworth	1	logical	include in fr

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\HNHN_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	w_Cx	
COM_CONTRIBUTION	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.005	
N	7000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	16	
fixture delay time	[0 0]	
Tukey_Window	1	
Z_t	46.25	Ohm
Noise, jitter		UI
sigma_RJ	0.01	UI
A_DD	0.02	V^2/GHz
eta_0	1.00E-08	dB
SNR_TX	33.5	
R_LM	0.95	

Table 93A–3 parameters			
Parameter	**Setting**	**Units**	Information
package_tl_gamma0_a1_a2	6e-4 0.00065 0.0003]		
package_tl_tau	0.006141	ns/mm	
package_Z_c	2 ; 70 70; 80 80; 100	Ohm	
z_p (TX)	1 11; 11 1 1 ; 0.5	mm	[test cases to run]
z_p (NEXT)	1 11; 11 1 1 ; 0.5	mm	[test cases]
z_p (FEXT)	1 11; 11 1 1 ; 0.5	mm	[test cases]
z_p (RX)	1 11; 11 1 1 ; 0.5	mm	[test cases]
C_p	[0.4e-4 0.4e-4]	nF	[test cases]
Operational			
ERL Pass threshold	10	dB	
COM Pass threshold	3	db	
DER_0	2.00E-04		
T_r	0.00400	ns	
FORCE_TR	1	logical	
PMD_type	C2C		
EW	1		
MLSE	1	logical	
ts_anchor	1		
sample_adjustment	[-16 16]		
Local Search	2		
Filter: Rx FFE			
ffe_pre_tap_len	6	UI	
ffe_post_tap_len	8	UI	
ffe_pre_tap1_max	0.7		
ffe_post_tap1_max	0.7		
ffe_tapn_max	0.7		
FFE_OPT_METHOD	MMSE		FV-LMS or MMSE
num_ui_RXFF_noise	4096		
Floating Tap Control			
N_bg	2	0 1 2 or 3 groups	
N_bf	4	taps per group	
N_f	80	UI span for floa	
bmaxg	0.2	max DFE value	
B_float_RSS_MAX	0.1	rss tail tap limi	
N_tail_start	9	(UI) start of tai	

SAVE_CONFIG2MAT	0		
Receiver testing			
RX_CALIBRATION	0	logical	
Sigma BBN step	5.00E-03	V	
ICN parameters			
f_v	0.565	Fb	
f_f	0.565	Fb	
f_n	0.565	Fb	
f_2	60.000	GHz	
A_ft	0.450	V	
A_nt	0.600	V	

Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 5.95e-4 2.6e-5]*	1.4 db/in @ 53.125G
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	92.5	Ohm
z_bp (TX)	*70*	mm
z_bp (NEXT)	*70*	mm
z_bp (FEXT)	*70*	mm
z_bp (RX)	*70*	mm
C_0	[2.9e-5 2.9e-5]	nF
C_1	[1e-5 1e-5]	nF
Include PCB	**1**	**logical**
Seletions (rectangle, gaussian,dual_rayleigh,triangle		
Histogram_Window_Weigh	gaussian	selection
Qr	*0.02*	UI

.START	PKG_HiR_CLASS_CRHN	[-] db	
Table 93A–3 parameters			
Parameter	**Setting**	**Units**	Information
package_tl_gamma0_a1_a2	[0.0005 0.00065 0.000293]		
package_tl_tau	0.006141	ns/mm	
package_Z_c	[87.5 87.5 ; 95 95 ; 100 100; 78 78]	Ohm	
R_d	[46.25 46.25]	Ohm	[TX RX]
z_p (TX)	[15 45 ; 2 2 ; 1.3 1.3 ; 1.5 1.5]	mm	[test cases]
z_p (NEXT)	[14 44 ; 2 2 ; 1.3 1.3 ; 1.5 1.5]	mm	[test cases]
z_p (FEXT)	[15 45 ; 2 2 ; 1.3 1.3 ; 1.5 1.5]	mm	[test cases]
z_p (RX)	[14 44 ; 2 2 ; 1.3 1.3 ; 1.5 1.5]	mm	[test cases]
C_p	[0.4e-4 0.4e-4]	nF	[TX RX]
A_v	[0.385 0.385]	V	Vf=0.400
A_fe	[0.385 0.385]	V	Vf=0.399
A_ne	[0.481 0.481]	V	Vf=0.400
.END			

Background

- https://www.ieee802.org/3/dj/public/24_07/motions_3dj_2407.pdf

Straw Poll #TF-5

I would support the approach presented in ran_3dj_01b_2407, of having a specific combination of package and PCB length per CR host class

A: Yes, with the original PCB parameters in the presentation (per ran_3dj_01b_2407, slides 13-15)

B: Yes but with modified PCB parameters to create 1.1 dB/inch (per ran_3dj_01b_2407, slides 23-25)

C: No

D: Abstain

(choose one)

Results (all): A: 8, B: 18, C: 25, D: 42

Background

- https://www.ieee802.org/3/dj/public/24_07/motions_3dj_2407.pdf

Straw Poll #TF-6

For the CR host channel model, I would prefer the combination of package and PCB length as follows:

A: Shorter package trace and longer PCB trace, with C0 = 0 (similar to option 1 in ran_3dj_01b_2407)

B: Longer package trace and shorter PCB trace, with C0 = 0 (similar to option 2 in ran_3dj_01b_2407)

C: Shorter package trace and longer PCB trace, with C0 > 0 (similar to option 3 in ran_3dj_01b_2407)

D: Longer package trace and shorter PCB trace, with C0 > 0 (similar to option 4 in ran_3dj_01b_2407)

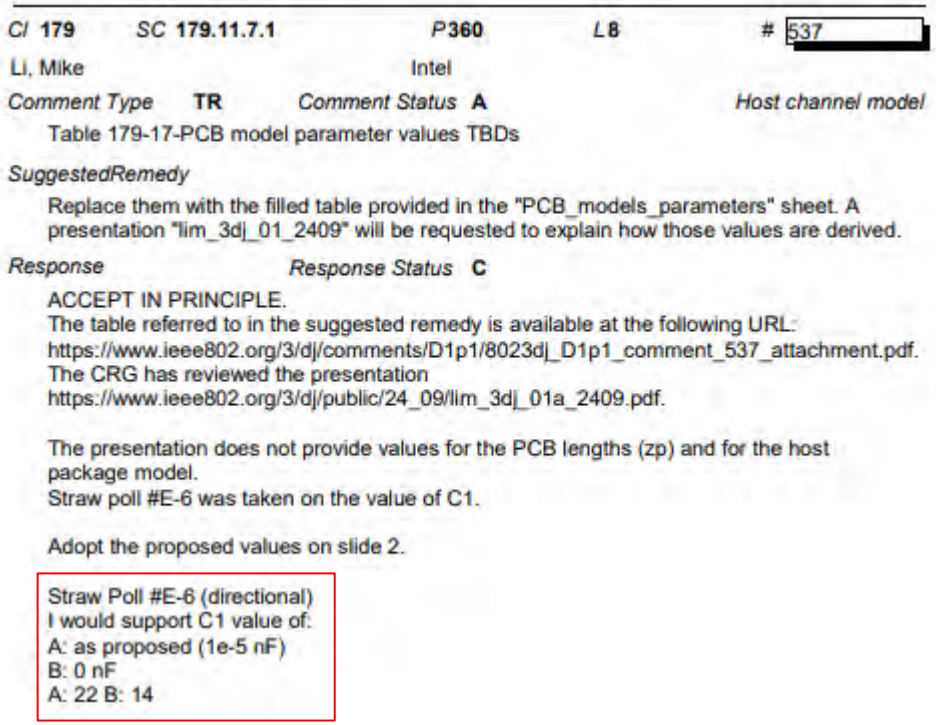
E: Abstain

(chicago rules)

Results(all): A: 14, B: 23, C: 26, D: 18, E: 59

Background

- https://www.ieee802.org/3/dj/comments/D1p1/8023dj_D1p1_comments_final_clause.pdf



Cl 179 SC 179.11.7.1 P360 L8 # 537

Li, Mike Intel

Comment Type TR Comment Status A Host channel model

Table 179-17-PCB model parameter values TBDs

SuggestedRemedy

Replace them with the filled table provided in the "PCB_models_parameters" sheet. A presentation "lim_3dj_01_2409" will be requested to explain how those values are derived.

Response Response Status C

ACCEPT IN PRINCIPLE.
The table referred to in the suggested remedy is available at the following URL:
https://www.ieee802.org/3/dj/comments/D1p1/8023dj_D1p1_comment_537_attachment.pdf.
The CRG has reviewed the presentation
https://www.ieee802.org/3/dj/public/24_09/lim_3dj_01a_2409.pdf.

The presentation does not provide values for the PCB lengths (zp) and for the host package model.
Straw poll #E-6 was taken on the value of C1.

Adopt the proposed values on slide 2.

Straw Poll #E-6 (directional)
I would support C1 value of:
A: as proposed (1e-5 nF)
B: 0 nF
A: 22 B: 14

https://www.ieee802.org/3/dj/public/24_09/lim_3dj_01a_2409.pdf