Addressing Clause 185 comments against D1.3 for 800GBASE-LR1

(Support contribution for Comments #474, 475)

Kishore Kota – Marvell

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Comment #474

Cl **185** *SC* **185.6.1** *P* **551** *L* **5** # 474

Kota, Kishore — Marvell Semiconductor

Comment Type **TR** *Comment Status* **X**

"Tx clock phase noise: phase noise mask frequency (max)" is an ill-defined spec in table 185.5. Unlike previous coherent interfaces 800GBASE-LR1 clocking on the line interface is derived from the upper layers. Without a clear spec on the phase noise of those layers, it is not possible to design to the specified phase noise mask at the 800GBASE-LR1 interface. Section 185.5.13 is also related to this spec.

SuggestedRemedy

No equivalent transmit clock phase noise mask specification is present in any of the prior IMDD clauses such as Clause 124. Recommendation is to delete this spec. Presentation to be provided.

Proposed Response *Response Status* **O**

Comment #474: Background

- 800GBASE-LR1 PCS and FEC sublayers clocking differs from all prior coherent line interfaces such as 400ZR or 800ZR
  - 400ZR/800ZR line interfaces use a clock which is asynchronous to the host interface – GMP is used to transfer data across the asynchronous clock interface
  - 800GBASE-LR1 line interface uses a synchronous clock derived from the higher layers similar to PAM4 interfaces
- Table 185-5 in D1.3 document defines a “TX clock phase noise: phase noise mask frequency (max)” specification which imposes a phase noise mask on the clock used to transmit the 800GBASE-LR1 signal
  - Since the clock is derived from the upper layers, this specification requires a well-defined phase noise requirement from upper layers. No such specification currently exists in any of the adjacent layers such as Annex 120F or Annex 120G
  - For e.g., Annex 120F specifies Jrms (max), J4u (max), J4u03(max) but not a phase noise mask

Comment #474: Proposed remedy

- Clause 185 defines a coherent PMD which is similar to other PAM4 PMDs (e.g. Clause 124)
- No equivalent specification is present in any of the similar clauses which derive clocking from upper layers
- Proposal is to delete the “TX clock phase noise: phase noise mask frequency (max)” specification from Table 185-5

Comment #475

Cl **185A** *SC* **185A.2.3** *P* **842** *L* **22** # 475

Kota, Kishore — Marvell Semiconductor

Comment Type **TR** *Comment Status* **X**

The offline digital signal processing described in this section is missing a post-equalizer after the "carrier phase recovery" block which is required to allow relaxation of the TX I-Q skew to the 0.75ps spec in Table 185-5.

SuggestedRemedy

Add post-equalizer stage to the digital signal processing. Presentation to be provided.

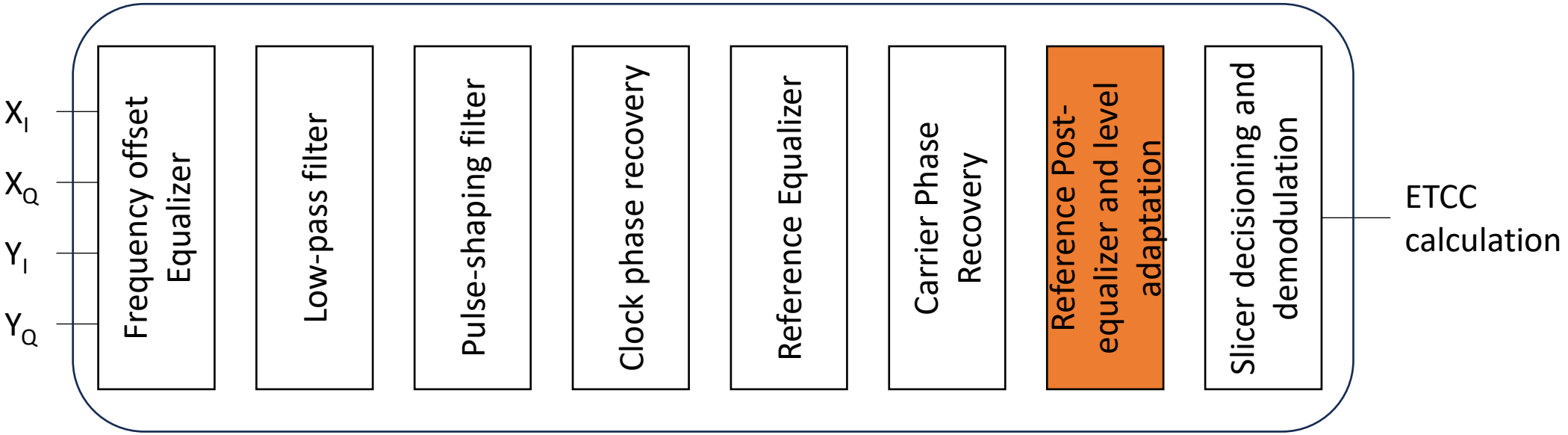
Proposed Response *Response Status* **O**

Comment #475: Background

- Table 185-5 includes a “I-Q quadrature skew (max)” specification of 0.75ps
  - This specification corresponds to 0.093UI normalized to the symbol period of 800GBASE-LR1
  - Specifications from prior generation coherent interfaces such as the OIF 400ZR IA had a tighter requirement of 0.045UI.
  - The relaxation envisioned by this specification requires the use of a post-equalizer after carrier recovery and this block is required in the reference DSP processing described in Section 185A.2.3 and shown in Fig 185A-4. See kota_3dj_02_2407 Slide 14 for an example.

Comment #475: Proposed Remedy

- Add a post-equalizer stage to Fig 185A-4.



Thank you!