Error ratio for coherent PHY types Draft 1.4 comments 16, 115, 117, 118

Matt Brown, Alphawave Semi

Supporters

- Adee Ran, Cisco

Introduction

- Addresses Draft 1.4 comments 115, 117, and 118 related to the 800GBASE-LR1 Inner FEC PRBS31 generator and checker, including adding block error checking to the checker.
- Addresses Draft 1.4 comments 16 related to the allocation of error ratios for an 800GBASE-ER1/ER1-20 Physical Layer implementation.

Part 1

PRBS31 test pattern and block error ratio for 800GBASE-LR1

Comments 115, 117, 118

Comments

Cl **184** *SC* **184.4.3** *P* **520** *L* **25** # 118

Brown, Matt — Alphawave Semi

Comment Type **T** *Comment Status* **X**

A PRBS31 test pattern generator was added in D1.4. It is defined as being optional. However, this test pattern can be used for block error ratio measurements as defined for PAM4 PMDs and AUIs.

SuggestedRemedy

Change: "The Inner FEC may optionally include a PRBS31"
To: "The Inner FEC shall include a PRBS31"

Proposed Response *Response Status* **O**

Cl **184** *SC* **184.5.10** *P* **530** *L* **49** # 115

Brown, Matt — Alphawave Semi

Comment Type **T** *Comment Status* **X**

A PRBS31 test pattern checker was added in D1.4. It is defined as being optional. However, this test pattern can be used for block error ratio measurements as defined for PAM4 PMDs and AUIs in 176.7.4.

SuggestedRemedy

Change "The Inner FEC may optionally include"
To "The Inner FEC shall include"
Add the follow text: "The PRBS31 checker includes block error detection and counters as specified in 176.7.4.7."

Proposed Response *Response Status* **O**

Cl **185** *SC* **185.2** *P* **542** *L* **39** # 117

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Comment Type **T** *Comment Status* **X**

Other comments propose that with the addition of the PRBS31 generator and checker in the 800GBASE-LR1 Inner FEC it is now possible to assess the quality detected signal using block error counters similar to the method for PAM4 PMDs and AUIs as defined in 174A.7.1.

SuggestedRemedy

Update the specification for a PMD receiver in 185.2 accordingly.
Provide test configuration and method in 174A.
A contribution will be provided.

Proposed Response *Response Status* **O**

For this Inner FEC, the interface to the sublayer above is 32 PCS lanes, i.e., not one lane per PMD lane.
Implement block error counters on the PMA would require 32 instances and they'd all have to be convolved together.

Single PRBS31 pattern generator here

The pattern from a single generator is round-robin distributed to each of the 32 FEC flows.

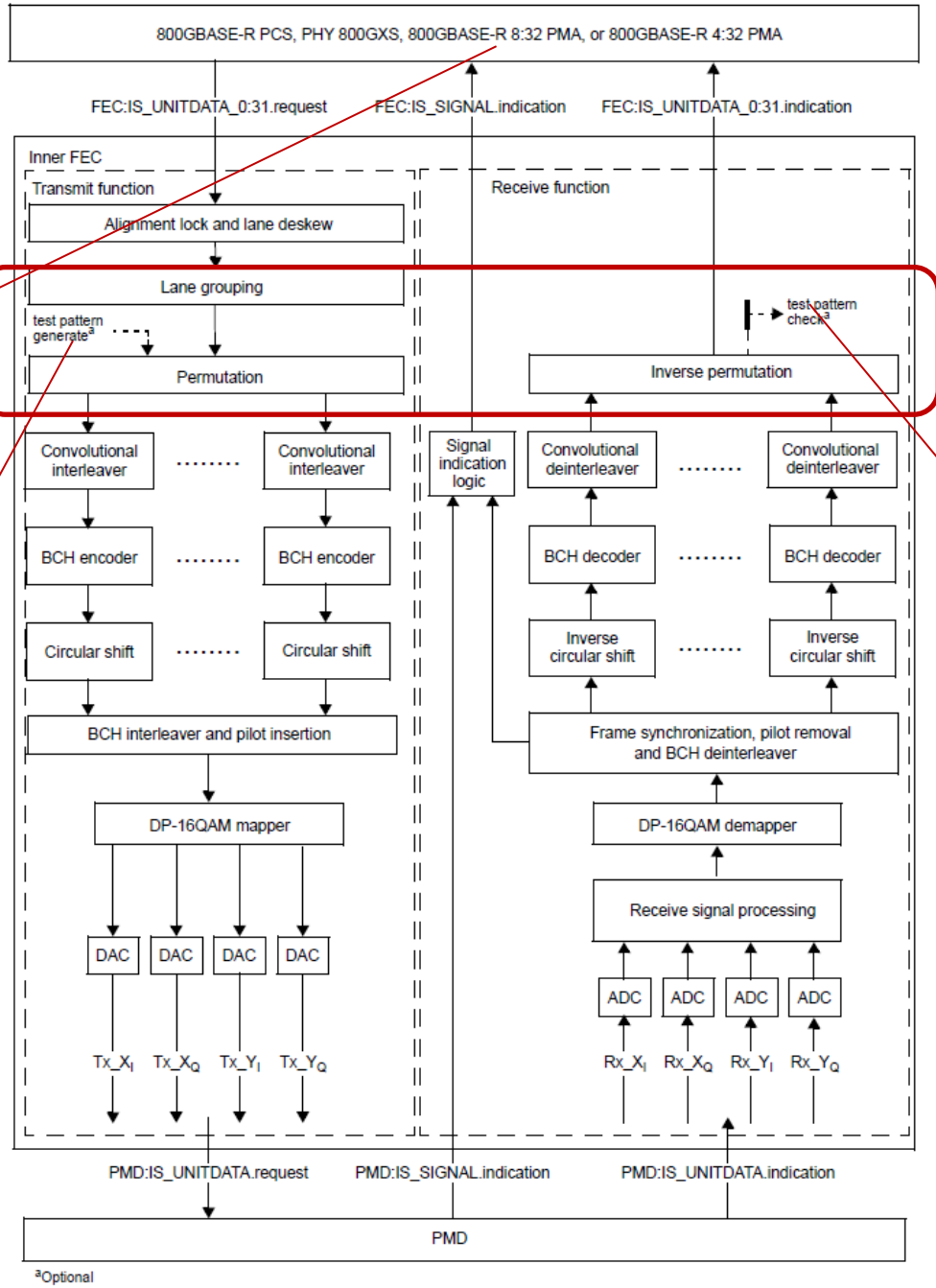

Figure 184–2—Inner FEC functional block diagram

Single PRBS31 pattern checker here

The pattern from 32 FEC flows is reassembled then processed by the checker.

Corresponds well to the single optical lane.

Proposed changes 1

Change 184.4.3 and 184.5.10 as follows…

184.4.3 Test pattern generator

The Inner FEC ~~may optionally~~ shall include a PRBS31 test pattern generator (see Figure 184–2). In test mode, 10-bit blocks from the PRBS31 generator are round-robin distributed to the 32 pcsla Inner FEC flows.

The PRBS31 generator implements the free-running PRBS31 pattern defined by Equation 49–2 and shown in Figure 49–9.

If supported the test pattern generator is enabled by the tx_generator_enable control variable.

…

184.5.10 Test pattern checker

The Inner FEC ~~may optionally~~ shall include a PRBS31 test pattern checker over the inverse permutation output PCS lanes (see 184.4.3). To recover the PRBS31 test pattern, 10-bit blocks are round-robin collected from the 32 inverse permutation function output flows.

If supported the test pattern checker is enabled by the rx_checker_enable control variable.

Each PRBS31Q test pattern checker shall include block error detection and 17 related counters. Block error detection and behavior of the counters is defined in 174A.7.

The following counters shall be implemented:

test_block_error_bin_0_*k*

A set of 16 48-bit counters where counter *k* counts once for each test block received with exactly *k* errored test symbols, *k* = 0 to 15.

test_block_error_bin_*0*_16p

A 48-bit counter that counts once for each test block received with 16 or more errored test symbols.

Proposed changes 2

Add the new counters (based on Table 176-9) to Table 184-5 as follows:

Status variable	Variable reference	MDIO register/bit number	MDIO register/bit reference
…	…	…	…
test_block_error_bin_0_<0:15>	184.5.10	1.2600 to 1.2647	45.2.1.213n
test_block_error_bin_0_16p	184.5.10	1.2648 to 1.2650	45.2.1.213n
…	…	…	…

Proposed changes 3

Add new test methods for the 800GBASE-LR1 PMD ISL, based on methods in 174A.7, after 174A.7 as follows…

174A.x Error ratio tests for 800GBASE-LR1 ISLs

This subclause defines test methods for an ISL (see 178B.3) with 800 Gb/s per lane signaling between a pair of 200GBASE-LR1 Inner FEC sublayers including a PMD and Inner FEC at each end and the medium between.

These tests are based on those defined in 174A.7.

174A.x.1 Block error ratio test methods using Inner FEC measurements

174A.x.1.1 Inner FEC block error ratio test configuration

Test configuration for an 800GBASE-LR1 ISL is illustrated in Figure 174A–x.

<Include figure from following slide>

174A.x.1.2 Inner block error counters

The block counters are defined in 174A.7.1.2 with the number of lanes $p = 1$.

174A.x.1.3 Inner FEC error histogram measurement

Error histograms are measured according 174A.7.1.3.

174A.x.1.4 Inner FEC error mask test method using Inner FEC measurements

Conformance using an error histogram mask is defined in 174A.7.1.5 for a single lane (p = 1).

174A.x.1.5 Block error ratio method for using Inner FEC measurements

Conformance using block error ratio is defined in 174A.7.1.6 for a single lane (p = 1).

The expected block error ratio is met if the measured value is less than the codeword error ratio limit specified in 174A.4 for a PHY-to-PHY link.

Update other text in 174A to align, as necessary.

Proposed changes 4

Add new test configuration diagram in 174A.x.1.1

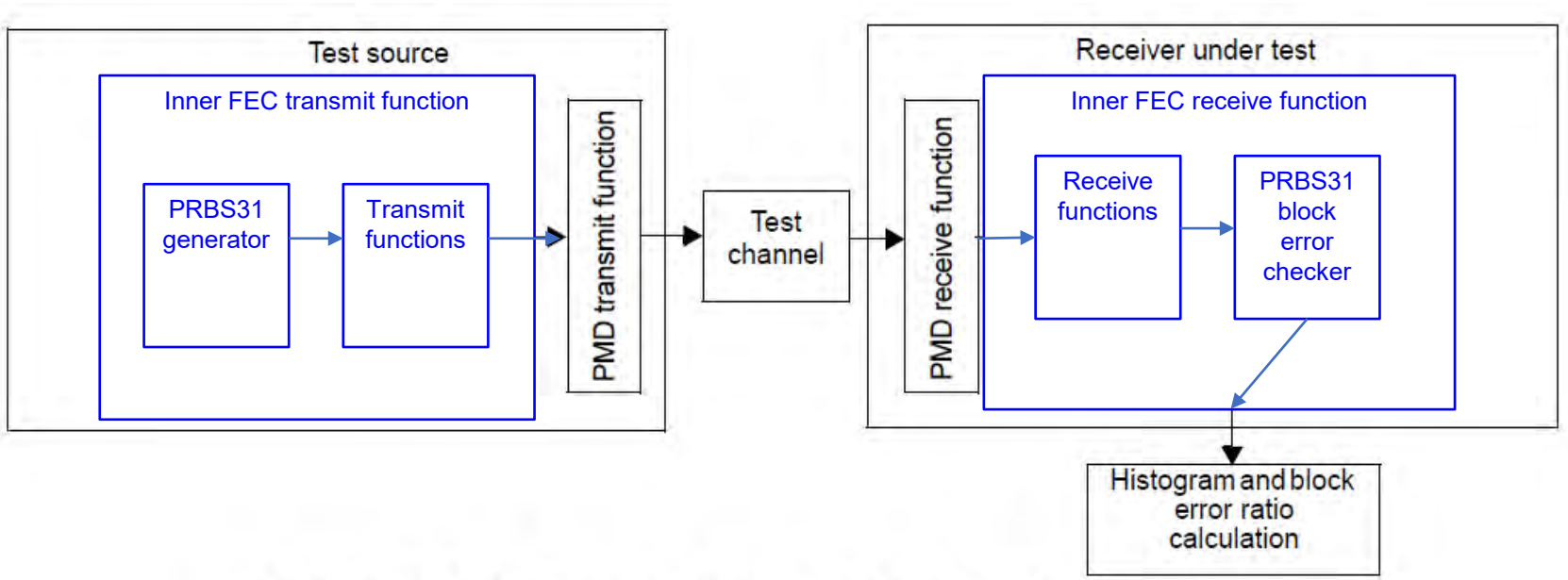

Figure 174A–X—Test configuration for 800GBASE-LR1 PMD

Proposed changes 5

Change 185.2 as follows…

185.2 Error ratio allocation

A complete PHY is expected to meet the frame loss ratio specifications in 174A.5.

A PHY receiver is expected to meet the block error ratio specifications in 174A.8, measured at the PCS, with BER_{added} equal to 3.2×10^{-5}.

A PMD receiver is expected to meet the block error ratio specifications in 174A.~~8~~x, measured at the ~~PCS~~ Inner FEC, with BER_{added} equal to 6.4×10^{-5}.

Part 2

Error ratio allocation for 800GBASE-ER1/ER1-20

Comments 16

Comments

Cl **174A** *SC* **174A.6** *P* **662** *L* **31** # 16

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Comment Type **T** *Comment Status* **X**

CRC error ratio based on 6E-11. However, this would not account for an Extender plus a pair of AUIs in the PHY. Options:
(a) disallow extender
(b) state that either extender or AUIs in PHY, but not both
(c) reduced FLR for PCS-to-PCS to 5.8E-11.

SuggestedRemedy

A contribution will be provided.

Proposed Response *Response Status* **O**

Other options:

(d) leave allocations as they are but add a note pointing out that the sum of FLR for the xMII Extender plus the RS-FEC path are unlikely to exceed the allocation for the xMII Extender of 0.1E-11 if compliant AUIs are used.

(e) allocate 0.5E-11 FLR to all xMII Extenders and to RS-FEC path in segmented PHYs like 800GBASE-ER1/ER1-20.

Comments

Error ratio allocations for 800GBASE-ER1/ER1-20 PHY types…

187.2 Error ratio allocation

A PHY receiver is expected to meet the frame loss ratio specifications in 174A.4.

A PHY receiver is expected to meet the CRC error ratio specified in 174A.6.

174A.3 Error ratio allocation for an Ethernet network path

Error ratio allocation of the path between two Ethernet DTEs is defined in terms of the frame loss ratio from the PLS service interface of the Reconciliation Sublayer (RS) of the transmitting DTE to the PLS service interface of the RS of the receiving DTE.

The frame loss ratio for 64-octet MAC frames with minimum interpacket gap is expected to be less than 6.2×10^{-11}.

NOTE—The frame loss ratio is affected by multiple components along the network path and is not a normative requirement of a specific component.

174A.4 Error ratio allocation for an xMII Extender

This subclause defines the error ratio allocation for a 200GMII, 400GMII, 800GMII, or 1.6TMII Extender (see Clause 118 and Clause 171).

Error ratio allocation of the xMII Extender is defined in terms of the frame loss ratio between the transmitting XS (DTE or PHY) and the receiving XS (PHY or DTE, respectively).

The frame loss ratio for 64-octet frames with minimum interpacket gap is expected to be less than 10^{-12}. This is equivalent to a FEC codeword error ratio (see 174A.9) lower than 2.4×10^{-13}. If the errors at the input of the RS-FEC are uncorrelated, this is equivalent to a pre-correction BER (BER_{total}) of 2.21×10^{-4}.

NOTE—The frame loss ratio is affected by multiple components within the xMII Extender and is not a normative requirement of a specific component.

174A.5 Error ratio allocation for a PHY-to-PHY link

Error ratio allocation of a PHY-to-PHY link is defined in terms of the frame loss ratio between the service interfaces of the transmitting PCS and the receiving PCS.

The frame loss ratio for 64-octet MAC frames with minimum interpacket gap is expected to be less than 6×10^{-11}.

For PHYs using the 200GBASE-R, 400GBASE-R, 800GBASE-R, or 1.6TBASE-R PCS, the expected frame loss ratio is equivalent to an FEC codeword error ratio (see 174A.9), as measured at the PCS, of less than 1.45×10^{-11}. If the errors at the input of the RS-FEC are uncorrelated, this is equivalent to a pre-correction BER (BER_{total}) of 2.92×10^{-4}.

NOTE—The frame loss ratio is affected by multiple components within the PHYs and by the medium, and is not a normative requirement of a specific component.

174A.6 Error ratio allocation for an FEC-to-FEC link

Error ratio allocation of an FEC-to-FEC link, for PHYs that include a segmented FEC sublayer (see 169.2.4c), is defined in terms of the frame loss ratio between the service interfaces of the transmitting FEC and the receiving FEC for FEC sublayers which fully terminate the FEC.

The frame loss ratio for 64-octet MAC frames with minimum interpacket gap is expected to be less than 6×10^{-11}.

For PHYs using the 800GBASE-ER1 FEC, the expected frame loss ratio is equivalent to a CRC error ratio (see 174A.9) of less than 5.903×10^{-11}. If the errors at the input of the FEC are uncorrelated, this is equivalent to a pre-correction BER (BER_{total}) of 2×10^{-2}.

Current error ratio budgets

Table 174A–1—Error ratio allocations for optical PHYs

ISL	Frame loss ratio for entire PCS-to-PCS link	Codeword error ratio for entire PCS-to-PCS link	BER for entire PCS-to-PCS link (BER_{total})	BER per ISL [a]
xAUI-n C2C[b]	6×10^{-11}	1.45×10^{-11}	2.92×10^{-4}	0.08×10^{-4}
xAUI-n C2M				0.24×10^{-4}
PMD-to-PMD				2.28×10^{-4}
xAUI-n C2M				0.24×10^{-4}
xAUI-n C2C[b]				0.08×10^{-4}

[a] Measured at the PMA closest to the PMD or AUI component and after Inner FEC decoding, if present.
[b] If the PMD is a type defined in Clause 180, Clause 181, Clause 182, or Clause 183 (i.e., 200 Gb/s per lane), and xAUI-n C2C is a type defined in Annex 120D (i.e., 50 Gb/s per lane) or Annex 120F (i.e., 100 Gb/s per lane), the xAUI-n C2C is expected to meet the BER allocations in this table.

Table 174A–3—Error ratio allocations for xMII Extenders

ISL	Frame loss ratio for entire XS-to-XS link	Codeword error ratio for entire XS-to-XS link	BER for entire XS-to-XS link (BER_{total})	BER per ISL [a]
xAUI-n C2C	0.1×10^{-11}	2.4×10^{-13}	2.21×10^{-4}	0.1×10^{-4}
xAUI-n C2M				0.24×10^{-4}

[a] Measured at the PMA closest to the AUI component.

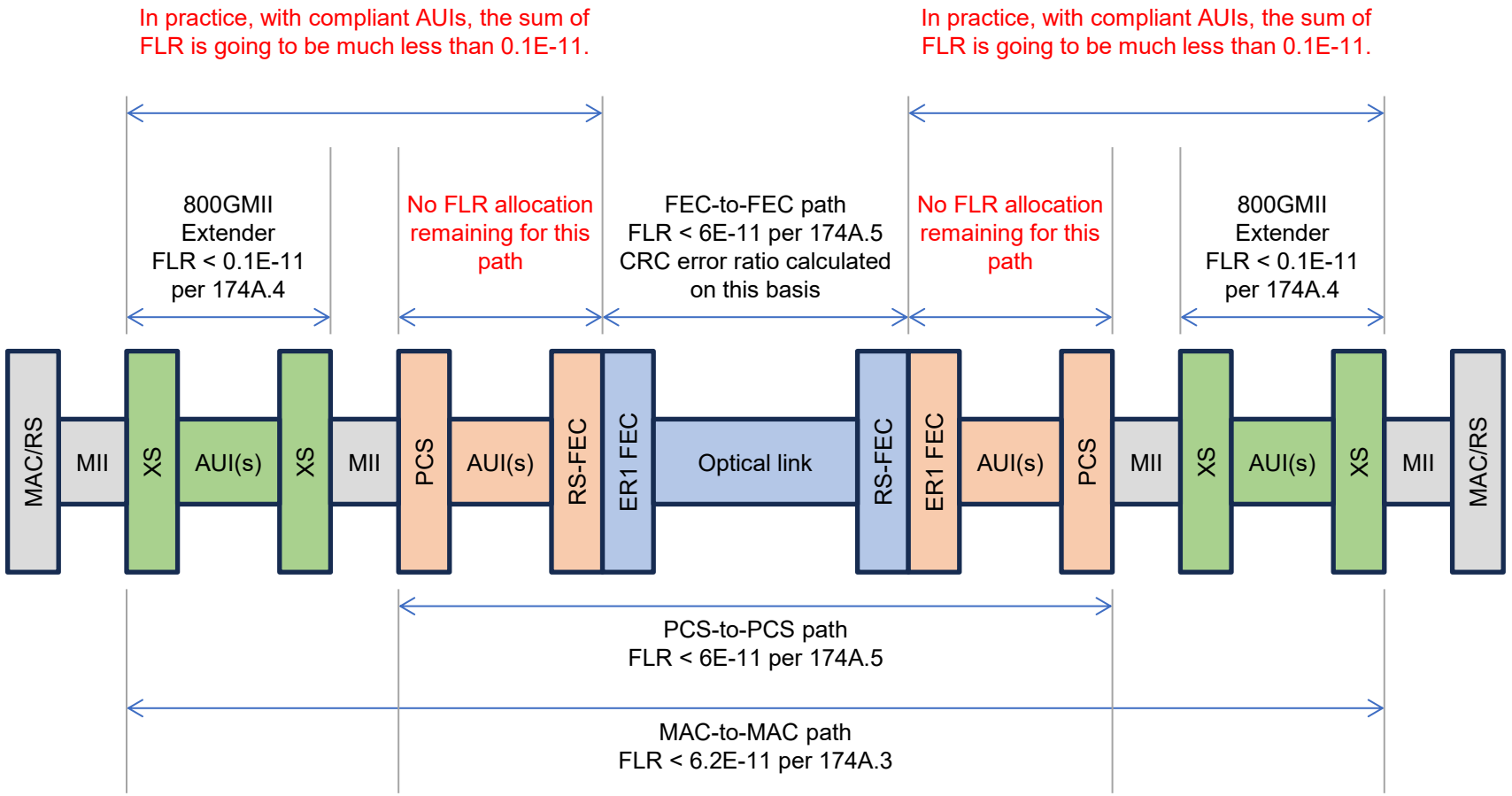
Not accurate. This table is for optical PHYs with concatenated Inner FEC. This table does not apply to optical PHYs with a segmented FEC, like 800GBASE-ER1/ER1-20.

Footnote b is also relevant to the 800GBASE-LR1 PHY. Should fix this.

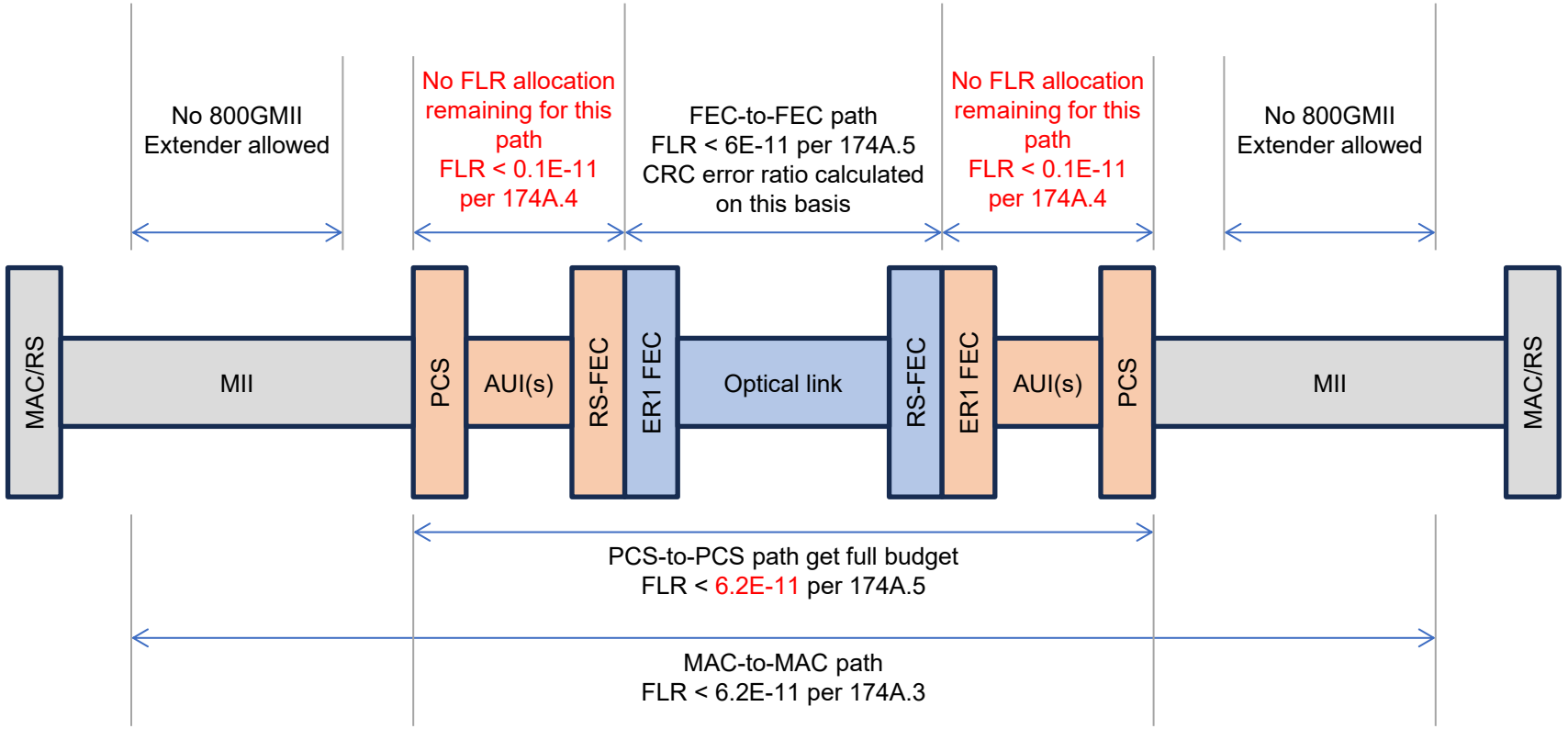
There is ample margin in the xMII extender budget that might be shared between the xMII extender and the RS-FEC to RS-FEC path on the PHY.

For random BER of 0.34E-4, FLR of 2.5E-25 can be supported on each path. Therefore in practice, with compliant AUIs, the sum of FLR for the xMII Extender and the RS-FEC path will be far below 0.1E-11.

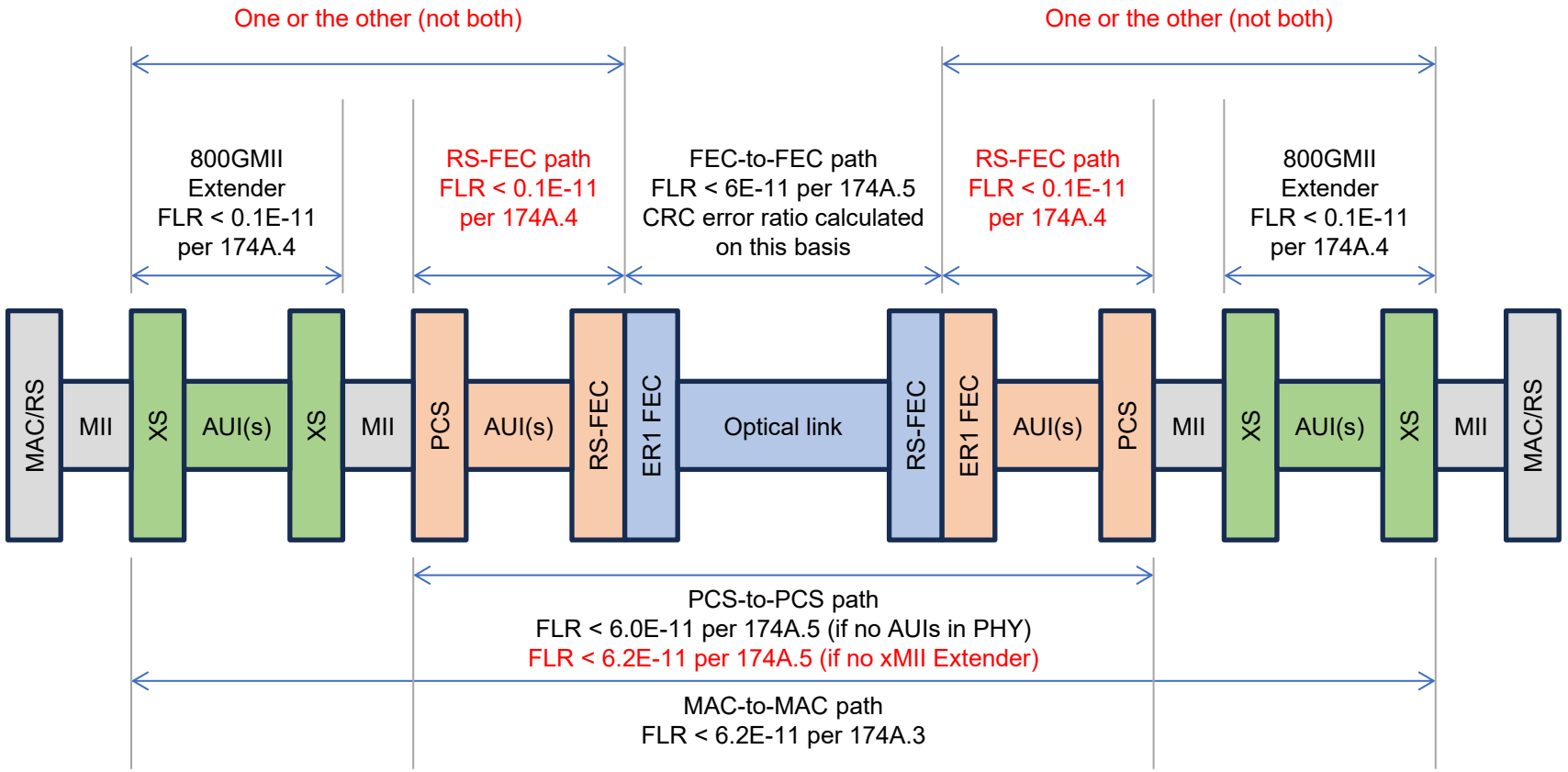
Draft 1.4 error ratio allocations for 800GBASE-ER1/ER1-20 Physical Layer Implementations



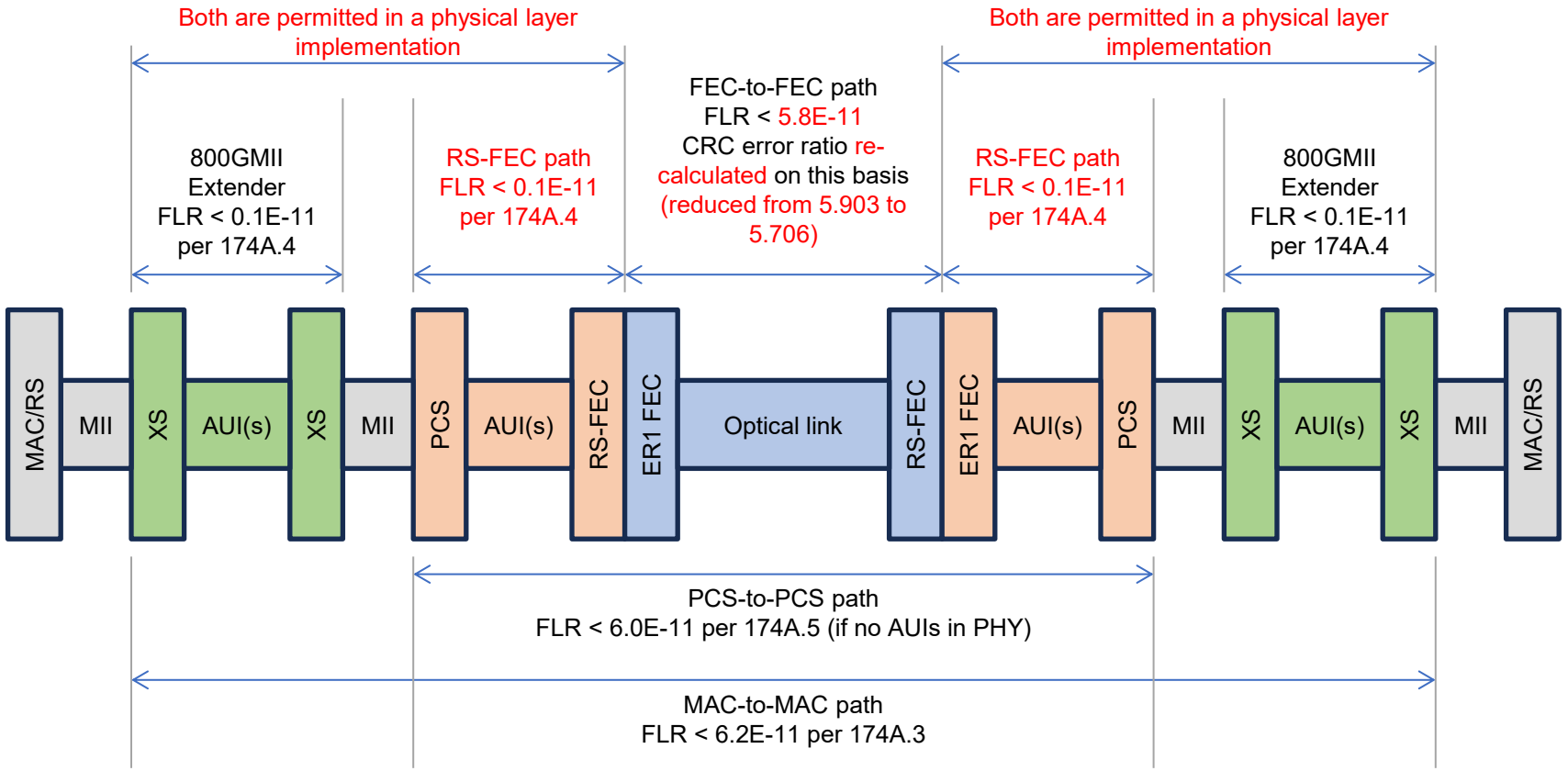
Option #1: No Extenders allowed.



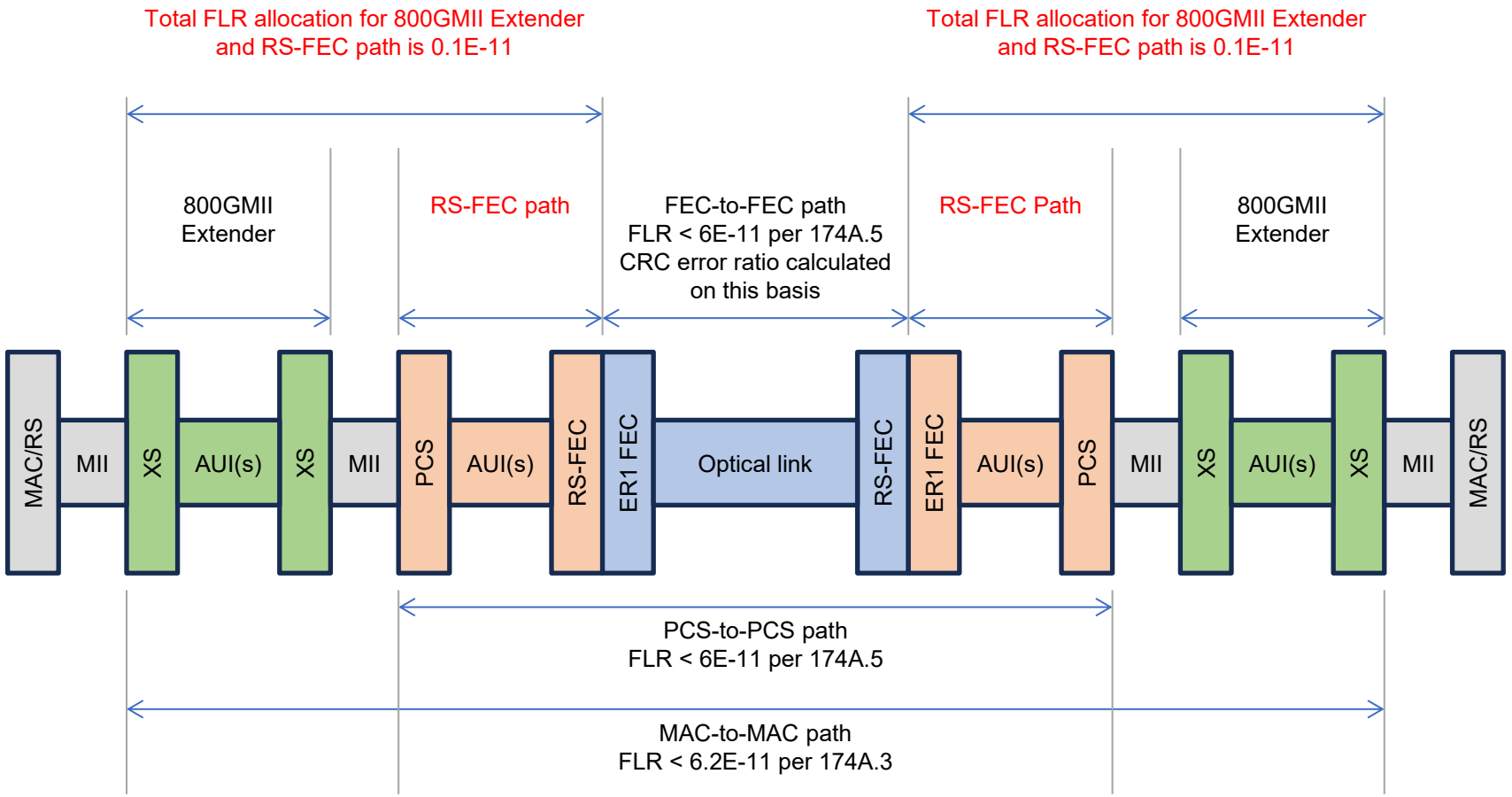
Option #2: Allow either AUIs in the PHY or Extender, but not both



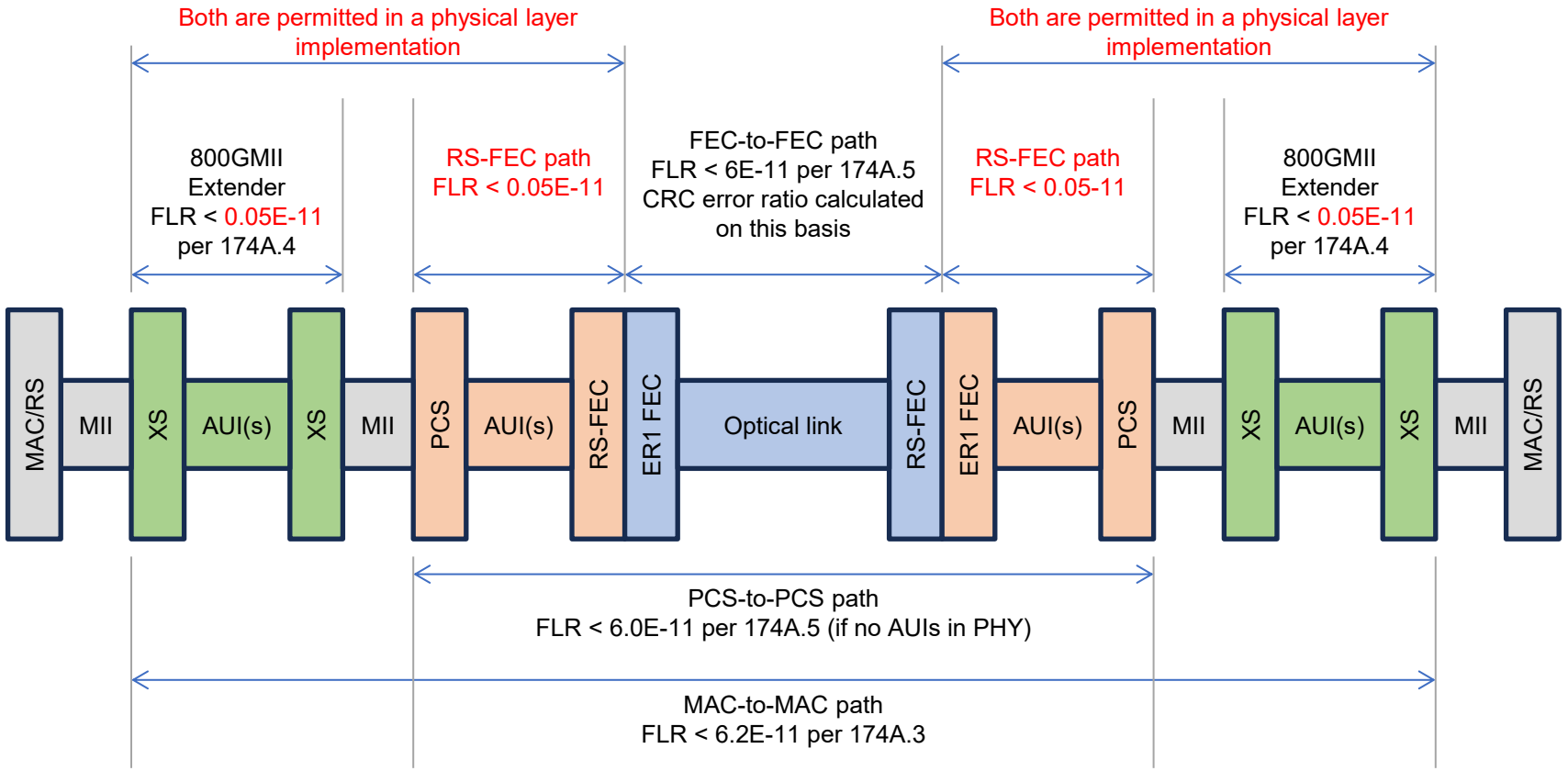
Option #3: Reduce FLR option for ER1 FEC path



Option #4: add a note that the FLR allocation for the xMII Extender can be shared with the RS-FEC path



Option #5: Reduce xMII allocation in half (for all PHY types) and allocate same to RS-FEC path



Thanks