802.3dj D1.4 Comment Resolution Common Track

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Introduction

- This slide package was assembled by the 802.3dj editorial team to provide background and detailed resolutions to aid in comment resolution.
- Specifically, these slides are for the various common track comments.

Error ratio

Comments 132, 133, 155

Error ratio
Comment #155

Cl **180** *SC* **180.2** *P* **418** *L* **37** # 155

Mi, Guangcan — Huawei Technologies Co., Ltd

Comment Type **TR** *Comment Status* **D** *Block error ratio*

In this revision, the block error ratio spec is said to define the PMD receiver or the PHY receiver spec. I am having second thought about this.

The error ratio of an optical PMD/PHY is not met or defined by a receiver only. It must have a transmitter or receiver input signal. It seems odd to say " a PMD receiver is expected to meet the block error ratio…..", without specifying the PMD/PHY transmitter condition.

The same applies to all other optical PMD clauses.

SuggestedRemedy

This reference of receiver seems meant to relate to the testing setup and definition in CL174A. A possible easy way to make the text more clear is to add some text describing the input signal condition. For example,"under optical transmitter signal compliant to this specification".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Change the text in 180.2 to the following...
With a compliant input signal, a PMD receiver is expected to meet the block error ratio specifications in 174A.7, measured at the PMA adjacent to the PMD, with BERadded equal to 6.4 × 10–5.
With a compliant input signal, a PHY receiver is expected to meet the block error ratio specifications in 174A.8, measured at the PCS, with BERadded equal to 3.2 × 10–5.
Make similar changes in clause 180 through 183, 185, 187, 176C, 176D.

180.2 Error ratio allocation

A complete PHY is expected to meet the frame loss ratio specifications in 174A.5.

A PMD receiver is expected to meet the block error ratio specifications in 174A.7, measured at the PMA adjacent to the PMD, with BER_{added} equal to 6.4×10^{-5}.

A PHY receiver is expected to meet the block error ratio specifications in 174A.8, measured at the PCS, with BER_{added} equal to 3.2×10^{-5}.

This comment expresses concern that the PHY and PMD receiver error ratio expectations in 180.2, etc., are not sufficiently defined. Need to define the expectation at the input.

The posted proposed responses addresses by also pointing out that this is with a compliant input signal.

This should also apply to clauses 178 and 179.

Error ratio
Comment 132

Cl 178 SC 178.2 P 344 L 1 # 132

Dudek, Mike Marvell

Comment Type T *Comment Status* D *error ratio*

It is very convoluted to find what the block error ratio specification is from the reference to 174A.7

SuggestedRemedy

Change "A PMD receiver is expected to meet the block error ratio specifications in 174A.7, measured at the PMA adjacent to the PMD, with BERadded equal to 1.6 × 10−5." to A PMD receiver is expected to meet the block error ratio of 1.45e-11 as described in 174A.7, measured at the PMA adjacent to the PMD, with BERadded equal to 1.6 × 10−5." Make the equivalent change in clauses 179 to 183 and annexes 176C and 176D. (Note the required block error ratio is the same value of 1.45e-11 for all these clauses and annexes)

Proposed Response *Response Status* W

PROPOSED ACCEPT IN PRINCIPLE.
The comment and suggested remedy have merit, but the details should be presented.
For CRG discussion.

Summary: The comment notes that D1.4 it is difficult to find the block error ratio specification from the reference to **174A.7**.
The suggested remedy is to add the value 1.45e-11 to the text in 178.2 and corresponding subclauses in other PMDs.

(Note: the specific value 1.45e-11 is not stated in 174A.7 - instead, 174A.7.1.7 points to 174.5).

178.2 Error ratio allocation

A complete PHY is expected to meet the frame loss ratio specifications in 174A.5.

A PMD receiver is expected to meet the block error ratio specifications in 174A.7, measured at the PMA adjacent to the PMD, with BER_{added} equal to 1.6×10^{-5}.

A PHY receiver is expected to meet the block error ratio specifications in 174A.8, measured at the PCS, with BER_{added} equal to 8×10^{-6}.

174A.7 Error ratio tests for 200 Gb/s per lane ISLs

…

174A.7.1.7 Block error ratio method for a single lane using PMA-based measurements

… (procedure using the value of BER_{added})

The expected block error ratio is met if the measured value on each lane is less than the codeword error ratio limit specified in 174A.4 for an xMII Extender or 174A.5 for a PHY-to-PHY link.

174A.5 Error ratio allocation for a PHY-to-PHY link

Error ratio allocation of a PHY-to-PHY link is defined in terms of the frame loss ratio between the service interfaces of the transmitting PCS and the receiving PCS.

The frame loss ratio for 64-octet MAC frames with minimum interpacket gap is expected to be less than 6×10^{-11}.

For PHYs using the 200GBASE-R, 400GBASE-R, 800GBASE-R, or 1.6TBASE-R PCS, the expected frame loss ratio is equivalent to an FEC codeword error ratio (see 174A.9), as measured at the PCS, of less than 1.45×10^{-11}. If the errors at the input of the RS-FEC are uncorrelated, this is equivalent to a pre-correction BER (BER_{total}) of 2.92×10^{-4}.

NOTE—The frame loss ratio is affected by multiple components within the PHYs and by the medium, and is not a normative requirement of a specific component.

Error ratio
Comment 133

Cl **178** SC **178.2** P **344** L **4** # 133

Dudek, Mike — Marvell

Comment Type **T** *Comment Status* **D** *error ratio*

It is convoluted to find what the block error ratio specification is from the reference to 174A.8

SuggestedRemedy

Change the reference from 174A.8 to 174.8A.8.1.4. Make the equivalent change in clauses 179 to 183

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.
[Editor's note: CC: 178 to 183]

Similar to #132 but for PHY receiver instead of PMD receiver. The referenced subclause 174A.8 is similar in length and detail to 174A.7.

The suggested remedy is to point to 174A.8.1.4, which includes an expected block error ratio value (identical to the FEC codeword error ratio stated in 174A.5).

178.2 Error ratio allocation

A complete PHY is expected to meet the frame loss ratio specifications in 174A.5.

A PMD receiver is expected to meet the block error ratio specifications in 174A.7, measured at the PMA adjacent to the PMD, with BER_{added} equal to 1.6×10^{-5}.

A PHY receiver is expected to meet the block error ratio specifications in 174A.8, measured at the PCS, with BER_{added} equal to 8×10^{-6}.

174A.8.1.4 PCS block error ratio method for a complete PHY receiver

The following method is used to calculate the block error ratio for a complete PHY receiver using FEC bin counters provided in the PCS.

a) Measure the error histogram $H_m(k)$ (see 174A.8.1.3) with no stress applied to the receive input on any lane and assign $H_m(k)$ to $H_{mu}(k)$.

b) For each lane i, measure the error histogram $H_m(k)$ (see 174A.8.1.3) with stress, as specified for the PMD or AUI component, applied only to the receive input on lane i and assign $H_m(k)$ to $H_{ms}^{(i)}(k)$.

c) Calculate the error histogram $H_a(k)$ for the added BER using Equation (174A–5) with $BER = BER_{added}$.

d) Initialize H_e(k), the composite error histogram, to $H_a(k)$.

e) Iteratively, for each lane i, assign the result of hconv($H_e(k)$, $H_{ms}^{(i)}(k)$) (see 174A.7.1.4) to $H_e(k)$, and optionally (for better accuracy) deconvolve $H_{mu}(k)$ from H_e(k).

f) The measured block error ratio is equal to $H_e(16)$.

The measured block error ratio is expected be less than 1.45×10^{-11}.

Error ratio
Comments 132, 133, 155

Editor's recommendation

Change the text in 178.2 and 179.2 as follows:

178.2 Error ratio allocation

A complete PHY is expected to meet the frame loss ratio specifications in 174A.5.

With a compliant input signal, a PMD receiver is expected to meet the block error ratio of 1.45×10^{-11} (see 174A.5) ~~specifications in 174A.7~~, measured at the PMA adjacent to the PMD using the method described in 174A.7, with BER_{added} equal to 1.6×10^{-5}.

With a compliant input signal, a PHY receiver is expected to meet the block error ratio of 1.45×10^{-11} (see 174A.5) ~~specifications in 174A.8~~, measured at the PCS using the method described in 174A.8, with BER_{added} equal to 8×10^{-6}.

Apply similar changes, as appropriate, in 180.2, 181.2, 182.2, 183.2, 185.2, 176C.2, 176D.2; keeping the existing values for BER_{added} and block error ratio (which may be different).

To align it with 174A.7.1.7, change the last paragraph in 174A.8.1.4 as follows:

The measured block error ratio is expected be less than ~~1.45×10^{-11}~~ the codeword error ratio limit specified in 174A.5.

Implement with editorial license.

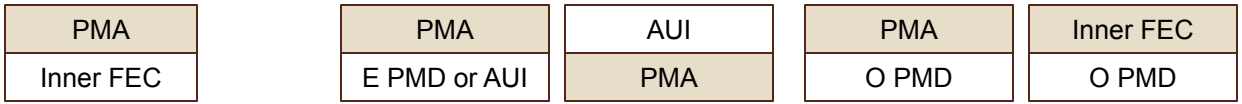
Pattern Generators and Checkers for PMA and xBASE-R Inner FEC

Comments 123, 26, 27, 116, 170, 171, 169
Expansion on dudek_3dj_01_2503

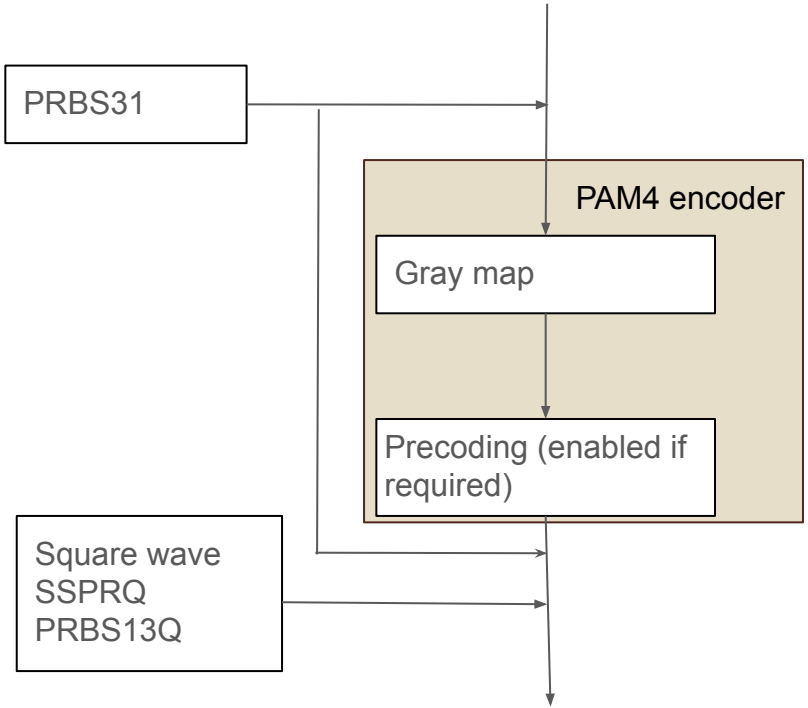
Functional requirements from black box perspective (background, not proposal)

(note that PRBS31Q is PRBS31 gray mapped)

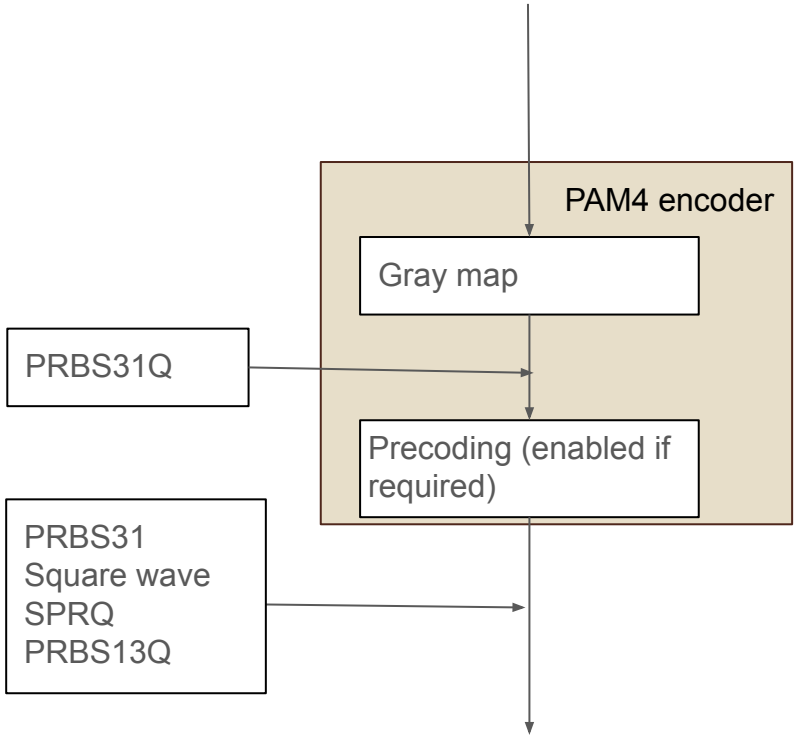
Functional capability	For an Clause 176 PMA above a Clause 177 Inner FEC	For a Clause 176 PMA above a KR/CR PMD or an AUI component or for a Clause 176 PMA below an AUI component	For a Clause 177 PMA or a Clause 177 Inner FEC above an IMDD optical PMD
PAM4 encoding/decoding (precoder enabled as required)	N/A	required	required
PRBS31 generation	required	N/A	N/A
PRBS31Q generation	N/A	required	required
PRBS13Q/PRBS9Q generation	N/A	optional	Optional (not PRBS9Q)
Square wave generation	N/A	N/A	optional
SSPRQ generation	N/A	N/A	Required in Inner FEC (#253) Optional in PMA
PRBS31 checking with block error counters	required	N/A	N/A
PRBS31Q checking With block error counters	N/A	required	Required (block error counting not required in Inner FEC)



Pattern generation and encoding in PMA or Clause 177 Inner FEC intent (background, not proposal)

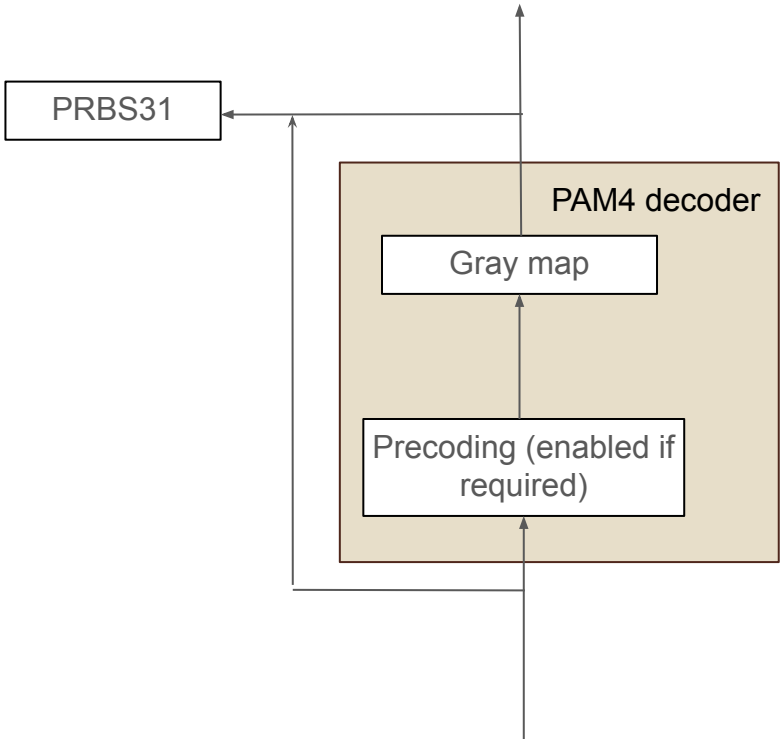


PROPOSED

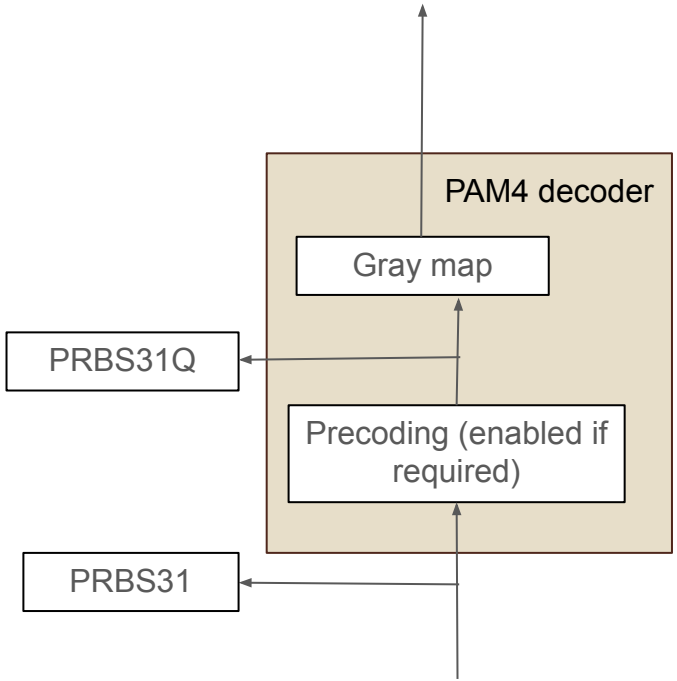


ALTERNATE

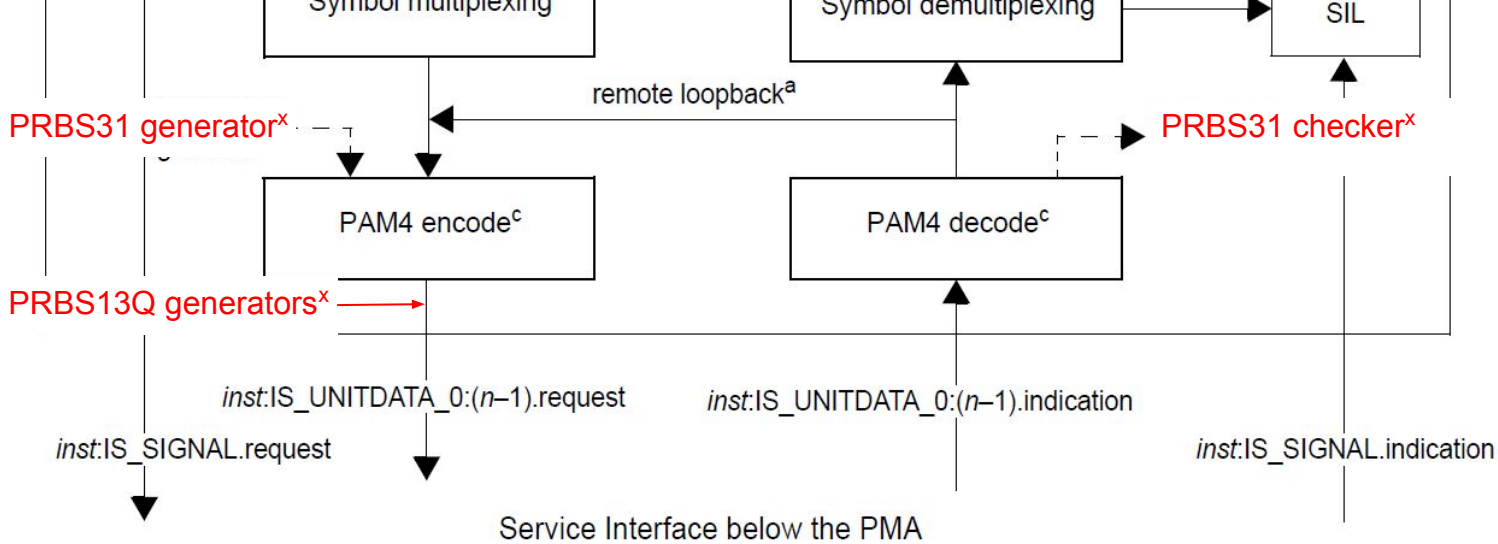
Pattern checking and encoding on PMA or Clause 177 Inner FEC intent (background, not proposal)



PROPOSED



ALTERNATE



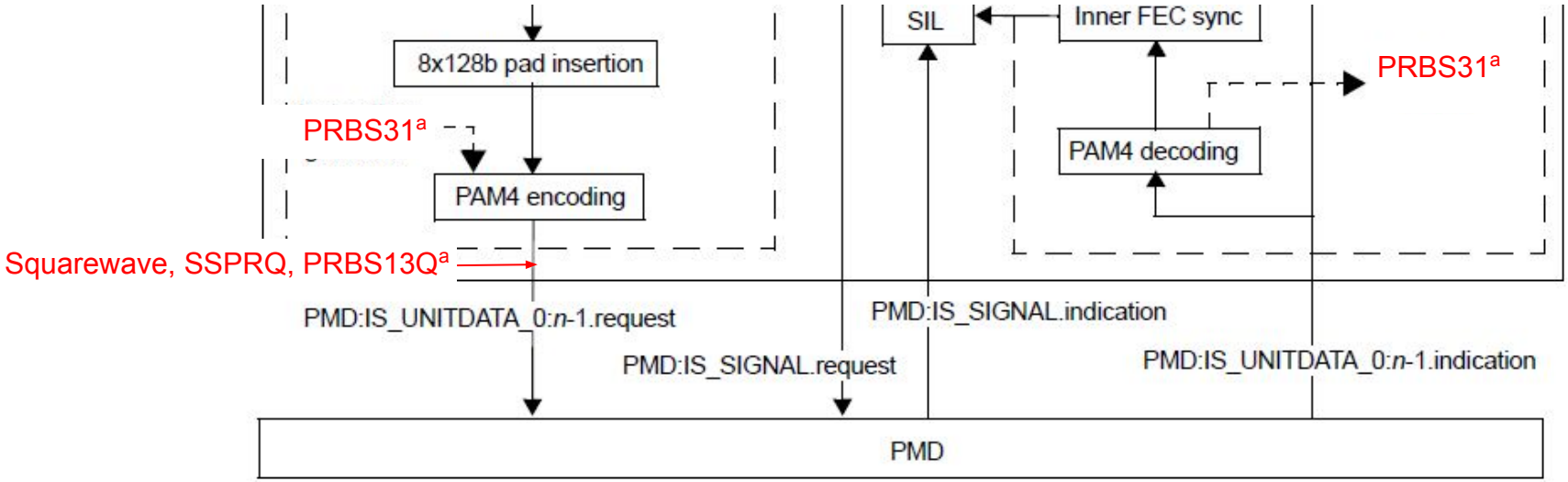
Changes to block diagrams in Clause 176.

inst: PMA or PMD or FEC or AUI
SIL: Signal indication logic

[a] Optional
[b] If 200GBASE-R, 400GBASE-R or 800GBASE-R
[c] If the sublayer below the PMA is an AUI or PMD
[d] If the sublayer above the PMA is a 1.6TAUI-16
[e] If the sublayer above the PMA is an 800GBASE-R BM-PMA
[f] PMA:IS_SIGNAL.request is not present when the sublayer above the PMA is a PCS or DTE XS
[x] Optional, required, or not applicable per <reference to table/text>
m = 8 (200GBASE-R), 16 (400GBASE-R), 32 (800GBASE-R), or 16 (1.6TBASE-R)
n = 1 (200GBASE-R), 2 (400GBASE-R), 4 (800GBASE-R), or 8 (1.6TBASE-R)

Figure 176–2—200GBASE-R 8:1, 400GBASE-R 16:2, 800GBASE-R 32:4, 1.6TBASE-R 16:8 PMAs functional block diagram

Changes to block diagram in Clause 177



[a] Optional, required, or not applicable per <reference to table/text>

Figure 177–2—Functional block diagram

Functional block requirements for Clause 176 PMA and Clause 177 Inner FEC

Functional capability	For a PMA above Clause 177 Inner FEC	For a PMA above a KR/CR PMD or an AUI or for a PMA below an AUI	For a PMA or an Inner FEC above an IMDD optical PMD
PAM4 encoder/decoder (precoder enabled as required)	N/A	required	required
PRBS31 generator	required	required	required
PRBS31Q provided by PRBS31 generator + PAM4 encoder	N/A	require	required
PRBS13Q/PRBS9Q generator	N/A	optional	PRBS13Q Optional (PRBS9Q n/a)
Square wave generator	N/A	N/A	optional
SSPRQ generator	N/A	N/A	Required for Inner FEC (#253) Optional for PMA
PRBS31 checker with block error counters	required	required	Required (for Inner FEC, block error counter not required)
PRBS31Q checking provided by PAM4 decoder + PRBS31 checker	N/A	required	Required (for Inner FEC, block error counter not required)

Annotate these requirements in text or table in 176.7.4, 177.4.9, and 177.5.2 (or other appropriate location) as editorially appropriate.