ILT for Coherent PMDs

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Supporters

Why ILT for coherent PMDs -- Need

- From the host equipment's POV, IMDD or Coherent serve as an 800GE optical port, it doesn't necessarily differentiate the modulation technology. The difference mostly lies in the user's experience in cost and performance. An example:
    - 10km reach sees application in Metro Access network and DC Campus networking
    - 802.3dj provides 800GBASE-LR4/800GBASE-LR1. + common form factors (QSFP-DD/OSFP) = 800GE optical module
        - Both support running 800GE MAC traffic
        - Both single pair of fiber
        - Both support interfacing 800G-AUI8 and 800G-AUI4
    - Modules are plugged in the same 800GE core switches/routers
- A pair of host equipment with 200G/lane SERDES will be able to bring up the full path using ILT, with IMDD modules.
    - Requires a protocol coordinating host & module, CMIS & ILT.
    - ILT also makes sure the path is up and communicate functionally.
- The same pair of host equipment will have to run through another path up protocol, with coherent modules.
    - This protocol is independent from the two link partners (the set of equipment + module)
    - Not guaranteeing quality of communication.
- It is also likely that a host equipment is plugged with IMDD modules and coherent modules at the same time.

Why ILT for coherent PMDs -- Benefit

- Bringing ILT to coherent PMDs
  - Consolidate path up protocol of the equipment, offers savings from R&D and OPEX perspective
  - Better confidence @ link up, i.e. each ISL is up and function properly
  - Provides possibility of coordinating settings between the two coherent PMD for better performance
    - Tx wavelength alignment,
      - LR1 allows $\pm$20GHz range, and up to 40GHz offset between carrier and LO, not sure it is good for DSP
    - XY/IQ skew and imbalance compensation
      - a known challenge among the coherent community for higher baud rate. OIF has agreed to open up a back channel, which also runs during operation.
  - Other possibilities to be explored.

ILT for coherent PMDs -Technical feasibility

- Key aspects of enabling ILT
  - **Transmitting Message between the link partners**, message encoded in a designed frame

    IMDD: A frame mapped to PAM4 symbols, carrying information defined for ILT. Allows NRZ for easier alignment/training.

    Coherent: A DSP frame mapped to 16QAM symbols. PS are mapped to QPSK constellation points for easier frame alignment.

  - **Deciding and Transmitting RTS/Remote_RTS among interfaces and ISLs**

    IMDD: RTS based on ISL_ready, requiring local_rx_ready and remote rx_ready(informed via the message carried in the frame) . i.e. based on training frame lock and signal quality (criteria is implementation specific)

    Coherent: coherent receiver already implements an "acquisition" process, and its DSP is well capable of confirm locking and signal quality, e.g., the dsp_lock<x> / all_locked state variable of the 800GBASE-LR1 inner FEC.

  - Configuration of Tx settings based on decision of link partner's receiver — A future topic

    IMDD: O1 currently only provides pre-coding configuration.

    Coherent: many possibilities, however, needs further and careful investigation on the content

No obvious technical barriers exist in using ILT for coherent PMDs, just need to build consensus

Can we extend link training to LR1?
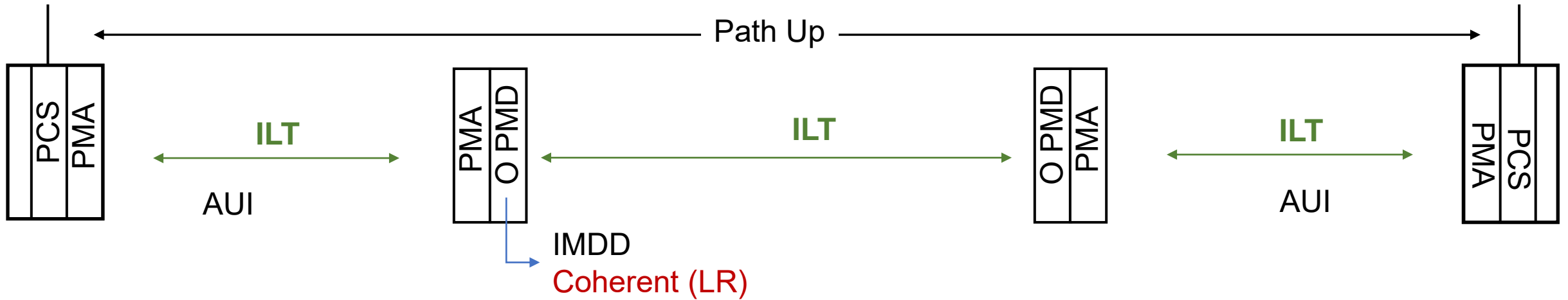
Can we extend link training to ER1-20 and ER?

178B.5.3 Training xMII Extenders

Seems ILT function already required for xMII Extenders?

Training on an ISL within an xMII Extender follows the same process, such that local_rts and remote_rts are communicated to the PHY XS using its IS_SIGNAL.indication and IS_SIGNAL.request primitives.

AUI components within an xMII Extender may train before or in parallel with the PCS to PCS path, and training signaling will continue until the main path is ready. This is the same behavior as AUI components within a PHY.
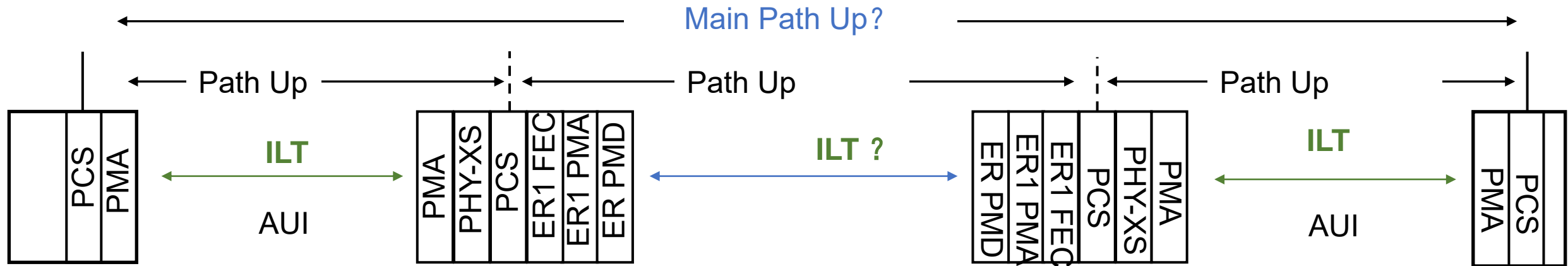
- Back Channel currently discussed in OIF for 1.6T-ZR+ → to me, sounds like a in-situ link training.
- Coordination between AUI path (xMII Extender) and ER1 coherent optical path needs some further explaining in the draft

ILT for coherent PMDs – Initial thought on solutions

- **Baby steps**, start with assigning and transmitting RTS, to allow path up based on true signal acquisition and quality, instead of an assumed RTS=1

Deciding RTS

> local_tf_lock
>
> Boolean variable that is true when mr_training_enable is true and the training frame marker positions have been identified on a lane of the interface and is false otherwise. The value of this variable is encoded in the receiver frame lock bit in the status field of transmitted training frames.

> dsp_lock<x>
>
> A Boolean variable that is set to true when the receiver has detected the location of the PS for a given polarization symbol stream on the 800GBASE-LR1 PMD service interface, where $x = 0:1$.

> local_rx_ready
>
> Boolean variable that is set to true when the receiver on a lane of the interface has determined that the peer interface transmitter is transmitting a PAM4 signal, that the remote transmit and local receive equalizers have been optimized, and that no further adjustments are required for normal data transmission. It is set to false otherwise. The exact criteria for setting this variable to true are implementation specific. When mr_training_enable is true, the value of this variable is encoded as the "receiver ready" bit in the status field of transmitted training frames.

- dsp_lock/all_locked of the Inner FEC may be a good proxy. (receiver locking into the position of the PS of the DSP frame)

- 16QAM data is detected.
- Signal quality is decided by the implementer.

Transmitting RTS

- Coherent PS has two seeds as identifier for X/Y polarization.
- Table 178B-1 defined 8 seeds of PRBS13 as identifier for the 8 lanes

- Define a set of seeds of the PS as the RTS indicator across the link partners

Summary

- Enabling ILT for coherent PMDs brings benefit to equipment management, plug-and-play of Ethernet coherent interfaces

- It also opens the door to performance tuning upon link up

- Ethernet will see more coherent interfaces as we go to higher speed. Coherent interface itself will see more technical challenge that could leverage the capability of ILT.

- Focus on the must-have function of supporting ILT for now, i.e. assigning and transmitting RTS. Parameter tuning may complicates things for now, but having the possibility is important for future generation.

- The goal in 800GBASE-R coherent PMDs is to bringing ILT as a building block.

Questions?