

Module Receiver Interference Tolerance Test Revisited

Kent Lusted, Synopsys

9 March 2026

D2.3 comment #58 & #60

Introduction – comment #58 & 60 from D2.3

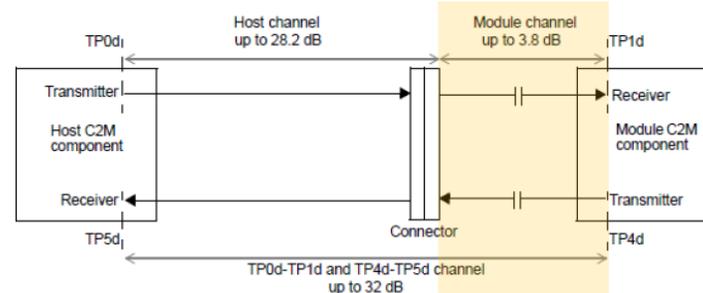
CI 176D	SC 176D.8.13.2	P 836	L 9	# 58
Healey, Adam		Broadcom, Inc.		
Comment Type	TR	Comment Status	R	channel model (E)
<p>For the module receiver interference tolerance test, item b) states that "COM is calculated using the module device package and device termination models". However, the module test channel shown in Figure 176D-8b includes the host compliance board (HCB). The reference loss of the HCB equals the module loss allocation to TP1d illustrated in Figure 176D-6. Therefore, the addition of the module device package model results in the interference tolerance test being calibrated with approximately 2.1 dB more loss than a module has been allocated.</p>				
<i>SuggestedRemedy</i>				
<p>Replace 176D.8.13.2 item b) with the following. "For the module test, the test channel is measured between the Tx and Rx test references shown in Figure 176D-8b, and COM is calculated using device termination model in Table 176D-6 for the receiver S-parameter model."</p>				
<i>Response</i>		<i>Response Status</i> C		
<p>REJECT.</p> <p>This comment does not apply to the substantive changes between IEEE P802.3dj D2.2 and D2.3 or the unsatisfied negative comments from previous drafts. Hence it is not within the scope of the recirculation ballot.</p> <p>The CRG has reviewed the contribution <https://www.ieee802.org/3/dj/public/26_01/healey_3dj_01_2601.pdf></p> <p>In discussion of the presentation there was support for the direction of the proposed changes in slide 4 of the presentation. However, further analysis of the effect of the changes is required.</p> <p>There is no consensus for making the suggested changes at this time.</p> <p>This topic can be reconsidered in SA ballot and the commenter is encouraged to resubmit at that time.</p>				

CI 176D	SC 176D.6.5	P 824	L 25	# 60
Healey, Adam		Broadcom, Inc.		
Comment Type	TR	Comment Status	R	channel model (E)
<p>Slide 7 of <https://www.ieee802.org/3/dj/public/25_11/healey_3dj_01a_2511.pdf> highlighted that there is some ambiguity in the loss that has been allocated to the module. The value computed on slide 12 for module output Rpeak was based on the more generous interpretation i.e., 5.9 dB from the TP4d to the mating point of the connector. If the loss from TP4d to the mating point of the connector is limited to 3.8 dB as shown in Figure 176D-6, then the Rpeak limit in Table 176D-3 needs to be adjusted.</p>				
<i>SuggestedRemedy</i>				
<p>If the module loss allocation is limited to 3.8 dB, then in Table 176D-3 change Rpeak (min) to 0.51 and change the lower value of the vf range to 0.392.</p>				
<i>Response</i>		<i>Response Status</i> C		
<p>REJECT.</p> <p>The CRG has reviewed the contribution <https://www.ieee802.org/3/dj/public/26_01/healey_3dj_01_2601.pdf>.</p> <p>There is no consensus to make the proposed changes at this time.</p> <p>Further work and consensus building on this topic are encouraged.</p>				

Healey Contribution from January 2026

Chip-to-module reference insertion loss budget

- The D2.3 reference insertion loss budget allocates 3.8 dB to the module
- This allocation is from the mating point of the MDI connector to TP1d or TP4d (it includes the module device package)
- Note that the reference insertion loss of a host compliance board is also 3.8 dB
- Some module specifications in D2.3 are not consistent with this insertion loss allocation



NOTE—For loss budgeting purposes, the host channel loss is from TP0d to the center of the edge connector of the module.

Figure 176D-6—Reference insertion loss budget at 53.125 GHz

IEEE P802.3dj Task Force, January 2026 (r0)

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https://www.ieee802.org/3/dj/public/26_01/healey_3dj_01_2601.pdf

March 2026

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Healey Contribution from January 2026

D2.3 interference tolerance test calibration

176D.8.13.2 Test channel calibration

The COM of the test channel is calculated using the method defined in Annex 178A and the parameters of 176D.7.2, with the following considerations:

- For the host test, the test channel is measured between the Tx and Rx test references shown in Figure 176D-7b, and COM is calculated using the partial host channel, device package, and device termination models in Table 176D-6 for the receiver S-parameter model.
- For the module test, the test channel is measured between the Tx and Rx test references shown in Figure 176D-8b, and COM is calculated using the module device package and device termination models in Table 176D-6 for the receiver S-parameter model. Calculation is performed for both case 1 and case 2 of the package transmission line 1 length, and the value of COM is taken as the lower of the two calculated values.

Table 176D-11—Interference tolerance test parameters

Parameter	Host test	Module test L (low loss) ^a	Module test H (high loss)	Units
Test channel insertion loss at 53.125 GHz	9 ± 2	9 ± 2	32 ± 0.5	dB

Table 176D-6—Host and module model parameters (continued)

Parameter	Symbol	Value	Units
Device package model, module			
Transmission line parameter γ_0	γ_0	5×10^{-4}	1/mm
Transmission line parameter a_1	a_1	8.9×10^{-4}	ns ^{1/2} /mm
Transmission line parameter a_2	a_2	2×10^{-4}	ns/mm
Transmission line parameter τ	τ	6.141×10^{-3}	ns/mm
Transmission line 1 length, case 1	$z_p^{(1)}$	4	mm
Transmission line 1 length, case 2	$z_p^{(2)}$	10	mm
Transmission line 1 characteristic impedance	$Z_c^{(1)}$	87.5	Ω
Transmission line 2 length	$z_p^{(2)}$	1.8	mm
Transmission line 2 characteristic impedance	$Z_c^{(2)}$	92.5	Ω
Single-ended package capacitance at package-to-board interface	C_p	40×10^{-6}	nF

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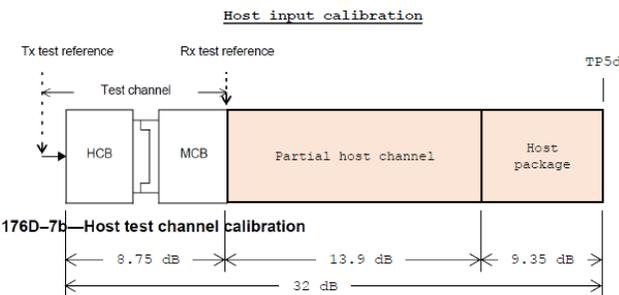
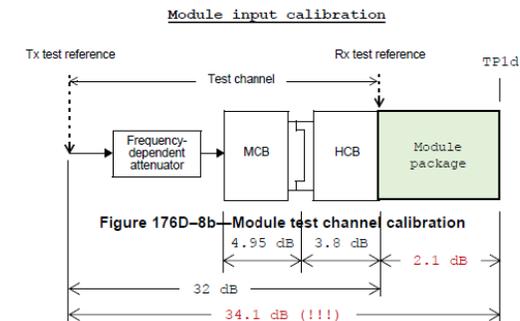


Figure 176D-7b—Host test channel calibration



Assumed module loss is too high!

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Healey Contribution from January 2026

Correction to interference tolerance test calibration

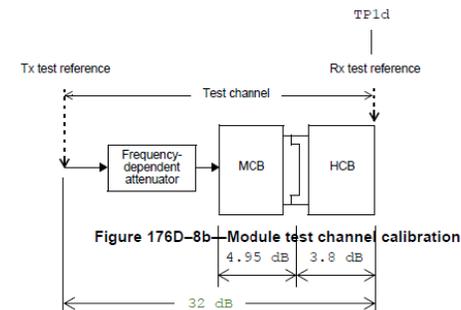
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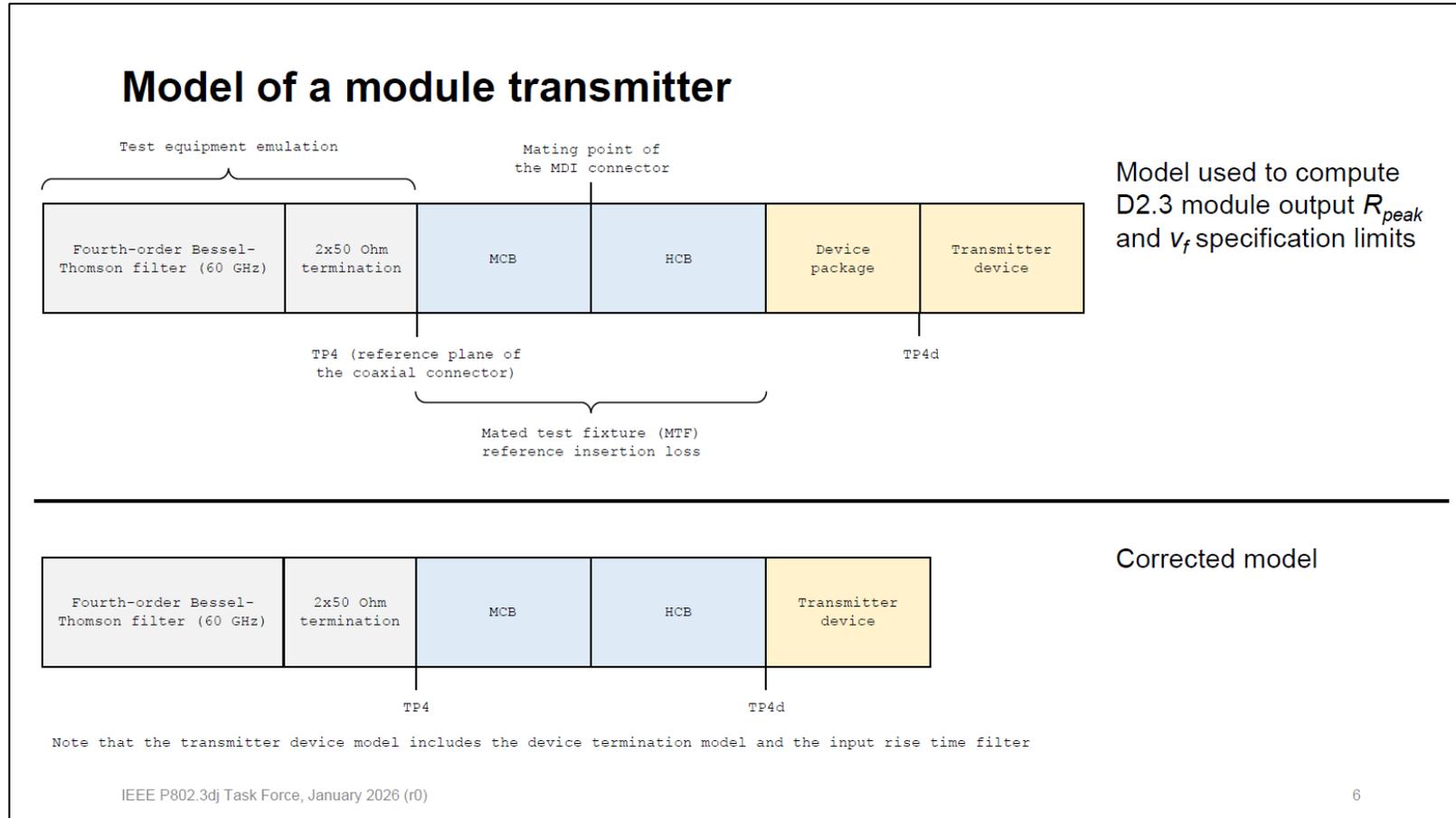


Healey Contribution from January 2026

Module output R_{peak} and v_f

- In [healey_3dj_01a_2511](#), module output specification limits were derived from the Channel Operating Margin (COM) model of a module transmitter and the mated test fixture reference insertion loss
- Limits were computed with a module device package model in addition to the host compliance board
- This was consistent with the interference tolerance test calibration but not consistent with the module loss allocation
- If the interference tolerance test calibration is corrected, then the module output specification limits should also be revisited

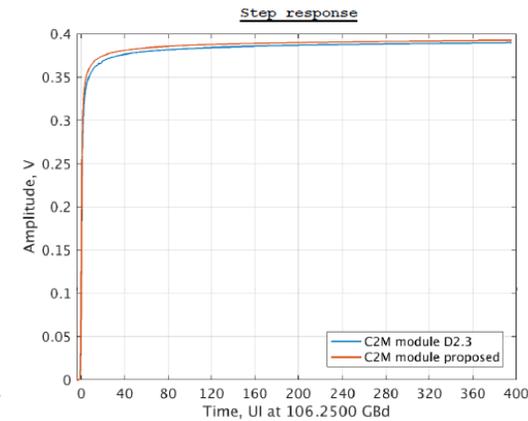
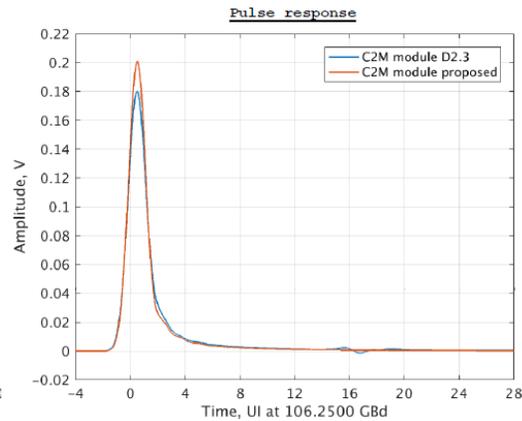
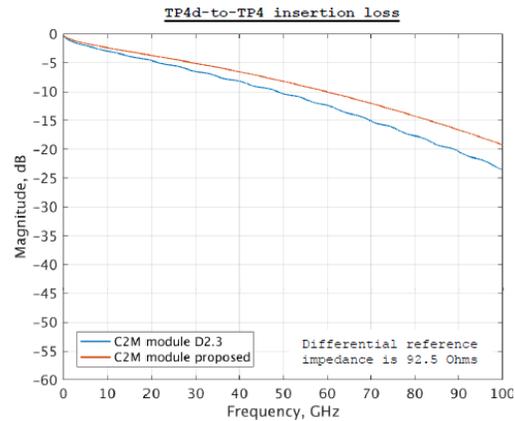
Healey Contribution from January 2026



https://www.ieee802.org/3/dj/public/26_01/healey_3dj_01_2601.pdf

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Specification limits recalculated using the corrected model



Case	Package		Insertion loss, dB		P_{max} , V	v_f , V	R_{peak}
	Class	Length, mm	Mated test fixture	TP4d-to-TP4			
C2M module, D2.3	A	10	8.75	10.82	0.179	0.389	0.46
C2M module, proposed	n/a	n/a	8.75	8.75	0.2	0.392	0.51

Corrected specification limits

Healey Contribution from January 2026

Recommendations

- Remove module device package model from module interference and jitter tolerance test calibration
- Update module output R_{peak} and v_f limits to be consistent with its insertion loss allocation

Summary & Discussion

- A comment was filed on this topic against D3.0
- What is the consensus?

Thanks!