Effects of random and deterministic jitter on FEC performance

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Contents

- Summary of 100 Gb/s lab experiment results
  - Contents courtesy of Marco Mazzini and Yi Tang
  - Full presentation was presented at OIF in August 2024 (*Transmitter Jitter vs EECQ/TDECQ vs Post-FEC Performance*, oif2024.449.02)
- 200 Gb/s jitter simulation experiment
  - Jitter-domain simulation of different profiles
  - Statistics at FEC codeword grouping (including symbol muxing and codeword interleaving)
- Notes and Thoughts

100 Gb/s per lane experiment results

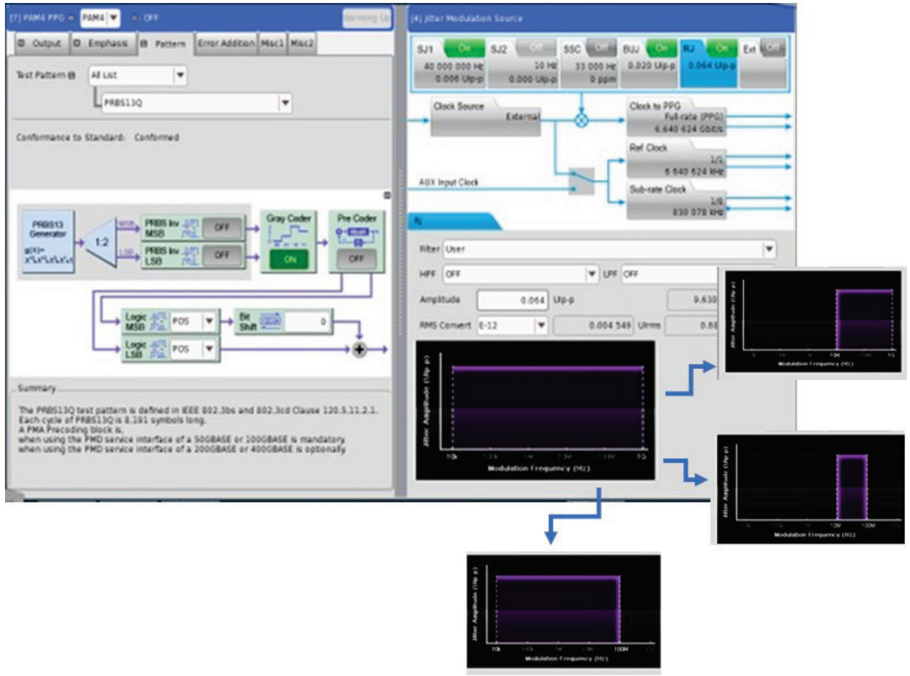
Test Setup

Electrical DAC
(Taps, SJ, BUJ)

RJ → Filter

Modulator
E/O

Scope



Calibrated optical signals:

- SECQ = ~3.4 dB (SER probability: 4E-4)
- SJ and BUJ are present and consistent across test cases.
- R_J = 0.054UI_{P-P} (0.0038382UI_{RMS}, BER@1e-12) with different spectral components applied through various filter settings.

CASE	Frequency [MHz]		Relative Power Density
	HPF	LPF	
1[1]	OFF	OFF	1
2	OFF	100	~10
3	20	OFF	~1
4	20	100	~10
5	10	OFF	~1
6	10	100	~10

[1]Unfiltered RJ has a white spectrum from 10KHz to 1 GHz.

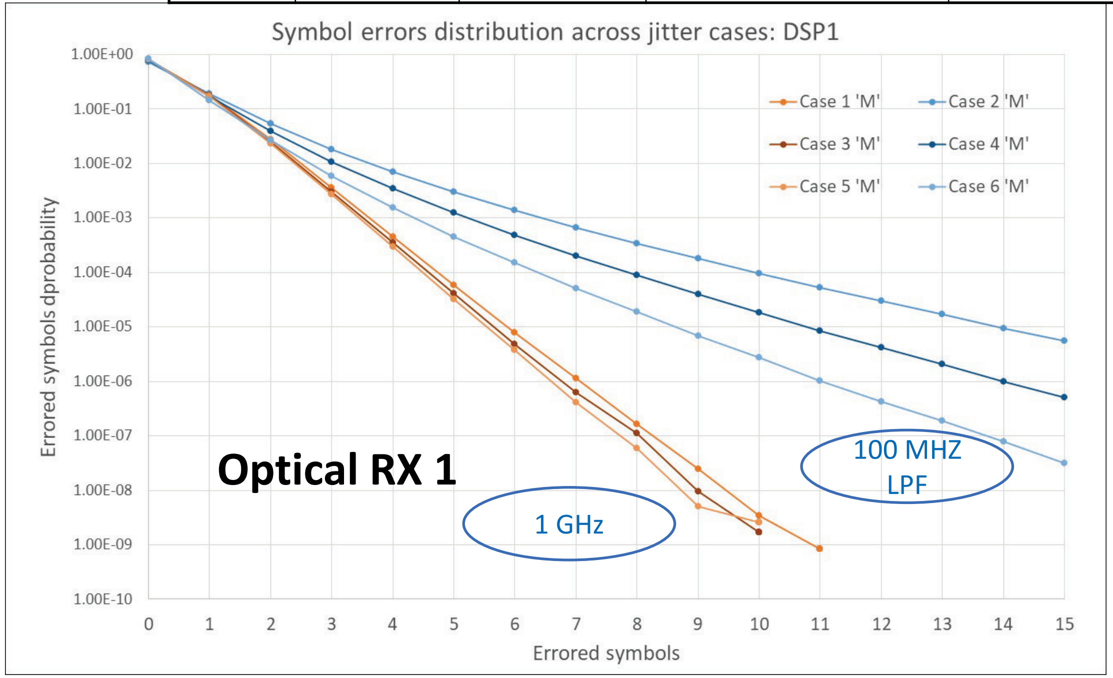
DUT – Optical RXs

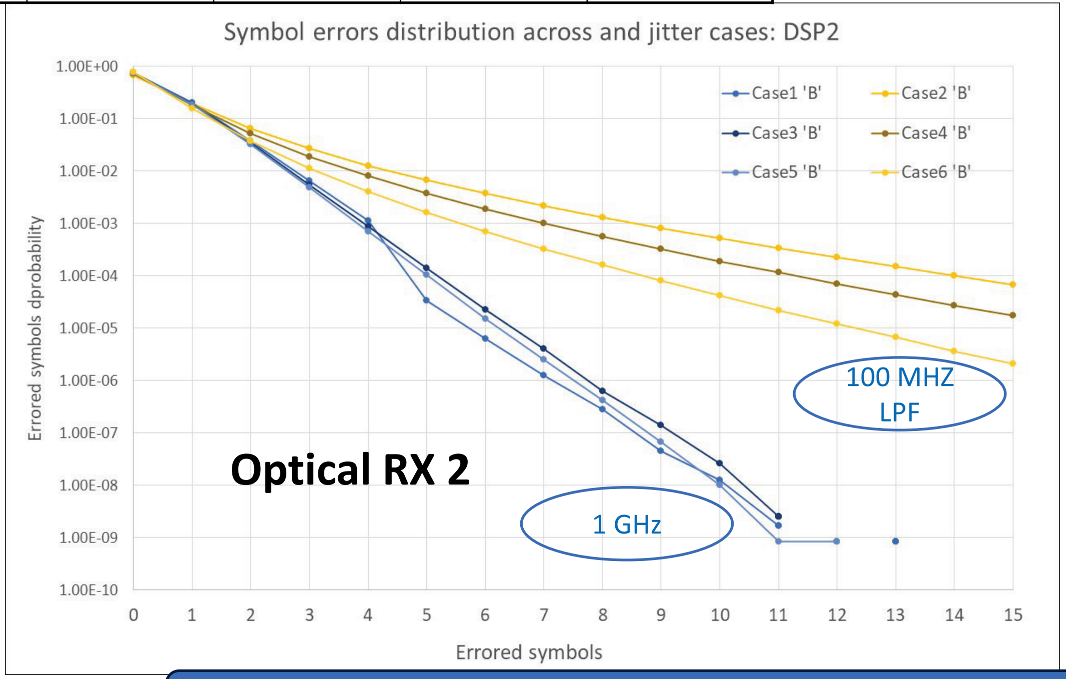
OMA = 0 dBm @ TP3

Content provided by Marco Mazzini and Yi Tang

Symbol Error Distribution

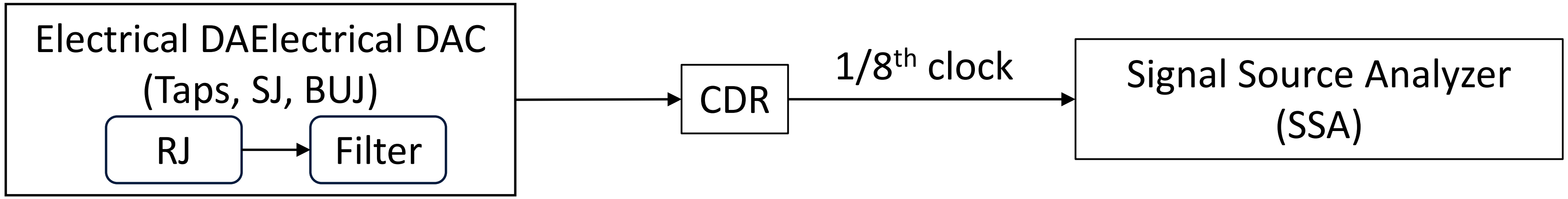
CASE	Frequncy [MHz]		Random Jitter Relative Power Density	SECQ [dB]	Optical RX 1		Optical RX 2	
	HPF	LPF			BER	Symbol Error	BER	Symbol Error
1	OFF	OFF	1	3.33	4.61E-05	13	3.94E-05	11
2	OFF	100	~10	3.33	5.83E-05	> 16	5.02E-05	> 16
3	20	OFF	~1	3.27	4.36E-05	11	3.77E-05	10
4	20	100	~10	3.39	4.94E-05	> 16	4.11E-05	> 16
5	10	OFF	~1	3.33	4.22E-05	12	3.64E-05	10
6	10	100	~10	3.4	3.96E-05	> 16	3.29E-05	> 16



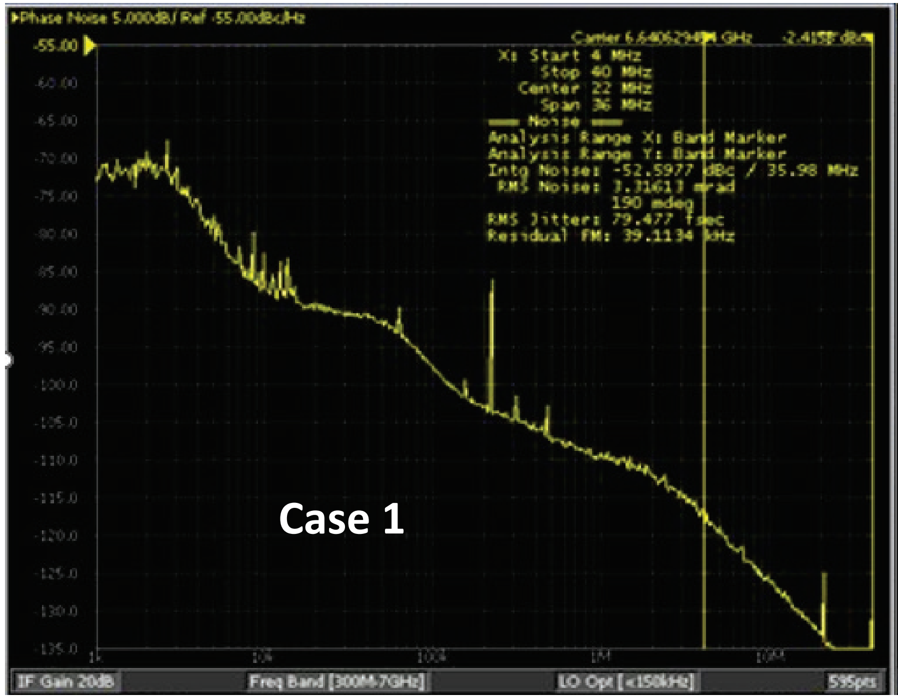


Content provided by Marco Mazzini and Yi Tang

Jitter Characterization of Test Cases



CASE	Frequency [MHz]		RJ_{RMS} [fs]
	HPF	LPF	(4MHz - 40MHz)
1	OFF	OFF	79.5
2	OFF	100	104
3	20	OFF	76
4	20	100	93.5
5	10	OFF	75.7
6	10	100	87



Content provided by Marco Mazzini and Yi Tang

Takeaway

- Certain jitter profiles are detrimental to FEC performance, and current industry specifications do not effectively regulate jitter behavior for either TX or RX, leading to an interoperability gap at the system level.
  - TX: The TDECQ measurement fails to capture the negative impact of certain jitter profiles, such as high phase noise just above the CDR LBW, of a transmitter.
  - RX: A. Stress input tests, such as SRS, do not include jitter profiles to which the RX may be sensitive; B. RX BER is not sensitive to burst error conditions when harmful jitter profiles are applied. Tightening RX BER requirements does not provide sufficient protection against long FEC tails and marginal/failing FLR in such circumstances.

Content provided by Marco Mazzini and Yi Tang

200 Gb/s simulation

Purpose and method

- Test the effect of various jitter profiles
  - Sinusoidal, random with different filters, mixed
- Simplified simulation
  - Jitter-domain, not time-domain – 1 sample per UI
  - 1 ms per test case
- Accounting for symbol muxing and 4-way codeword interleaving:
  - For each 5 jitter samples (one per UI), find the largest (absolute) jitter per FEC symbol ➔ per-symbol jitter
  - For each FEC codeword:
    - Find the largest per-symbol jitter value that occurs in 16 or more FEC symbols ➔ **jitter_16 (**per-codeword, in mUI)
    - Find the number of FEC symbols that have per-symbol jitter larger than 50 mUI ➔ **num_sym_50**
  - Collect statistics of jitter_16 and num_sym_50
- Simulate J_{RMS} and J3u03 measurements
  - Using 1 of 8191 jitter samples

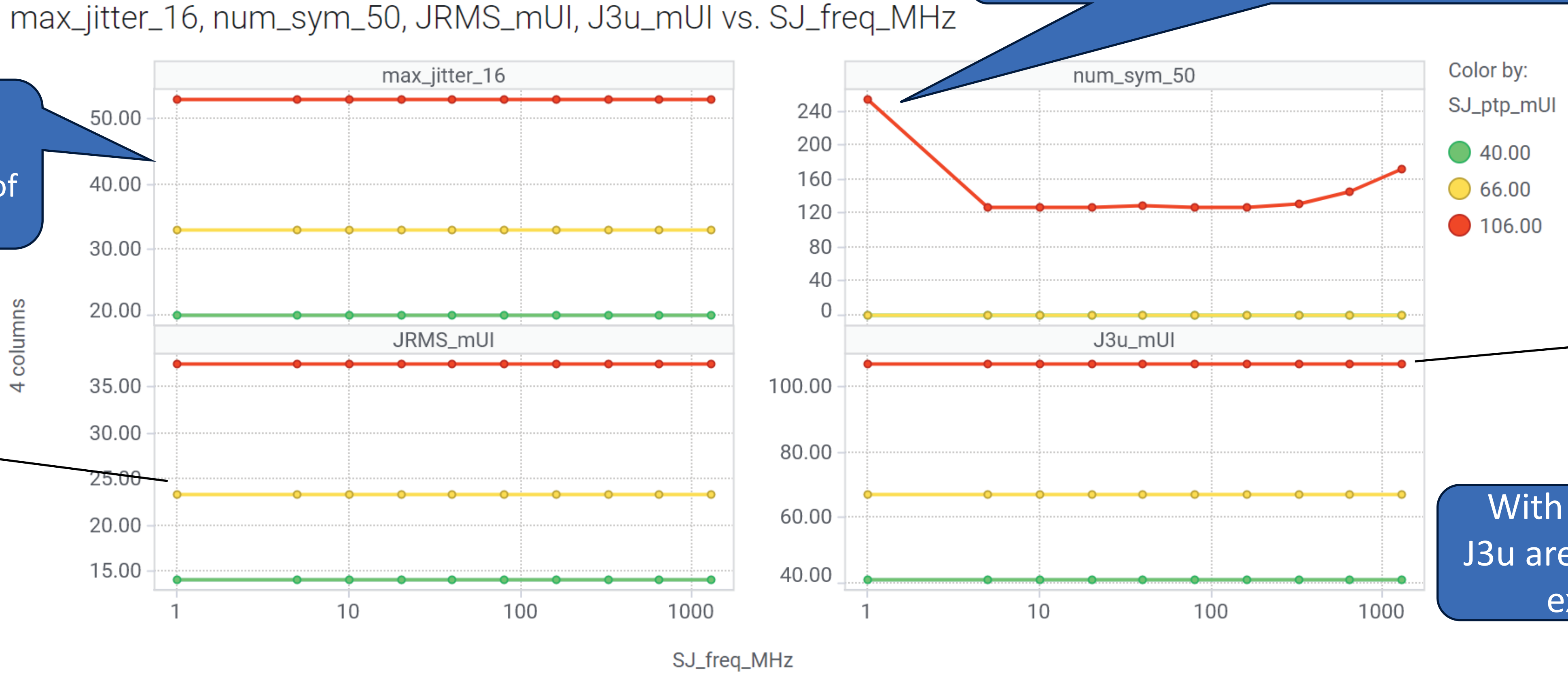
Test cases

- SJ
  - Frequency: 1 MHz, [5, 10, 20, … 1280] MHz
  - Amplitude (A_DD): [0, 20, 33, 53] mUI (0, 40, 66, 106 Pk-Pk)
- RJ
  - RMS: [0, 10, 16, 23] mUI
  - Each with:
    - Low-pass filter: 100 MHz, 1 GHz, or none
    - High-pass fiter: 100 MHz, 1 GHz, or none
    - Bandpass: from 100 MHz to 1 GHz
- All SJ cases without RJ
- All RJ cases without SJ
- SJ (f=40 MHz, A_DD=20 mUI) with RJ (RMS=10 mUI, all filter cases)
- Total of 54 cases

SJ only

Large low-frequency jitter can affect many more FEC symbols in 1 codeword – see next slide

Worst jitter effect is independent of frequency



Max J3u is 106 mUI

Max J_{RMS} is 23 mUI

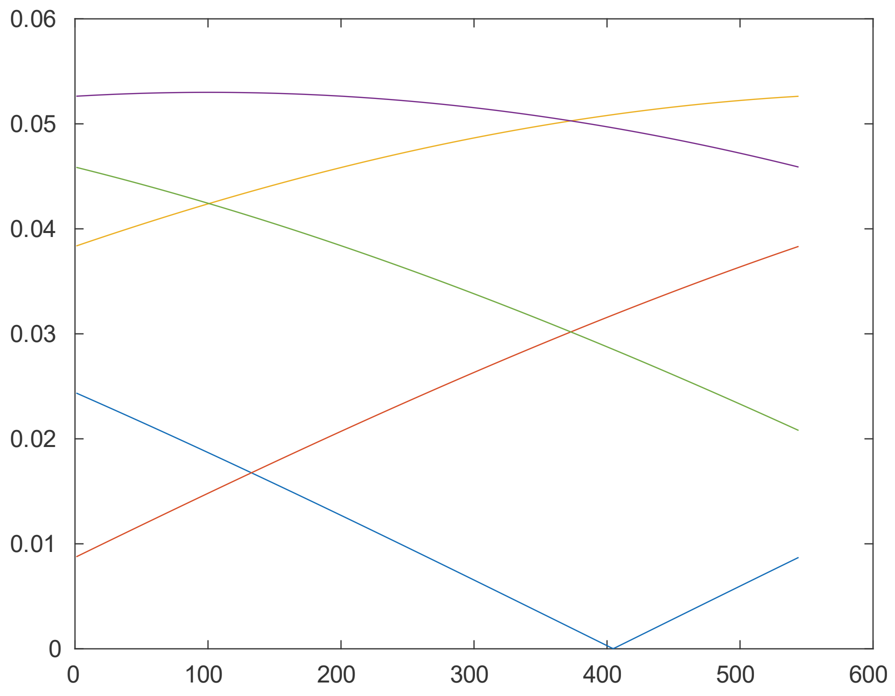
With SJ, J_{RMS} and J3u are constant, as expected

Jitter “scope traces” within one codeword

1 MHz SJ with A_{DD}=53 mUI :

Some codewords are “all high”, others are “all low”

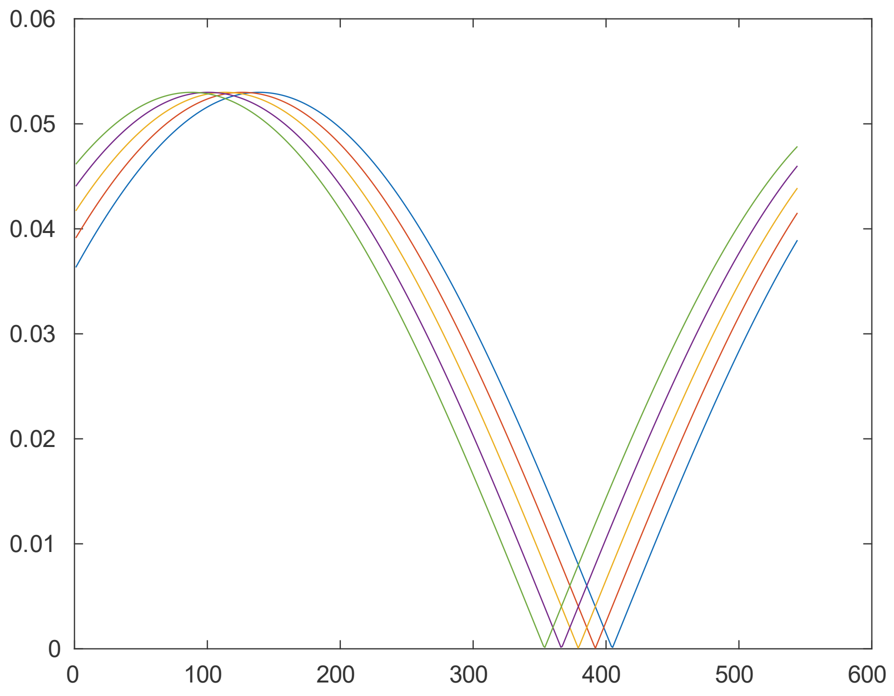
(Lower frequencies would be similar)



5 MHz SJ with A_{DD}=53 mUI :

Each codeword goes through a full SJ cycle

(Higher frequencies are similar)

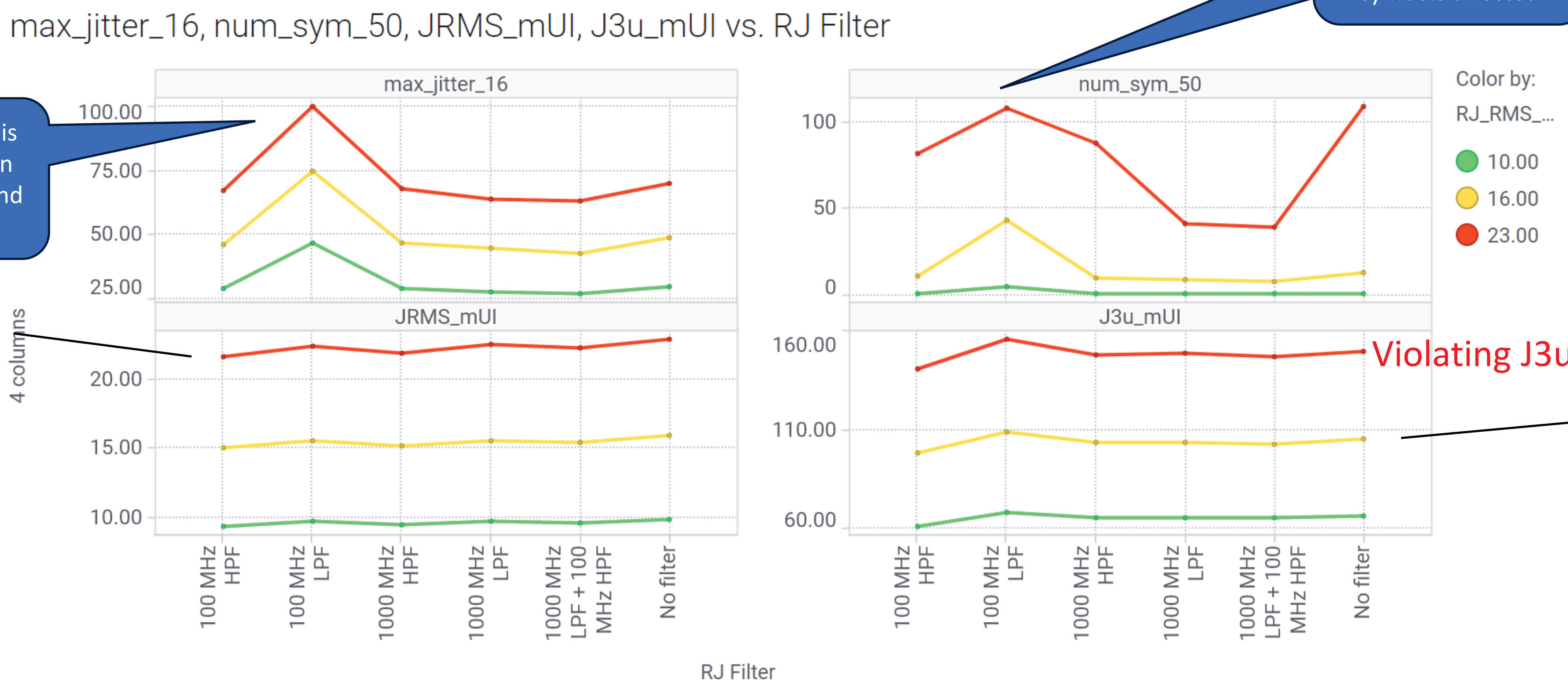


RJ only

Narrow band is also worse in terms of the number of symbols affected

Worst jitter effect is very dependent on profile. Narrow band is worse

Max J_{RMS} is 23 mUI



Violating J3u

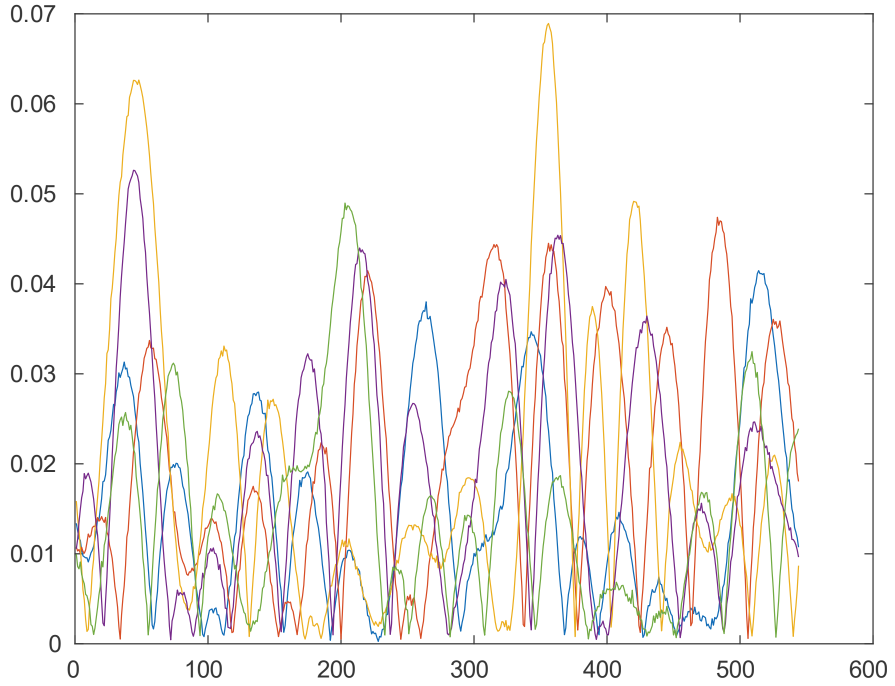
Max J3u is 106 mUI

Excessive J3u is always bad; meeting J_{RMS} it not enough. RJ concentrated at narrow bandwidth can be much worse.

Jitter "scope traces" within one codeword

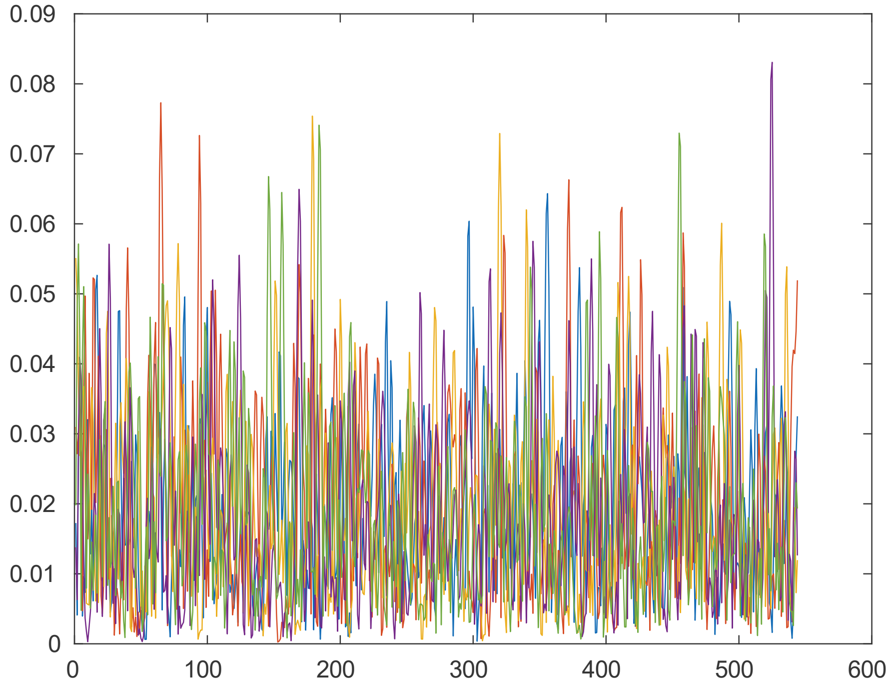
23 MUI RMS RJ with 100 MHz LPF:

Peaks are wide and span many symbols

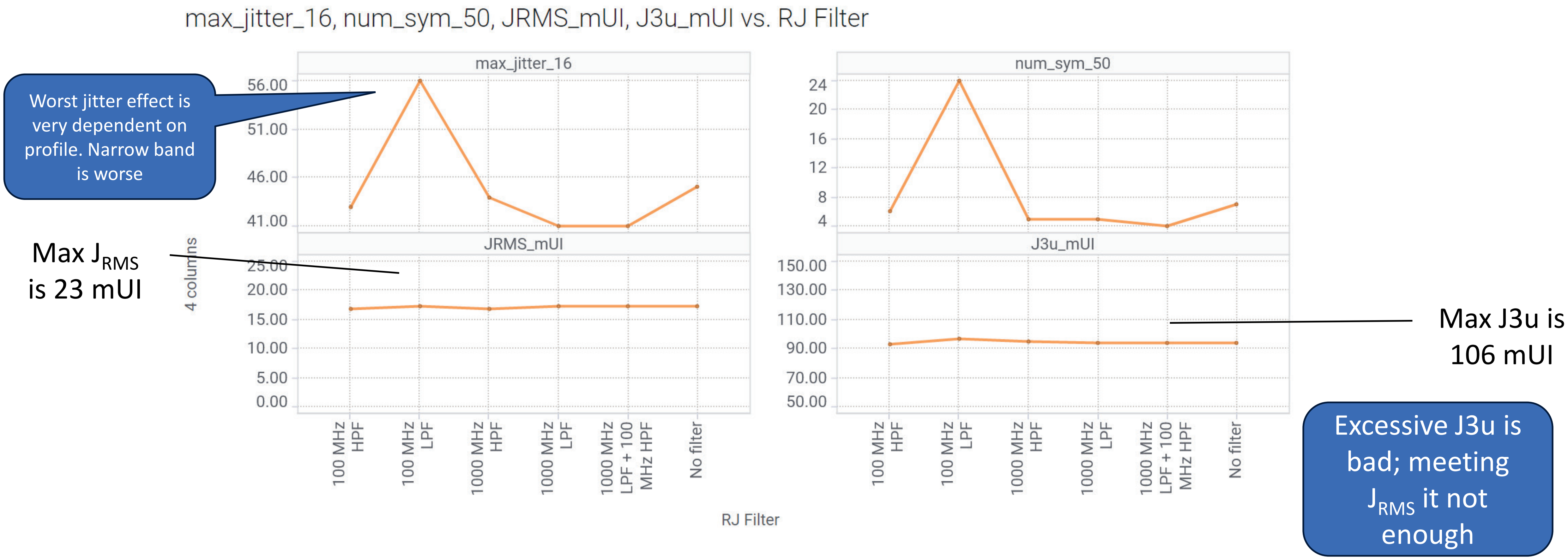


23 MUI RMS RJ with 1 GHz LPF:

Peaks are narrow and span few symbols



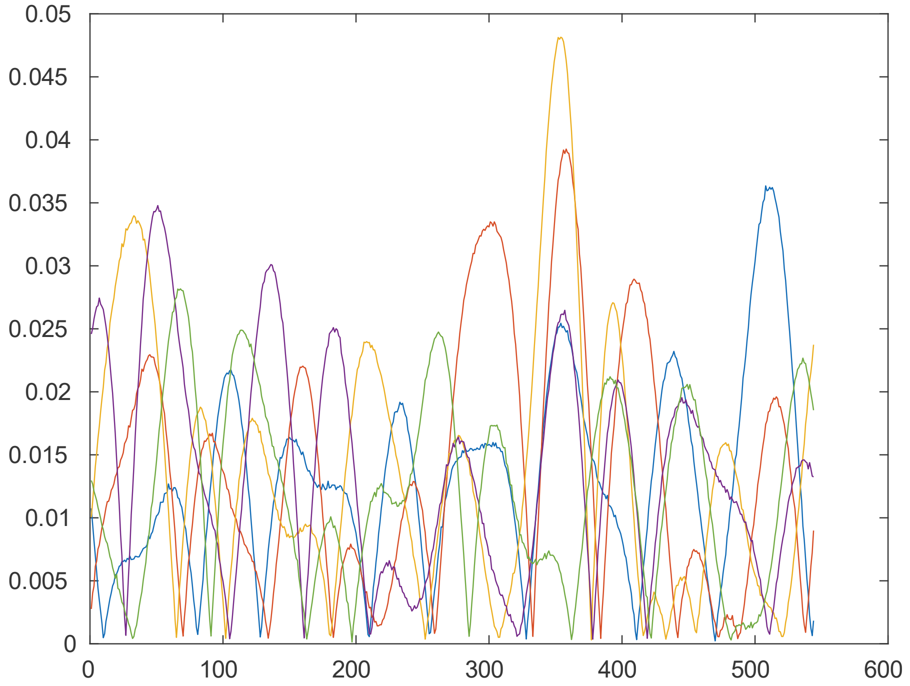
Combined SJ (40 mUI PtP) + RJ (10 mUI RMS)



Jitter “scope traces” within one codeword

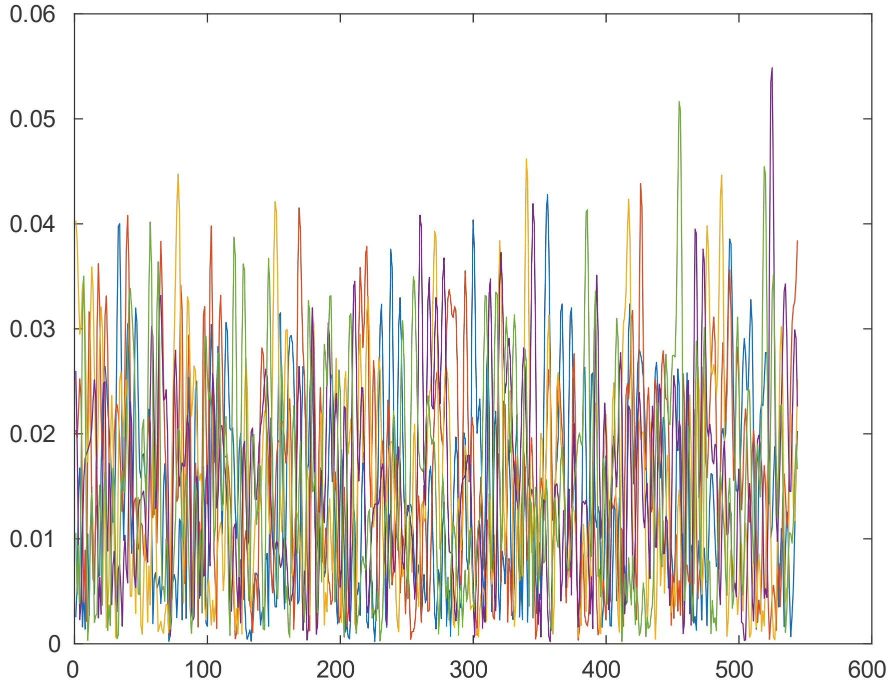
Combined SJ+RJ with 100 MHz LPF:

Peaks are wide and span many symbols



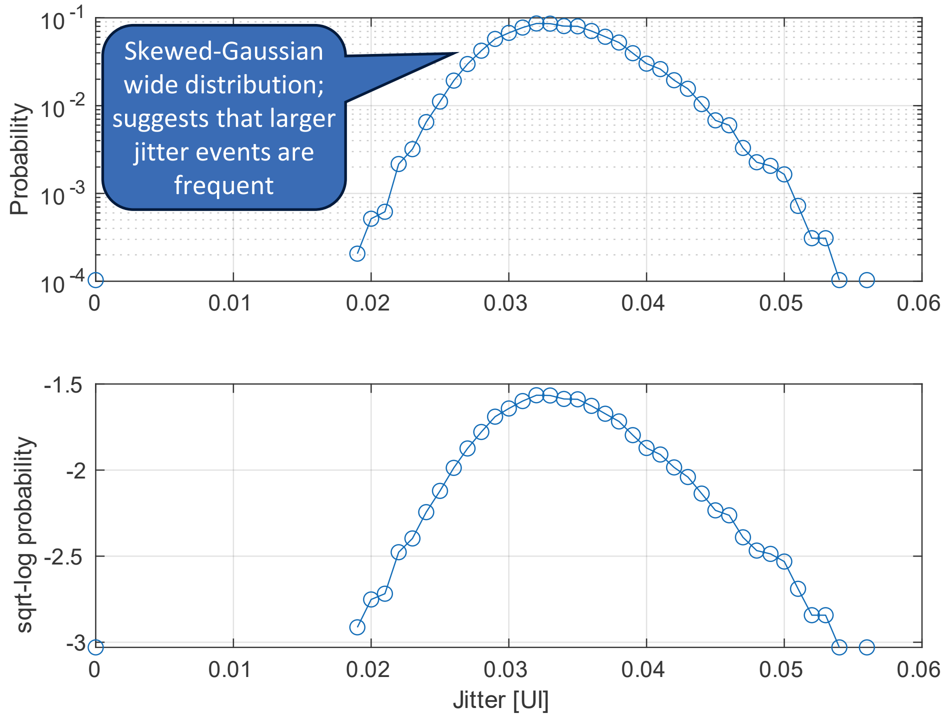
Combined SJ+RJ with 1 GHz LPF:

Peaks are narrow and span few symbols

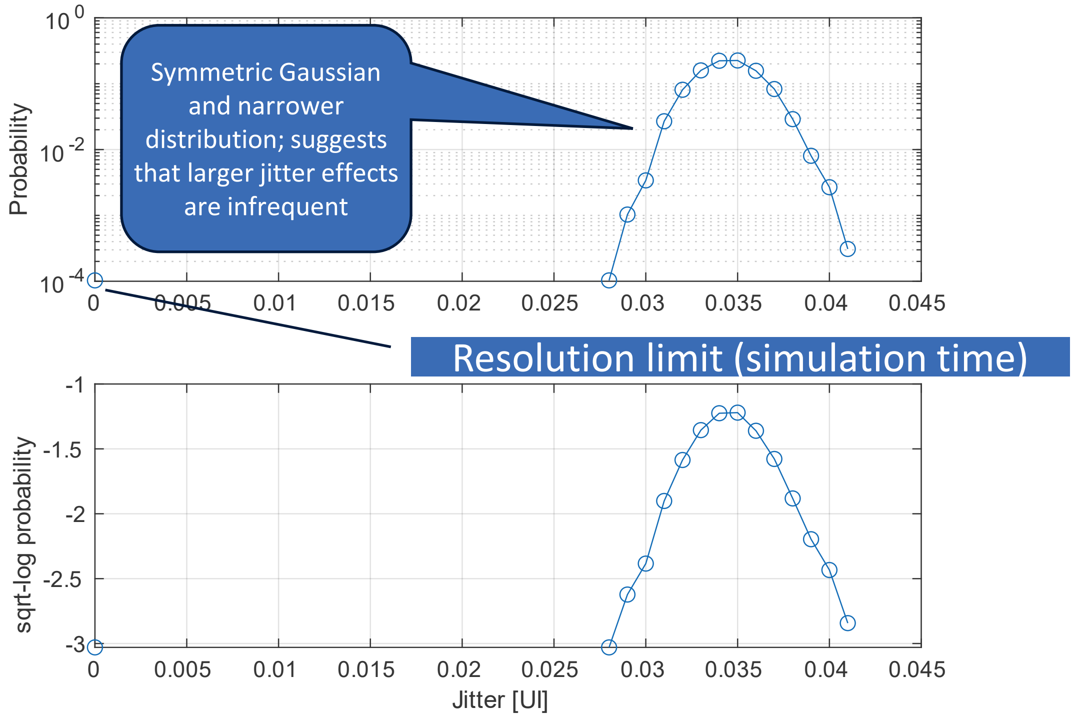


jitter_16 histograms

Combined SJ+RJ with 100 MHz LPF



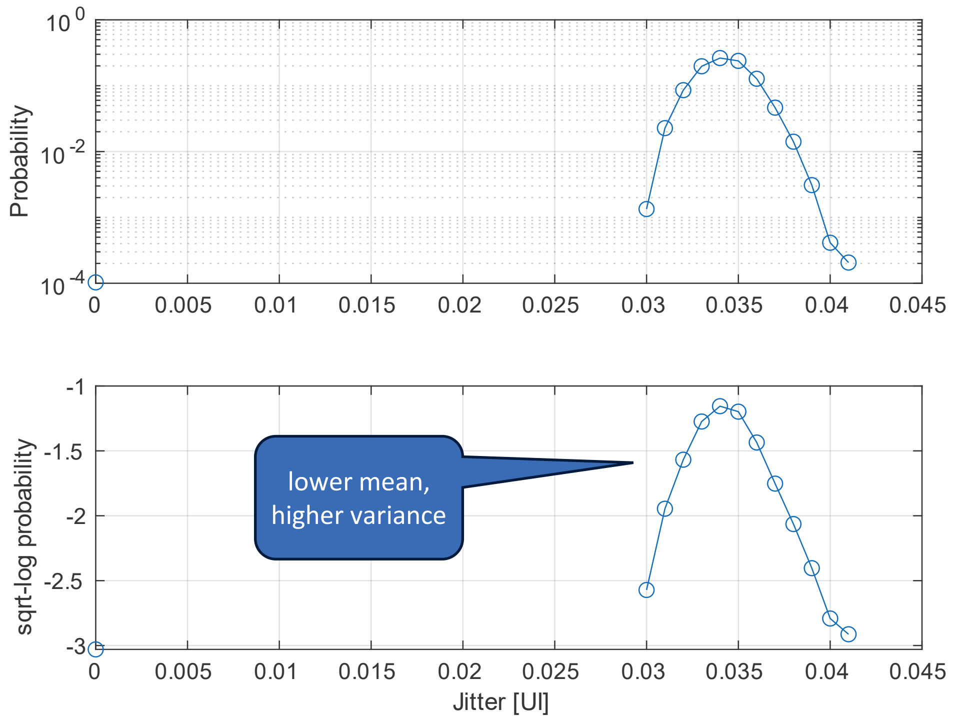
Combined SJ+RJ with 1 GHz LPF



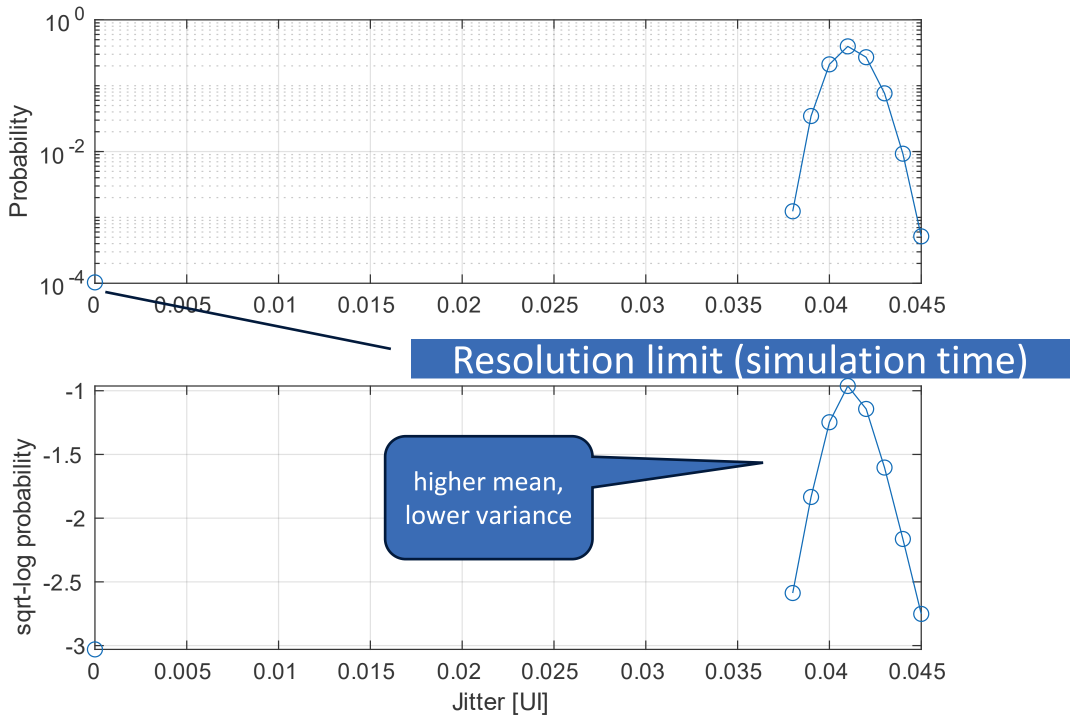
Bottom plots are “linearized” versions of the top ones

jitter_16 histograms

Combined SJ+RJ with 100-1000 MHz BPF



Combined SJ+RJ, no filter (wideband)



Notes and Thoughts

1. jitter_16, as introduced here, is assumed (without proof) to be indicative of the jitter effect on FEC performance
   - Because 16 FEC symbols see at least this amount of jitter in 1 or more UI
   - If the jitter_16 value is outside of the “eye width” (uni-directional jitter margin) then having 16 errors in one codeword is probable
     - The effect of jitter is combined with other interferers such as residual ISI and noise
     - Jitter margin is design-dependent, but with DSP equalizers it is likely <<0.25 UI
     - This is relevant for optics too
   - Measuring this metric may be too onerous, but it was easy to check in simulation
   - There may be better metrics
2. SJ+RJ combination has lower J3u as the dual-Dirac model
   - As shown by S3U measurement in the combined SJ+RJ cases
     - Because SJ does not take the extreme values with such high probability
   - Real transmitters can have periodic jitter that is worse than SJ
     - Arguably the current J3u limits are somewhat relaxed
     - Testing with SJ may be less stressful than with real transmitters

Notes and thoughts

3. Apparently narrow-band jitter creates worse effects on FEC performance
    - Jitter from real transmitters is more likely to be concentrated at low frequencies than "white"
        - Jitter frequencies right above the CDR bandwidth is likely important
        - Frequencies below the CDR bandwidth are attenuated 20 dB/decade, but the residual jitter can still be harmful
    - Can we penalize transmitters more for jitter below some frequency (e.g., 20 MHz)?
        - Otherwise, receiver testing with wide-band RJ may be under-stressing compared to some transmitters
4. Such temporal properties of jitter would not be captured by plain histograms such as the one used in TDECQ
    - As seen in the OIF presentation

Summary

- Effect of some profiles of jitter on FEC performance were explored using a specific metric jitter_16 (max jitter that exists in at least 16 FEC symbols)
- The simulation results follow the trends shown in oif2024.449.02
- Emphasizing the need for jitter measurement and some learnings
  - “average” metrics (such as J_{RMS}) are not as indicative of performance as “extreme” metrics (such as J3u)
  - Excessive RJ is more harmful than SJ
  - Narrow-band RJ is more harmful with wide-band RJ of the same RMS
  - Lower measured jitter is always better
- There is room for more exploration

That’s all

Discussion / questions

Backup

Simulation setup (Simulink)