Rethinking the 800GBASE-ER1 model

Tom Huber (Nokia), Gary Nicholl (Cisco), Jeff Slavick (Broadcom), Eugene Opsasnick (Broadcom), Andras deKoos (Microchip), Mike Sluyski (Cisco), Dave Ofelt (Juniper)

Supporters

- John D’Ambrosia – Futurewei, US subsidiary of Huawei
- Matt Brown – Alphawave

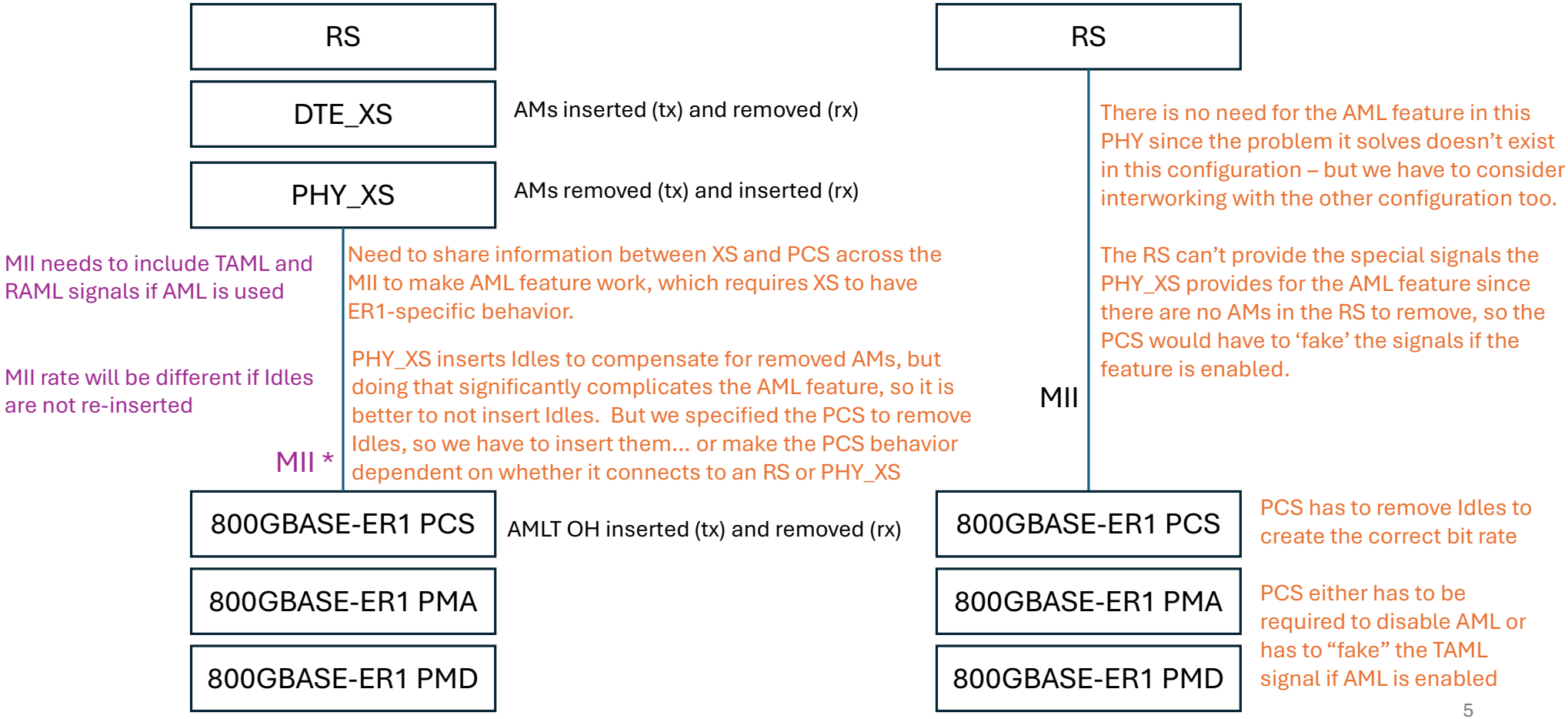
How did we get here?

- As we continued to fill in the details for 800GBASE-ER1 and 800GBASE-ER1-20, using a separate ER1 PCS, the following challenges were discovered:
  - 800GBASE-ER1 is a new PHY family
  - The feature for conveying alignment marker location requires introducing new modes of operation to the 800G XS
  - The description of the functions in the XS and ER1 PCS is not well-aligned with anticipated implementations because the interface between the XS and the PCS is the MII, whereas practical implementations are mapping 257b blocks directly into the ER1 frame structure
  - The use of the XS cannot be mandated, which increases complexity in the PCS
- These challenges introduce potential schedule risk for WG ballot in May 2025
- There is an alternative architecture that avoids the complexity and mitigates the schedule risk

Alternative architecture for 800GBASE-ER1

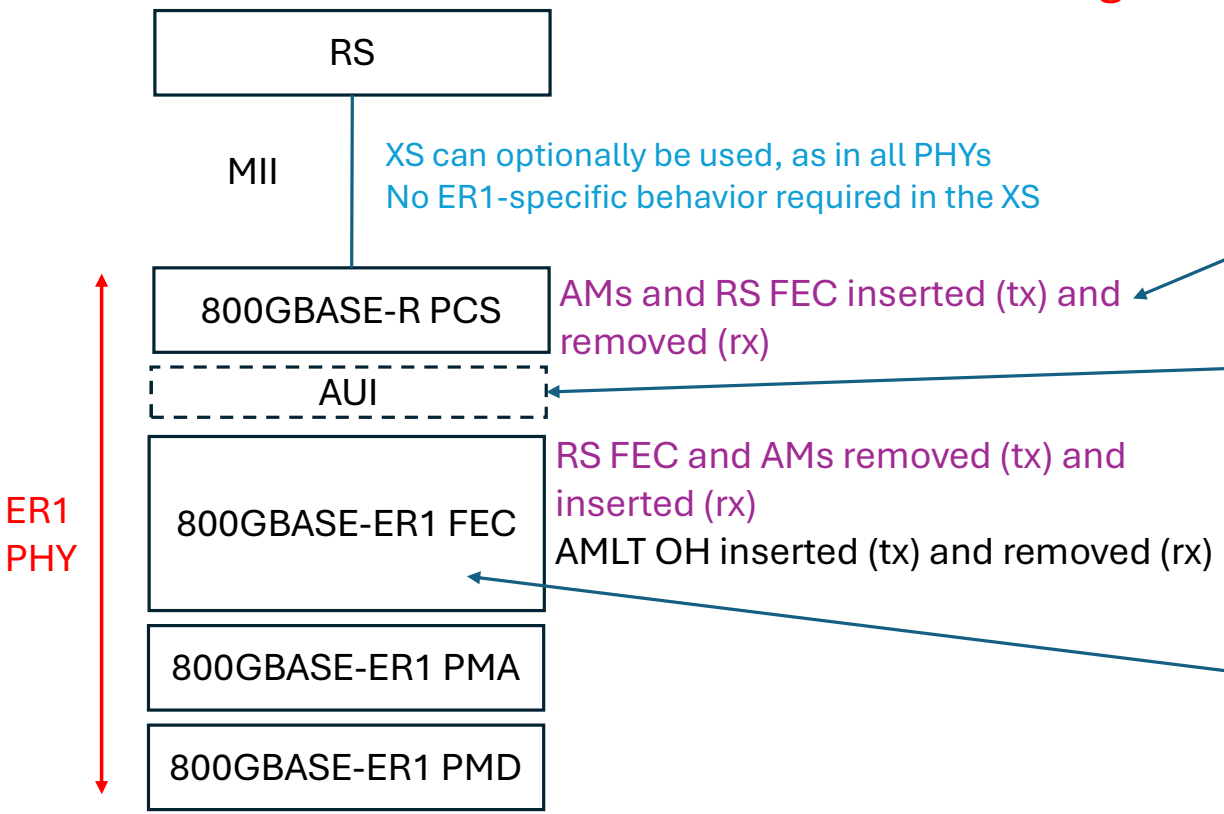
- The challenges are all related to treating ER1 as a separate PCS
  - The original rationale for this was based on ER1 having a separate FEC from 800GBASE-R
  - Implementations using pluggable modules would utilize a segmented FEC architecture since the AUI will use RS(544,514) FEC and the ER1 link will use something else
- An alternative is to use the 800GBASE-R PCS and define an 800GBASE-ER1 FEC sublayer that:
  - Terminates the RS FEC
  - Maps 257b blocks into the ER1 frame and adds the ER1 FEC
- This alternative has the same architecture as 800GBASE-LR1

Current 800GBASE-ER1 model is not self-consistent across possible PHY configurations



Alternative model for 800GBASE-ER1 based on FEC sublayer

This architecture aligns with 800GBASE-FR4, -LR4, and -LR1

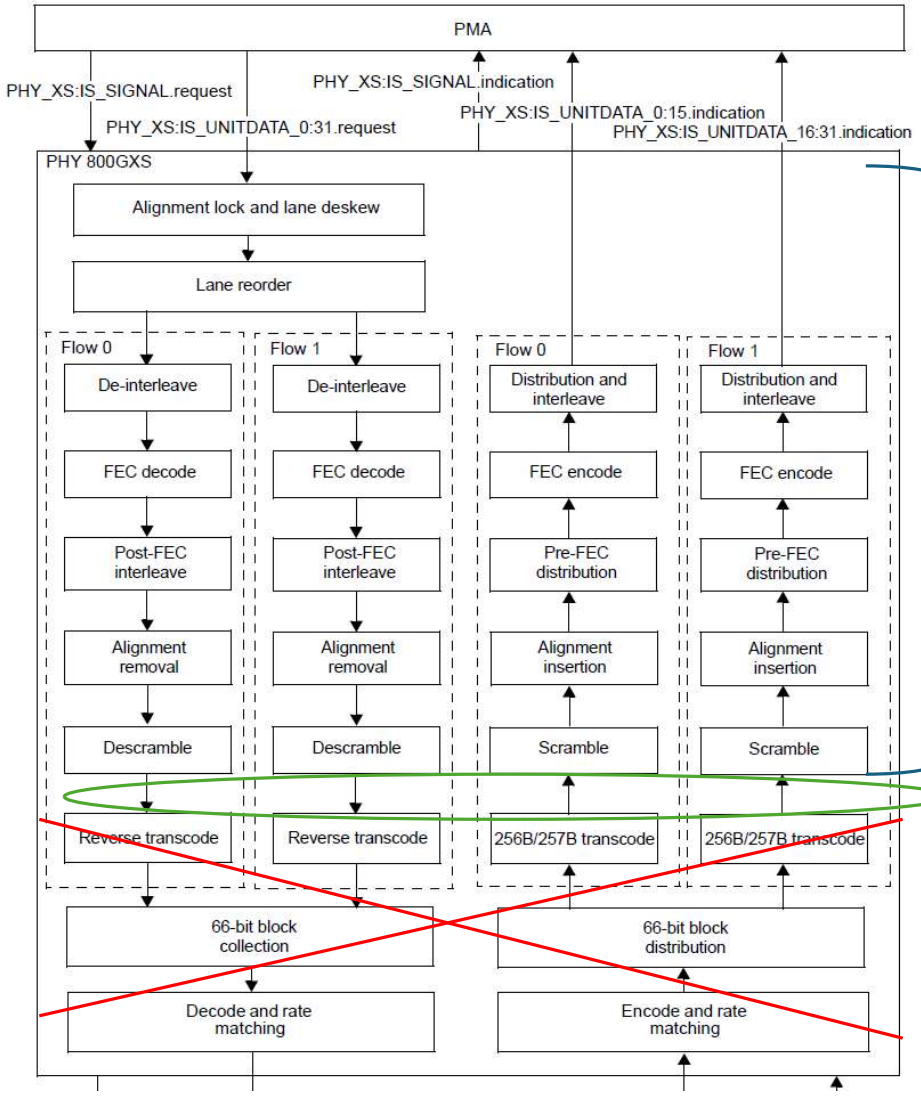


If PCS and FEC sublayers are in the same device (no AUI), purple functions can be omitted in implementation

Most implementations will have at least one AUI, which requires the RS FEC.

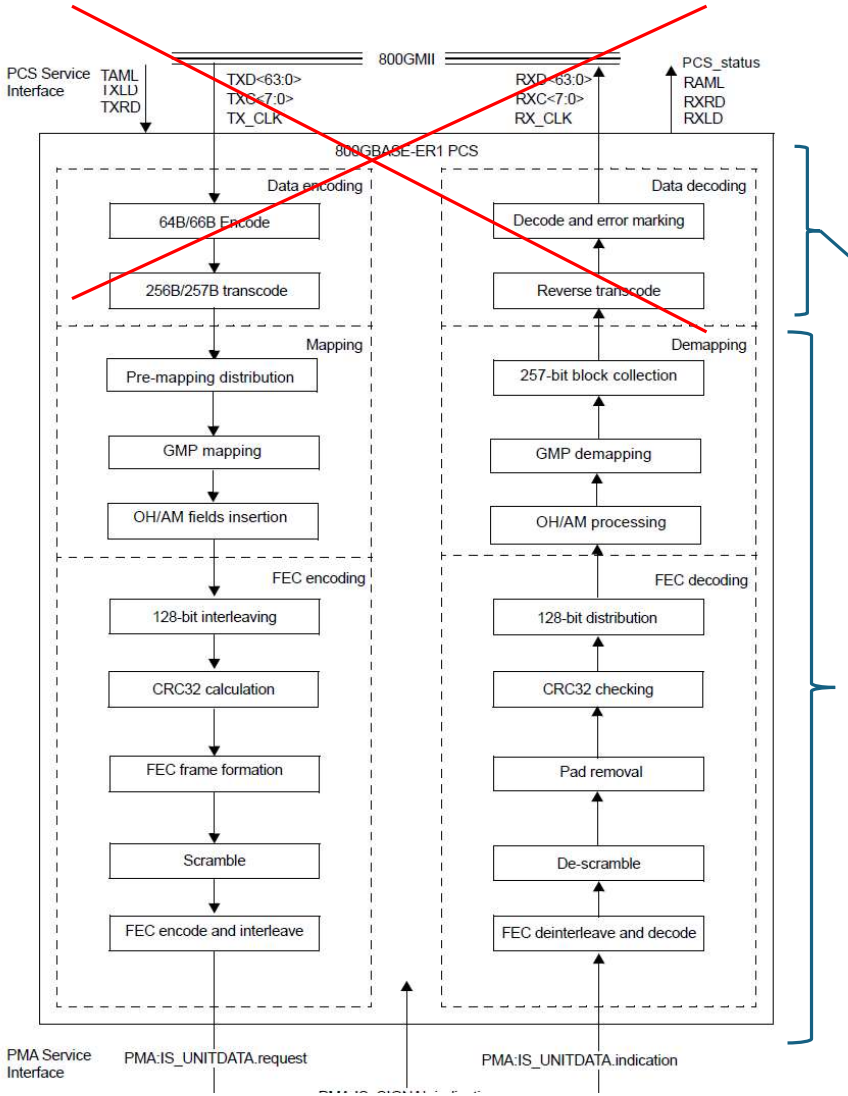
Description of ER1-specific processes (including AMLT feature) is contained in one sublayer and can be done based on 257b blocks, as it will be implemented, rather than based on MII transactions

PHY_XS functions used in ER1 FEC



These processes are incorporated into the ER1 FEC sublayer but can all be specified by reference

Add a “flow merge”/”flow distribute” functions here to merge the two flows to a single stream of 257b blocks in the Tx path and distribute the single path to two flows in the Rx path

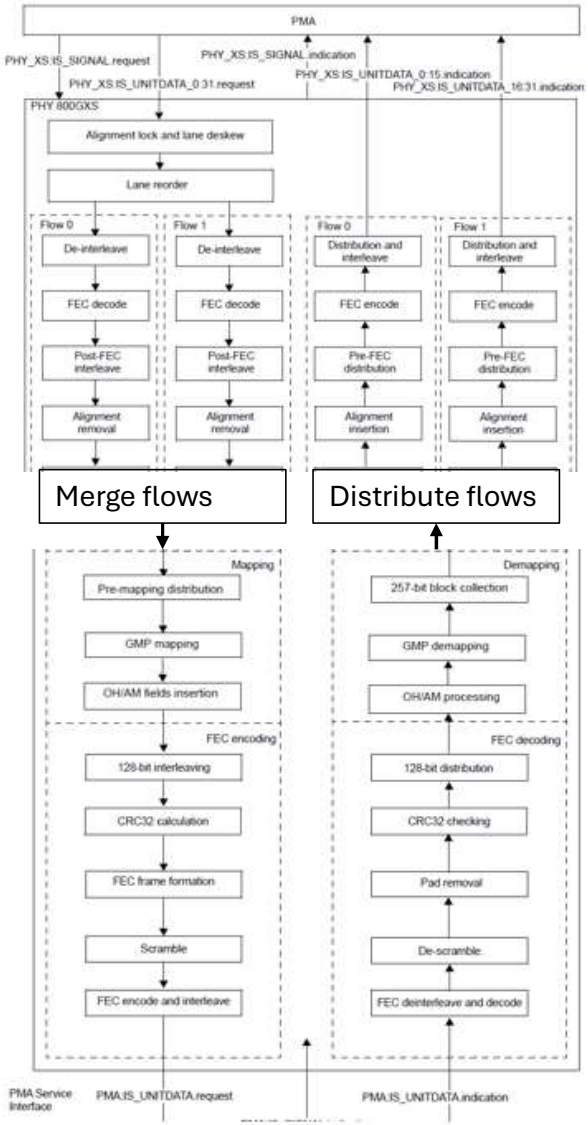


ER1 PCS functions used in ER1 FEC

Replace this Data encoding/decoding block with a “Inverse RS FEC” block that uses functions from the PHY_XS (see previous slide) plus a “flow merge” function to combine the two flows into a single 257b block stream

No changes needed as a result of changing the architecture to a FEC sublayer, other than in description of AML field in the OH/AM fields insertion function

New ER1 FEC sublayer



Functions defined by reference to the PHY_XS

New functions to 802.3dj, but defined already in OIF and ITU-T

Functions currently in 800GBASE-ER1 PCS

Clause 169 changes to reflect alternative architecture

Work in progress…

- Update Table 169-1 to indicate that the 800GBASE-ER1 and ER1-20 PHYs use 800GBASE-R encoding
- Update Table 169-3 to change the title of clause 186, and to include clauses 172, 173, 120F, 120G, 176, 176C, 176D as for LR1
- Remove all changes to 169.2.3
- Add a new 169.2.4c to discuss the ER1 FEC
  - <text proposal to be added>
- Remove the sentence inserted in 169.3 about PHYs that are not part of the 800GBASE-R family
- In the change to 169.3.2, add “or 800GBASE-ER1 FEC” after “Inner FEC”
  - <specific text to be added>
- Add a row to Table 169-4 for ER1 FEC (also a row for the PMA, which is currently missing)

Clause 171 doesn’t need ER1 exceptions

Work in progress…

- Remove everything related to the ER1 PCS alignment marker location transparency feature in these locations:
  - 171.1.1
  - 171.3
  - Figure 171-2
  - 171.3.3
  - 171.6a
  - Table 171-2
  - Table 171-3
  - 171.9.4.6a

Clause 186: Rename the PCS subclause to an ER1 FEC sublayer clause

Work in progress…

- ER1 FEC sublayer include part of what the PHY_XS includes
- The ER1 FEC sublayer would be most of what is in the ER1 PCS clause currently:
  - Remove 66b encoding/rate adaptation and 257b transcoding
  - Rework the AMLT text to be based on 257b blocks rather than MII transactions (the text gets simpler); all the behavior related to this feature is contained within the ER1 FEC sublayer rather than being split between the XS and the PCS
  - Add a function to merge the two flows from the PCS into a single flow prior to mapping with GMP and the corresponding function to distribute to two flows at the demapper (similar to what OIF and ITU already specify)
- The ER1 FEC sublayer is at the same location in the PHY stack as the ‘inner FEC’ for LR1
- The ER1 FEC sublayer can be specified such that no changes are needed to ER1 PMA
- ER1 FEC and PMA sublayers could be combined as they are in 177 and 184
- Need to consider how frame loss ratio and bit error rate is defined
- If the PCS and FEC are co-located in an implementation, there are further simplifications that can be achieved wrt not literally adding and removing the RS FEC

AML feature details

Work in progress…

- The AML feature is part of the “OH/AM fields insertion” and “OH/AM processing” functions
- We still need to do many of the things in https://www.ieee802.org/3/dj/public/adhoc/optics/1224_OPTX/slavick_3dj_optx_01_241219.pdf to complete specification of the AML feature
- The exact details of what changes need to be made depend on how the ER1 PHY is modeled (and are not the subject of this presentation)

Proposal

- Change the model of ER1 from a PCS to a FEC sublayer
  - All 800G PHYs use the same PCS
  - All 800G PHYs use the same optional XS
  - FEC-specific aspects are captured in FEC sublayers for all PHYs that use FEC beyond/other than RS(544,514)
  - Better alignment with real-world implementation enables simpler description
- This is purely a change in documentation structure, not a change in functionality