Deskew in 800GbE/1.6TbE for Inner FEC (CL177)

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Motivation

- Recap: The Inner FEC Convolutional Interleaver is to guarantee 12 RS symbols that form the Inner FEC Hamming payload are from 12 different RSFEC Codewords, i.e. 12-way RS Interleaved
- Input of the Inner FEC Convolutional Interleaver is output from CL-176 SM-PMA
- 3 delay lines are used to create 12-way RS interleaved with the RS-interleaved from CL176 SM-PMA
- As input to each delay lines are from different PCSLs, input skew from these PCSLs can (partially) undo the effect of the Convolutional Interleaver Delay Lines.

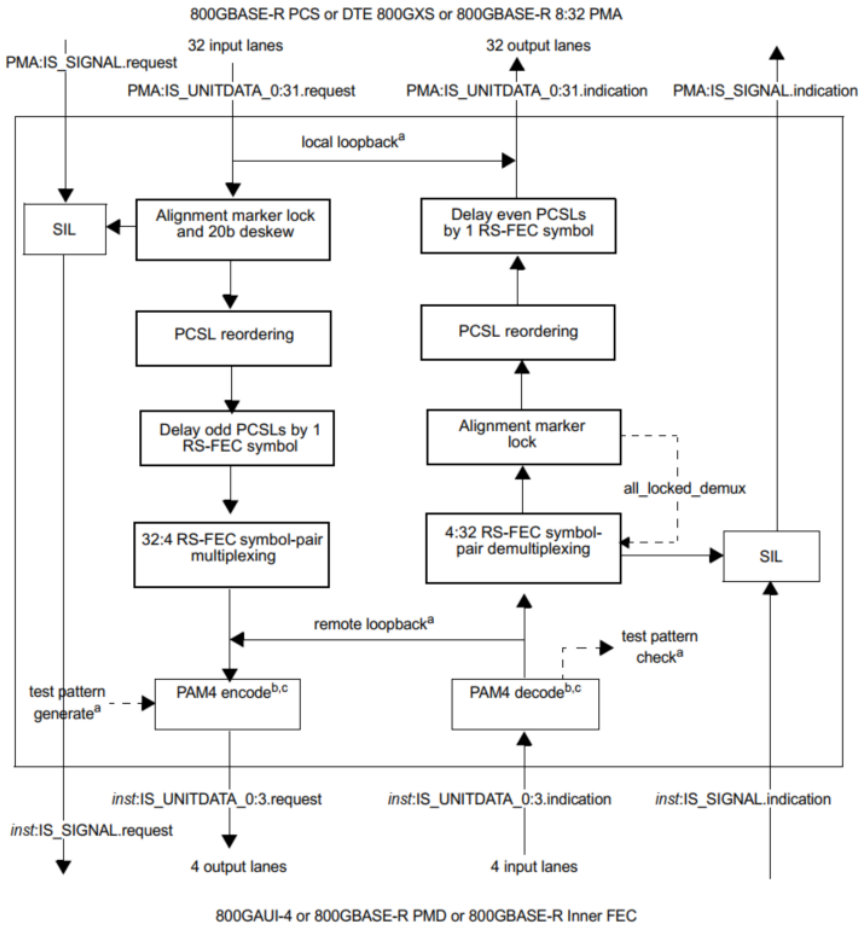
Skew output of SM-PMA (CL176): 200GE/400GE

- 200GE/400GE: per *"shrikhande_3dj_01a_2406.pdf"*, skew output of the SM-PMA lane(s) is deterministic :
  - All even PCSLs are aligned
  - All odd PCSLs are 1370/690 bits delayed compared to even PCSLs
  - The Skew introduced by different delays in 200G per lane C2C or C2M links between the SM-PMA and the FECi input does not change the skew within the 200G lanes

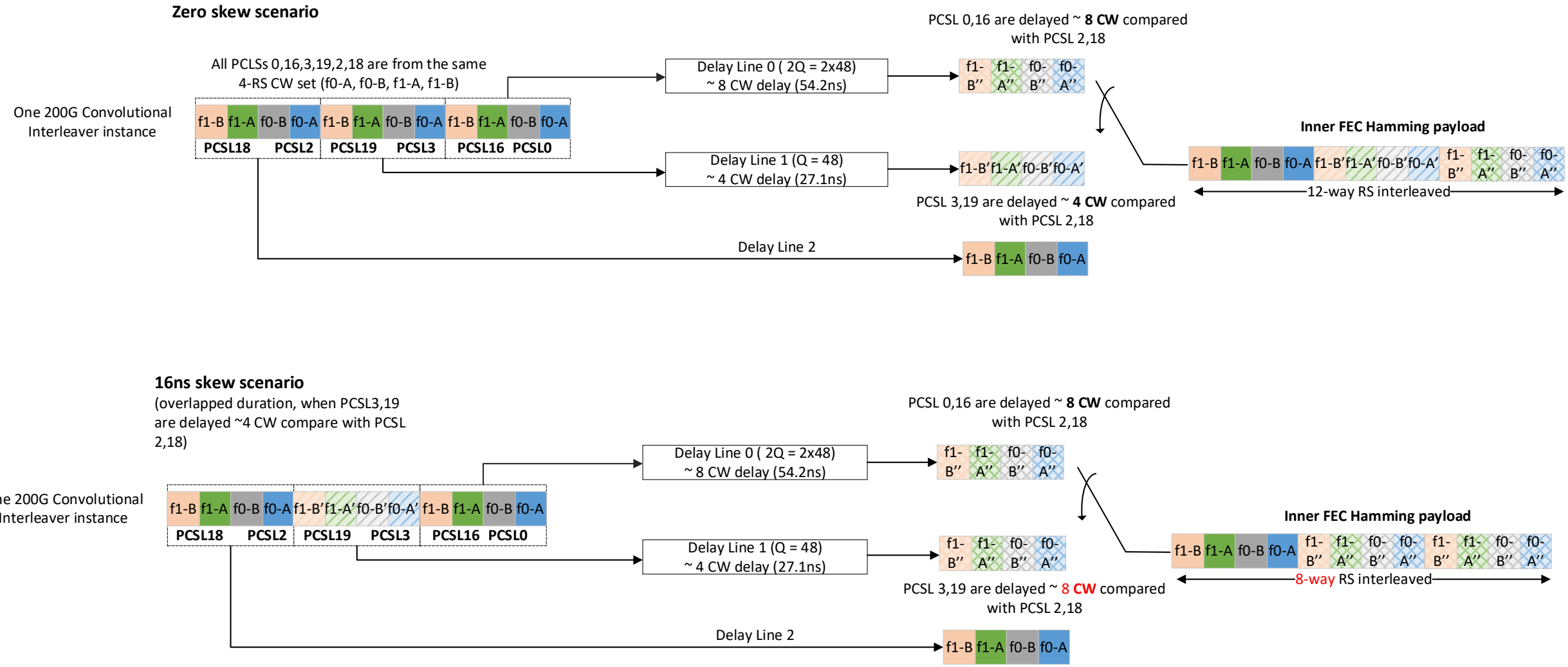
- As a result, the Inner FEC Convolutional Interleaver which operates on a 200G lane basis can guarantee 12-way RS Interleaved

Skew output of SM-PMA (CL176): 800GE

- 800GBASE-R 8:32 PMA can have 16ns skew, which is ~ 0.625 x 4CW
- 20b deskew in 800GE SM-PMA is not enough to align RSFEC CW between PCSLs

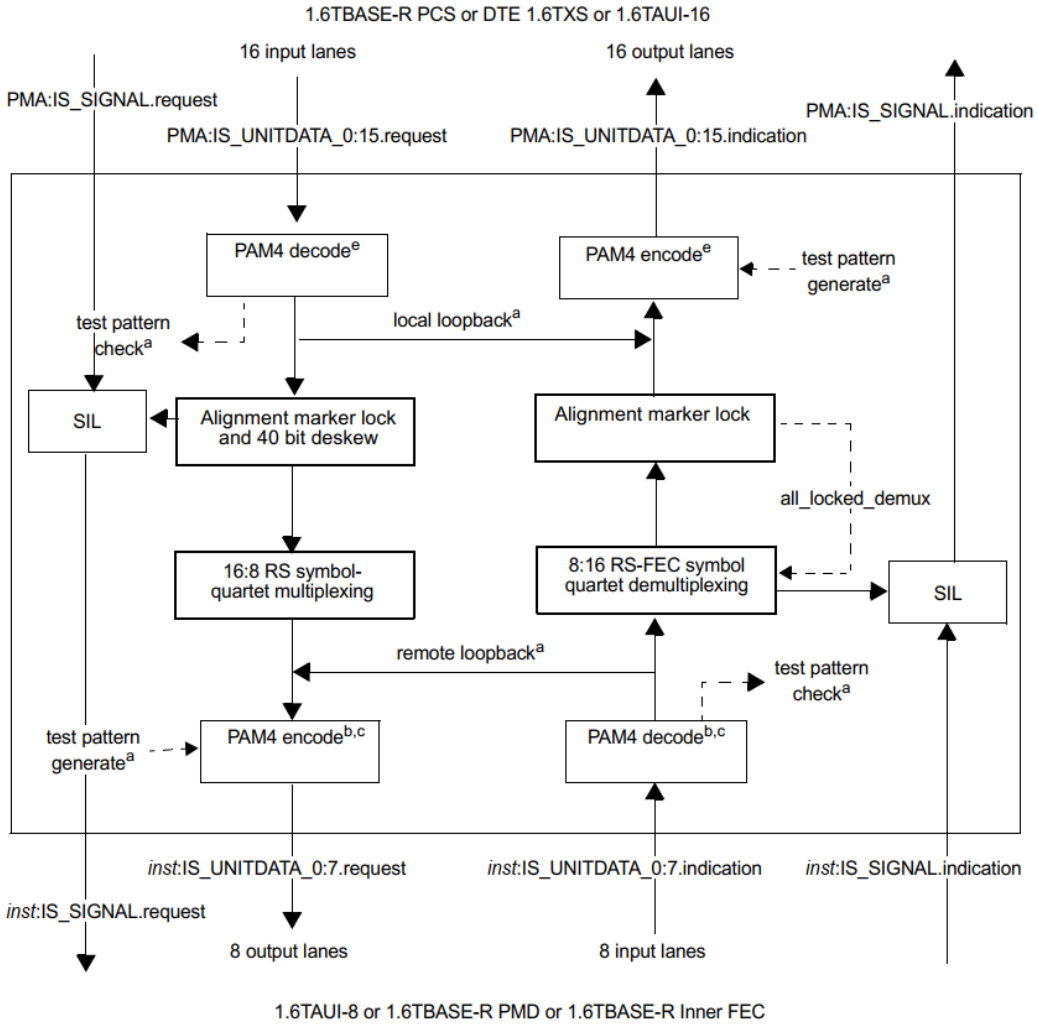


Skew impact to Inner FEC Convolutional Interleaver Illustration (800GE)

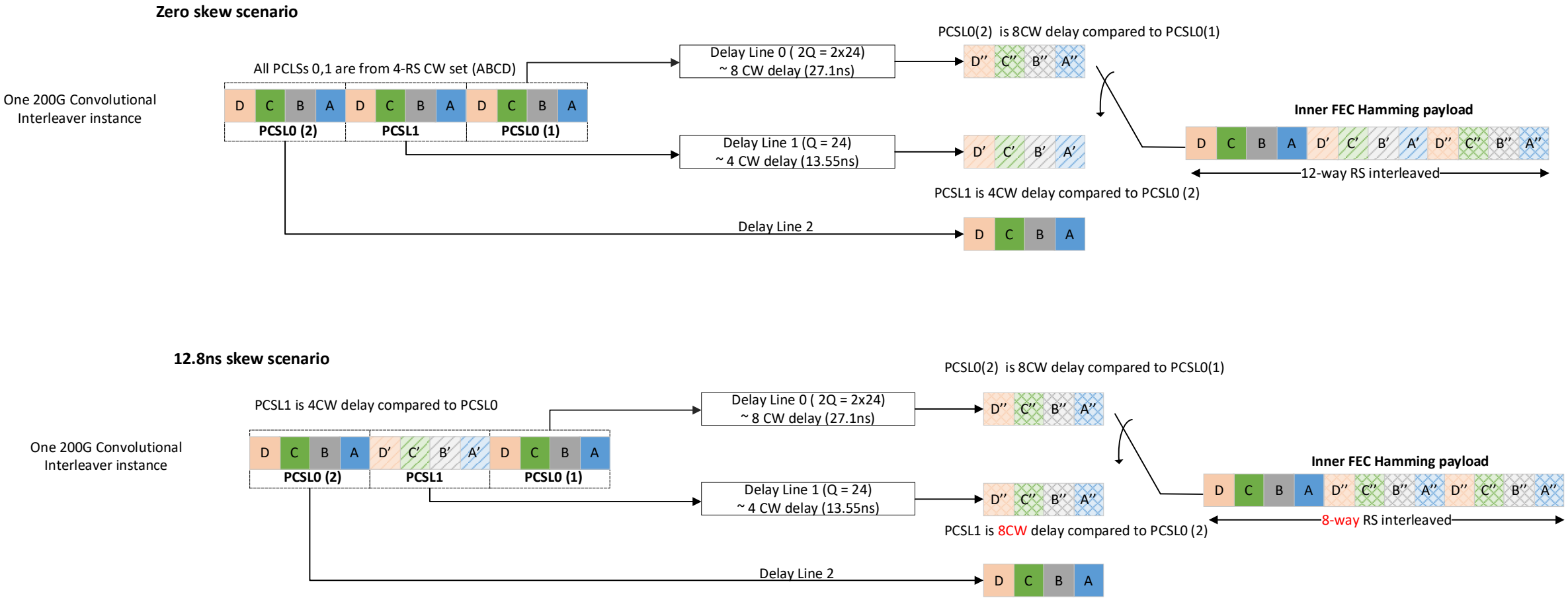


Skew output of SM-PMA (CL176): 1.6TbE

- 1.6TAUI-16 can have 16ns skew (SP1), which is ~ 1.25 x 4CW (*per Table 174–5—Summary of Skew constraints*)
- 40b deskew in 1.6TbE SM-PMA is not enough to align RSFEC CW between PCSLs

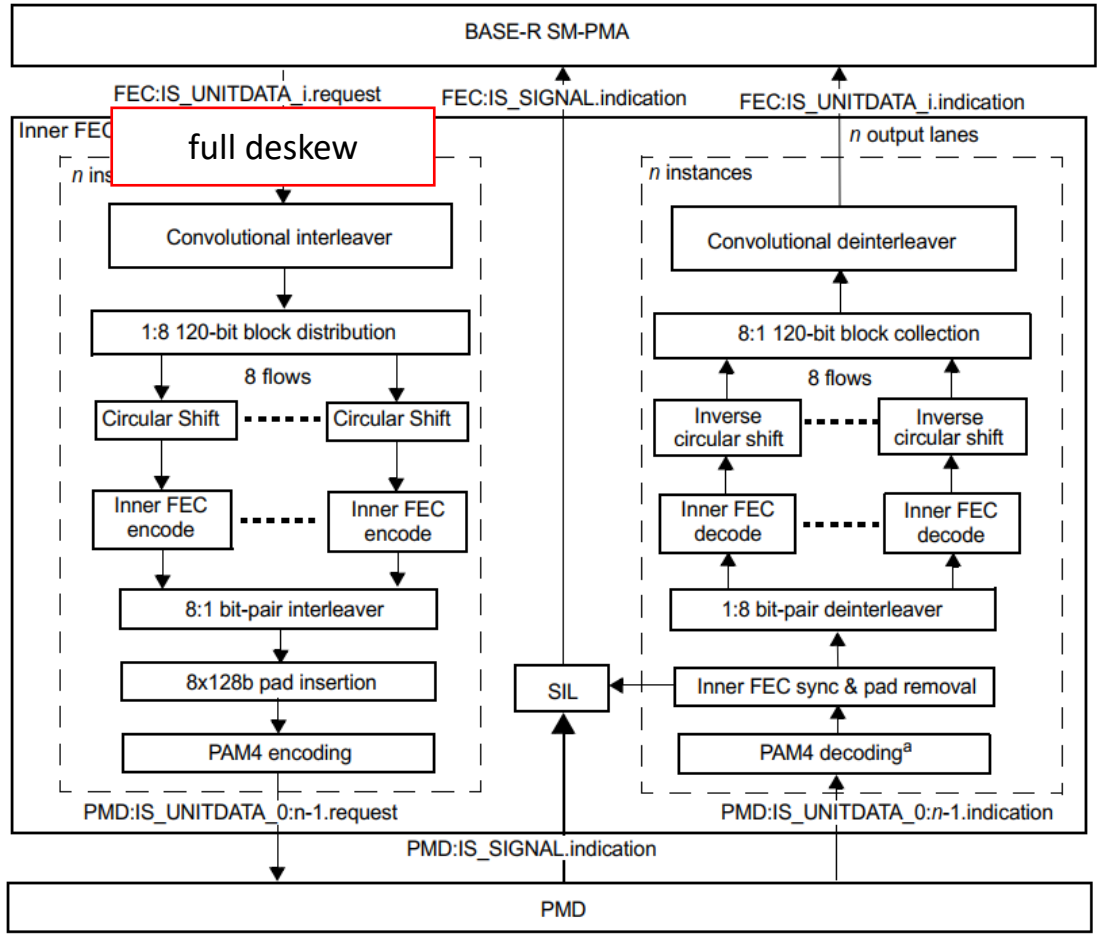


Skew impact to Inner FEC Convolutional Interleaver Illustration (1.6TbE)



Deskew for Inner FEC Convolutional Interleaver Proposal

- Add full-deskew to align RSFEC CW between PCSLs, either within PMA lane or across PMA lanes so that output of the Convolutional Interleaver is always 12-way RS Interleaved
  - Full deskew memory needed should be more than 16ns (SP1) but less than 25ns (SP2) for both 800GE and 1.6TbE
- Another option is to extend the “CW boundaries deskew” proposed in “*shrikhande_3dj_01a_2406.pdf*” to support full deskew for 800GE 8:4 SM-PMA and 1.6TbE 16:8 SM-PMA
  - This requires less memory than 4CW boundaries deskew for 200GE/400GE



[a] Optional when soft-decision decoding is used.

Figure 177–2—Functional block diagram

Backup