# DR / DR-x MDI: Support for Breakout (Comments #341 and #342)

## IEEE P802.3dj Task Force
## Optical / Logic Ad hoc Meeting
## 29 August 2024


- John D'Ambrosia, Futurewei, U.S. Subsidiary of Huawei
- Matt Brown, Alphawave Semi


# Introduction

- The following presentation addresses the following comments
  - **Comment #341** (SC 180.8.3.1) - Any DR MDI is also capable of supporting any lower lane count DR interfaces than what it is specified for as applicable, as well as combinations. Clause 180.8.3.1.1 starts off specifying 400GBASE-DR2 with twelve total positions. It could support multiple ports of 200GBASE-DR1, or could support a combination of a single 400GBASE-DR2 with two ports of 200GBASE-DR1.
  - **Comment #342** (SC 182.8.3.1~~1~~) - Any DRx-2 MDI is also capable of supporting any lower lane count DRx-2 interfaces than what it is specified for as applicable, as well as combinations. Clause 182.8.3.1.1 starts off specifying 400GBASE-DR2-2 with twelve total positions. It could support multiple ports of 200GBASE-DR1-2, or could support a combination of a single 400GBASE-DR2-2 with two ports of 200GBASE-DR1-2.
- "Breakout" scenarios can be supported – why wouldn't we?
  - Annex 162C addresses MDIs for 100GBASE-CR1, 200GBASE-CR2, and 400GBASE-CR4, and 800GBASE-CR8
  - Annex 179C addresses MDIs for 200GBASE-CR1, 400GBASE-CR2, 800GBASE-CR4, and 1.6TBASE-CR8
  - QSFP-DD maps electrical signal to optical port mapping (Per Rev 7.0 - QSFP112 specifications removed from QSFP-DD and forwarded to SNIA.)
  - OIF CMIS - The CMIS specification also explicitly defines the mapping of groups of electrical lanes to particular fibers, though it does not specifically identify lanes numbers within a group.
  - **See section 6.2.1.3.** **https://www.oiforum.com/wp-content/uploads/OIF-CMIS-05.2.pdf**
- This presentation will initiate discussion on how DRx / DRx-2 MDI's could be specified to address break-out.

# Background (Comment #341)

- Mapping DR2 and DR4 MDI lane assignments to the same connector
- For both assignments
  - Only single port of target PHY defined
  - Lower lane count PHYs could be supported
- Multiple PHY types could be mapped to the same connector in different configurations

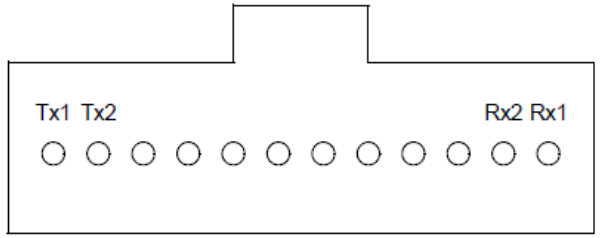


Figure 180–7—400GBASE-DR2 optical lane assignments

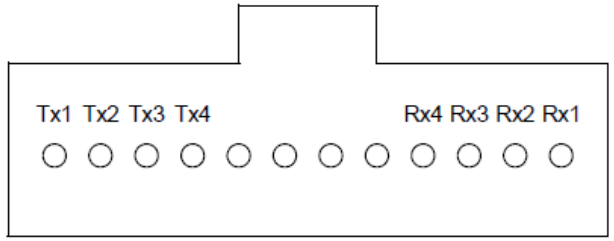


Figure 180–8—800GBASE-DR4 optical lane assignments

# Background (Comment #341) - continued

- **Only single port of target PMD implemented**
- **Multiple PHY types could be mapped to the same connector in different configurations**

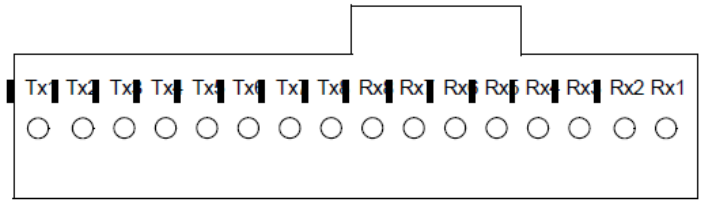


Figure 180–9—1.6TBASE-DR8 optical lane assignments

# Background (Comment #342)

- Mapping DR2-2 and DR4-2 MDI lane assignments to the same connector
- For both assignments
  - Only single port of target PHY defined
  - Lower lane count PHYs could be supported
- Multiple PHY types could be mapped to the same connector in different configurations

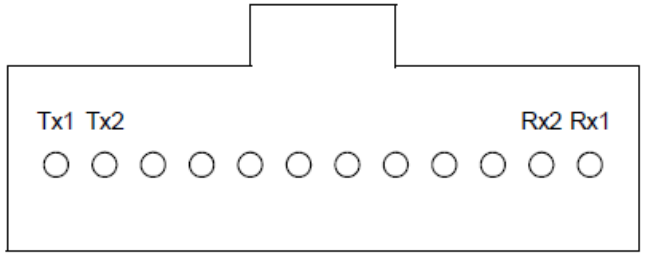


Figure 182–7—400GBASE-DR2-2 optical lane assignments

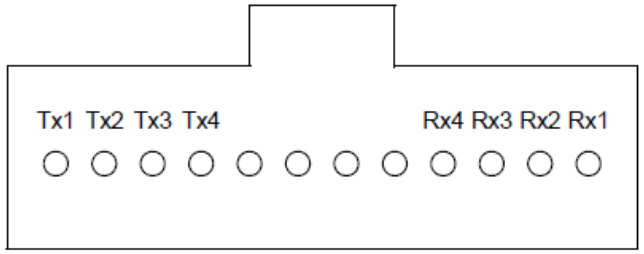


Figure 182–8—800GBASE-DR4-2 optical lane assignments

# Background (Comment #342) - continued

- **Only single port of target PMD implemented**
- **Multiple PHY types could be mapped to the same connector in different configurations**

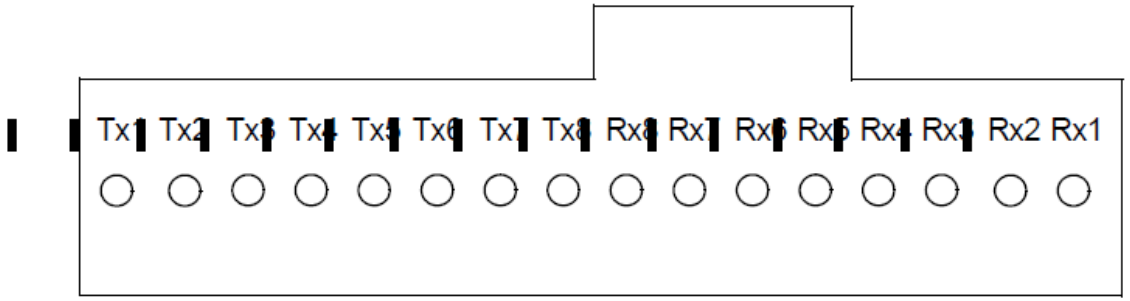


**Figure 182–9—1.6TBASE-DR8 optical lane assignments**

- **Note – Caption to Fig 182-9 is incorrect – it should be 1.6TBASE-DR8-2**

# Going Forward

- Any connector could support
  - A single PHY MDI
  - Multiple PHY types and configurations
- To gauge interest, we will focus on the single row 16-fibre interface

# IEEE 802.3 - CR – 1:1 mapping logical PMD/MDI lanes to to connector contacts

**Similar to IEEE P802.3dj, Tables 179C-2 / 179C-4**

Source: IEEE Std 802.3ck-2022

Table 162C–2—PMD to connector signal assignments

| PMD signal <PMD number>:<PMD signal> | | | | Connector signal |
|---|---|---|---|---|
| 100GBASE-CR1 | 200GBASE-CR2 | 400GBASE-CR4 | 800GBASE-CR8 | |
| 1-lane 0:DL0n | 0:DL0n | 0:DL0n | 0:DL0n | DL0n |
| 1-lane 0:DL0p | 2-lane 0:DL0p | 0:DL0p | 0:DL0p | DL0p |
| 1-lane 1:DL0n | 2-lane 0:DL1n | 0:DL1n | 0:DL1n | DL1n |
| 1-lane 1:DL0p | 0:DL1p | 4-lane 0:DL1p | 0:DL1p | DL1p |
| 1-lane 2:DL0n | 1:DL0n | 0:DL2n | 0:DL2n | DL2n |
| 1-lane 2:DL0p | 2-lane 1:DL0p | 0:DL2p | 0:DL2p | DL2p |
| 1-lane 3:DL0n | 1:DL1n | 0:DL3n | 0:DL3n | DL3n |
| 1-lane 3:DL0p | 1:DL1p | 0:DL3p | 8-lane 0:DL3p | DL3p |
| 1-lane 4:DL0n | 2:DL0n | 1:DL0n | 0:DL4n | DL4n |
| 1-lane 4:DL0p | 2-lane 2:DL0p | 1:DL0p | 0:DL4p | DL4p |
| 1-lane 5:DL0n | 2:DL1n | 1:DL1n | 0:DL5n | DL5n |
| 1-lane 5:DL0p | 2:DL1p | 4-lane 1:DL1p | 0:DL5p | DL5p |
| 1-lane 6:DL0n | 3:DL0n | 1:DL2n | 0:DL6n | DL6n |
| 1-lane 6:DL0p | 2-lane 3:DL0p | 1:DL2p | 0:DL6p | DL6p |
| 1-lane 7:DL0n | 3:DL1n | 1:DL3n | 0:DL7n | DL7n |
| 1-lane 7:DL0p | 3:DL1p | 1:DL3p | 0:DL7p | DL7p |
| 0:SL0n | 0:SL0n | 0:SL0n | 0:SL0n | SL0n |
| 0:SL0p | 0:SL0p | 0:SL0p | 0:SL0p | SL0p |
| 1:SL0n | 0:SL1n | 0:SL1n | 0:SL1n | SL1n |

Mapping of logical PMD lanes to physical connector lanes is explicitly defined for non-breakout and breakout cases. Therefore, for each Ethernet group, lane 0 is explicit.

Table 162C–4—MDI connector contact mapping for QSFP112 and QSFP-DD800

| QSFP112 | QSFP-DD800 | Connector signal name | Description |
|---|---|---|---|
| 1 | 1 | GND | Ground |
| 2 | 2 | SL1n | Transmitter inverted data input |
| 3 | 3 | SL1p | Transmitter non-inverted data input |
| 4 | 4 | GND | Ground |
| 5 | 5 | SL3n | Transmitter inverted data input |
| 6 | 6 | SL3p | Transmitter non-inverted data input |
| 7 | 7 | GND | Ground |
| 13 | 13 | GND | Ground |
| 14 | 14 | DL2p | Receiver non-inverted data output |
| 15 | 15 | DL2n | Receiver inverted data output |
| 16 | 16 | GND | Ground |
| 17 | 17 | DL0p | Receiver non-inverted data output |
| 18 | 18 | DL0n | Receiver inverted data output |
| 19 | 19 | GND | Ground |
| 20 | 20 | GND | Ground |
| 21 | 21 | DL1n | Receiver inverted data output |
| 22 | 22 | DL1p | Receiver non-inverted data output |

# QSFP-DD Mapping

- **Source:**
- **"QSFP-DD/QSFP-DD800/QSFP112 Hardware Specification for QSFP DOUBLE DENSITY 8X AND QSFP 4X PLUGGABLE TRANSCEIVERS", Revision 6.01, May 28, 2021**
  - **http://www.qsfp-dd.com/wp-content/uploads/2022/07/QSFP-DD-Hardware-Rev6.3-final.pdf**
  - **See Clause 6.1 Electrical data input/output to optical port mapping**
  - **See Table 24**
  - **Per Rev 7.0 - QSFP112 specifications removed from QSFP-DD and forwarded to SNIA.**
- **Module mapping from electrical input to optical fibers is explicit.**
- **However, the grouping of electrical inputs into Ethernet groups is not defined. But it does specify how groups of electrical lanes are mapped to a single fiber (e.g., for electrical or wavelength multiplexing).**
- **It is therefore not clear which groups of TX outputs would be mapped to a single Ethernet rate, nor which we might deem to be "lane 0".**
- **Nor is it defined whether like ports will be connected at each end of the fibers.**

# Moving Forward

- Single PHY MDIs can remain as is, however…
- Technology reuse key aspect of IEEE P802.3dj project.
- To address a connector supporting multiple PHY types and configurations
  - Same approach as what is done for CR (100G to 800G, 200G to 1.6T) PHYs can be re-used to address a single-row 16-fiber interface for appropriate PHYs ( 1) DR1, DR2, DR4, DR8; and 2) DR1-2, DR2-2, DR4-2, DR8-2)
  - Same basic approach can also be applied to a single-row twelve-fiber interface for appropriate PHYs ( 1) DR1, DR2, DR4; and 2) DR1-2, DR2-2, DR4-2)
- If there is interest then a more detailed proposal will be brought forward for consideration at the Sept Interim