Issue with implementation of "full deskew" for Clause 177 (comment #159 against D1.1)

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IEEE 802.3dj Logic/Optics ad-hoc, 17 Oct 2024

Introduction

• This contribution highlights an issue found when addressing comment #159 against D1.1, related to implementing "full deskew" for 800G/1.6T in Clause 177 (IMDD InnerFEC).

Background

- Mike Dudek presented <u>dudek_3dj_optx_01_240627</u> at the joint optics/logic ad-hoc on 6/27/2024 and showed that skew generated between PCSL's in the 50/100G per lane PMA's and AUIs can (partially) undo the effect of the Convolutional Interleaver Delay Lines for 800G and 1.6T for the IMDD InnerFEC (Clause 177).
- Mike presented an update to this contribution at the July plenary in Montreal (<u>dudek_3dj_01_2407</u>)
- This contribution proposed several possible solutions
- Following a lengthy discussion, a straw poll was taken with option #2 having the most support (see next slide)

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Straw Poll #TF-2
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To address the de-skew issue for 800GbE/1.6TbE Inner FEC (Clause 177) identified in dudek_3dj_01_2407, the de-skew function should be addressed in:

- A. Within Clause 177 Inner FEC sublayer (option 2 in dudek_3dj_01_2407)
- B. Within Clause 176 SM-PMA sublayer (option 3 in dudek_3dj_01_2407) c. Need more information

(choose one)

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Results (all): A: 59, B: 17, C: 21
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Source: https://www.ieee802.org/3/dj/public/24 07/motions 3dj 2407.pdf

Comment #159 - final response

- Comment #159 was submitted by Mike Dudek against D1.1 to address the issue identified in his earlier contributions.
- Based on the results of the straw poll taken in July, the final response to comment #159 was to implement option #2 in dudek_3dj_01_2407 for 800G/1.6T.

C/ 177	SC	177.1.3	P269	L7	# 159
Dudek, Mil	ke		Marvell		
Comment	Туре	TR	Comment Status A		Deskew
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Suggested	Remed	ly			
Impler descri	nent ful bed as	l de-skew option 2 o	at the input to the convoluti n slide 5 of that presentation	onal interleaver	r for 800G and 1.6T as
Response			Response Status C		
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Based the su	on the	results of d remedy (straw poll #TF-2 there is str option 2 in dudek 3di 01 2	rong support for 2407).	r the option called out in

Implement the suggested remedy with editorial license

Implementation of comment #159

- When the editorial team were implementing comment #159, it was realized that the solution is not as simple some of us had initially thought
- The reason is that the service interface to clause 177 is based on 200G symbol-muxed lanes, and not PCS lanes
- This means that the "deskew" function cannot simply reference the "deskew" function from the PCS clauses (e.g. clause 119, 172, etc), as in these cases the deskew is performed on PCS lanes.
- As a result, the description of the "deskew" function for Clause 177 (see section 177.4.1) was left intentionally vague and an editor's note added to highlight that a more complete proposal is required (see next slide)

D1.2 - "177.4.1 Alignment lock and deskew"

177.4 Transmit function 177.4.1 Alignment lock and deskew In order to maintain the full 12 RS-FEC codeword interleaving depth for the convolutional interleaver, alignment marker lock and deskew shall be provided for 800GBASE-R and 1.6TBASE-R. *Editor's note: Additional guidance is needed to describe the alignment marker lock and deskew process. It*

Editor's note: Additional guidance is needed to describe the alignment marker lock and deskew process. It is different from the PCS and PMA processes due to the 200Gb/s input lanes. This probably requires a new contribution describing the necessary changes to be added in the next draft

This function is not required for 200GBASE-R and 400GBASE-R.

Functional Block diagram

Incoming streams are 200G symbol-muxed (from the SM-PMA above)

Newly added "alignment lock and lane deskew" function (in response to comment #159).

- In order to perform the PCS lane deskew function the 200G input lanes would first have to be symbol-demuxed back to PCS lanes (essentially un-doing the symbol muxing of the SM-PMA layer above)
- Then deskew performed on the PCS lanes
- And finally, the PCS lanes symbol-muxed back to 200G lanes (repeating the function of the SM-PMA layer above).



^a For 800GBASE-R or 1.6TBASE-R

Next steps

- Several solutions to this issue are being discussed, including (but not limited to):
 - Provide a detailed description of the symbol-demuxing and symbol-muxing that is required to support the "alignment lock and deskew" function in 177.4.1 (perhaps by referencing the appropriate sections in Clause 176?)
 - Change to a PCSL based service interface for Clause 177 (similar to what was done for Clause 184).
 - Move the required PCS lane deskew function for 800G/1.6T into the SM-PMA (essentially option #3 in dudek_3dj_01_2407)
- Further discussion and consensus building on this topic is encouraged, ideally leading towards a comment against D1.2 and a complete technical proposal (on how to update the draft).

Thanks