A 212.5 Gbps-PAM4 Chip-to-Module Channel for "Universal Port" and Its Characteristics: Design A

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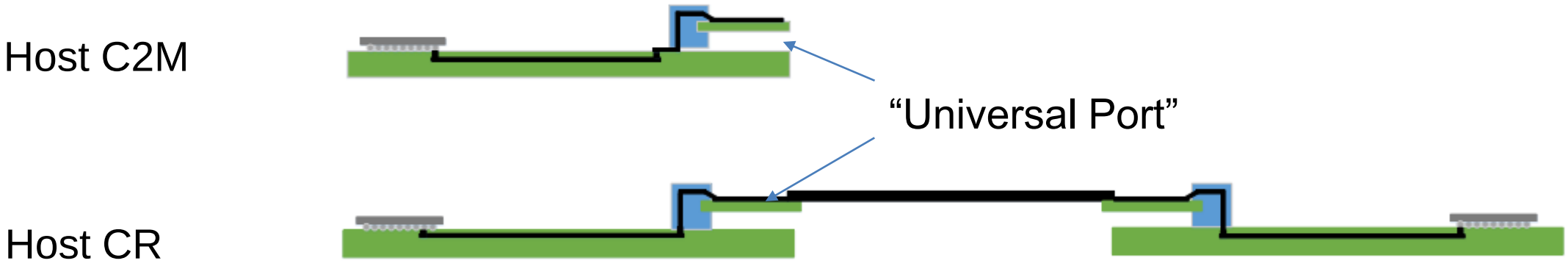
Background and Introduction (I)

- An important and common Chip-to-Module (C2M) Channel is the so-called “Universal Port” C2M, as shown in the following diagram

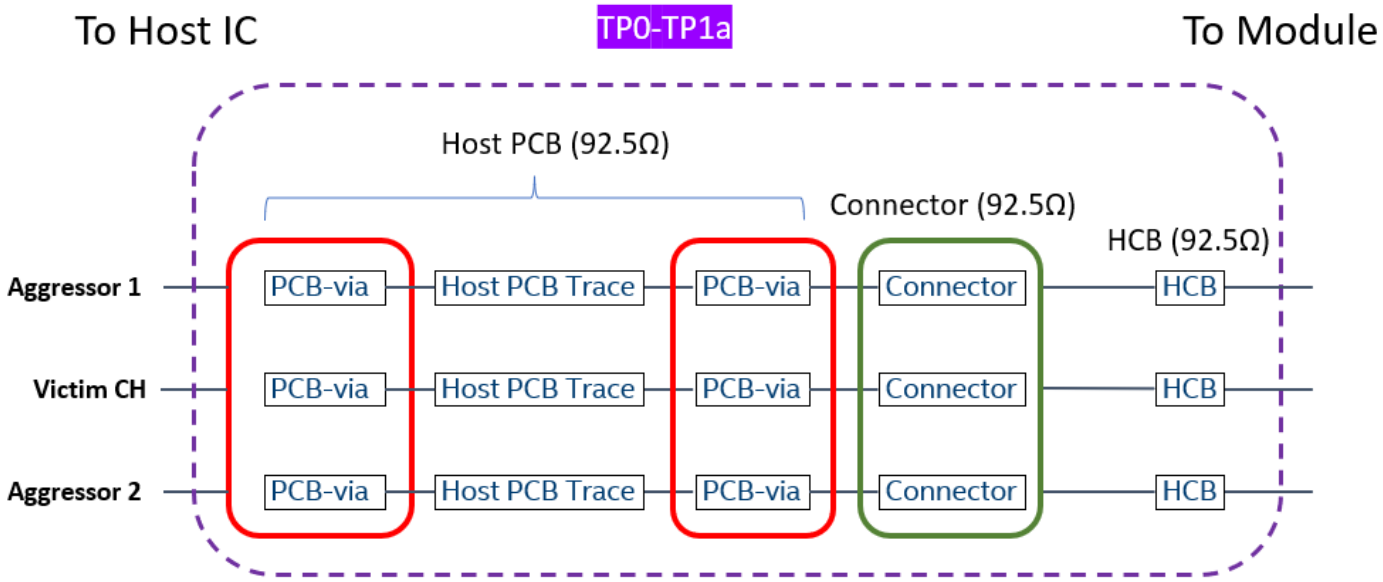


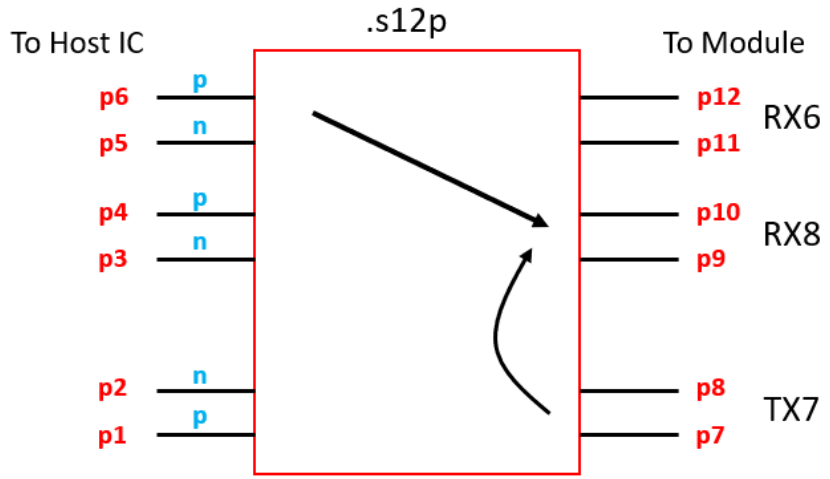
- The loss of the C2M channel (TP0-TP1A) budge is determined/bounded by the bump-to-bump, ref PKG, and DAC loss budget, which are trending <=40 dB, ~6 dB , ~16 dB, for 212.5 Gbps-PAM4 signaling.

Background and Introduction (II)

- We leveraged our established/validated C2M channel design tool-flow-methodology (TFM) (e.g., oif2022.355.00, oif2022.498.00, oif2023.032.00) to create this C2M channel design A to support 212.5 Gbps-PAM4 “Universal Port”.

C2M Channel Design A for “Universal Port”

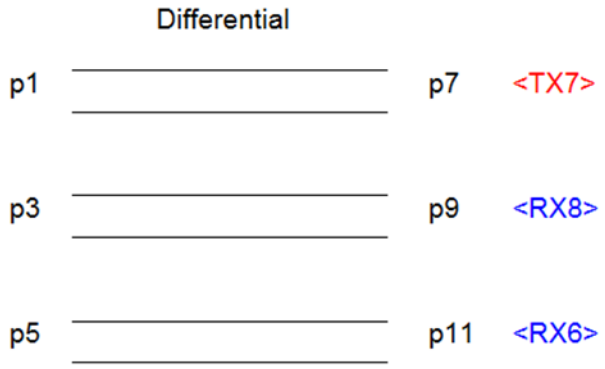


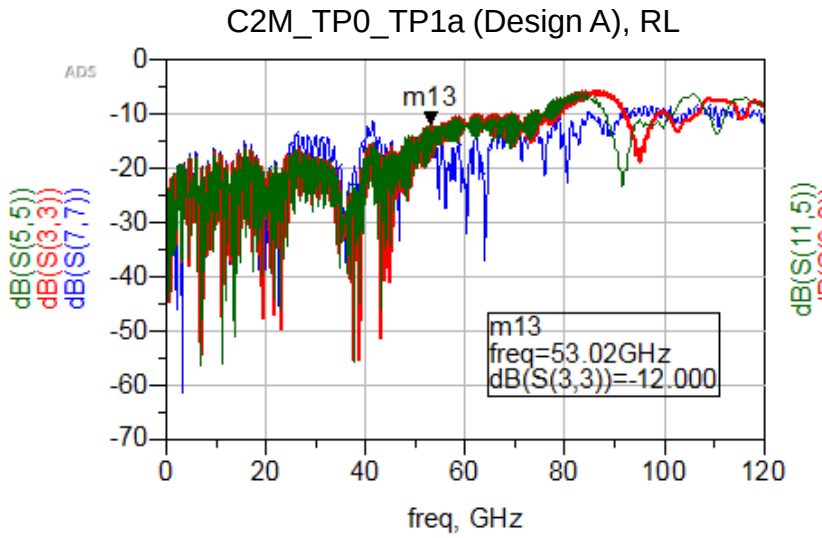


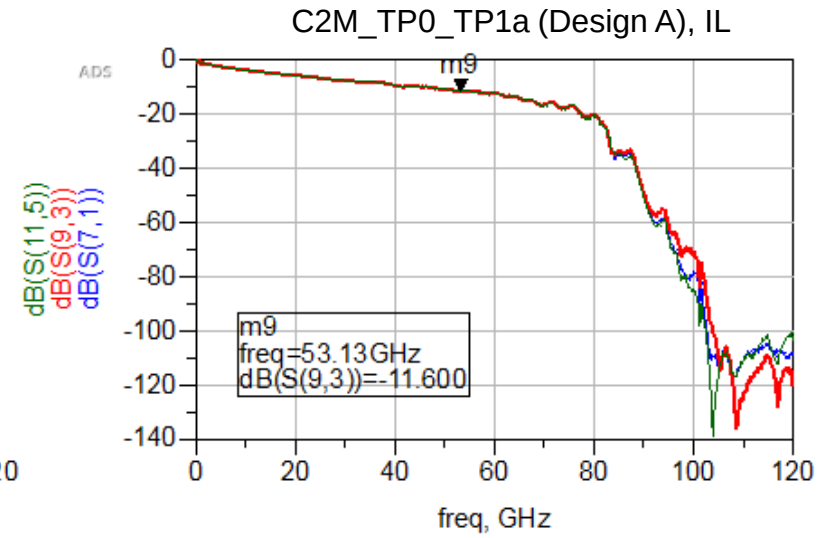
Component	Insertion Loss TP0-TP1a (dB) @ 53.125GHz
	Design A
Host PCB via	0.75 dB
Host PCB Trace	4.5 inch (1.27 dB/inch)
Connector	1.46 dB
HCB	3.42 dB
Total *	11.6 dB

* Not lineally added

C2M Channel Design A Characteristics (I)

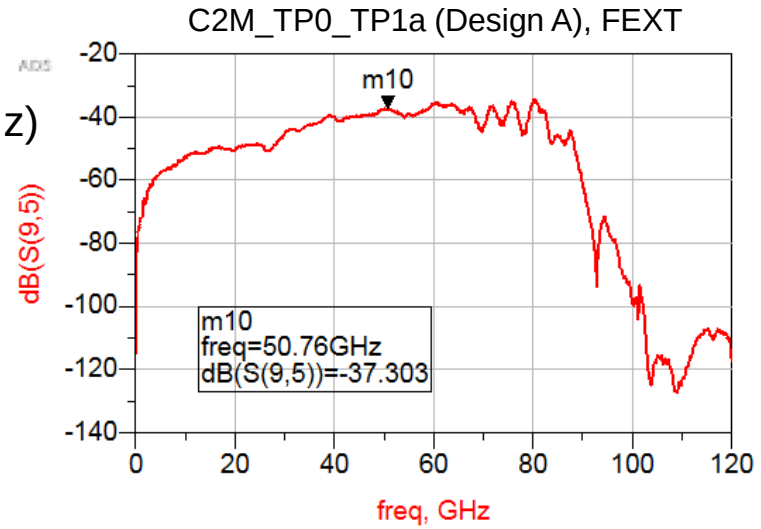


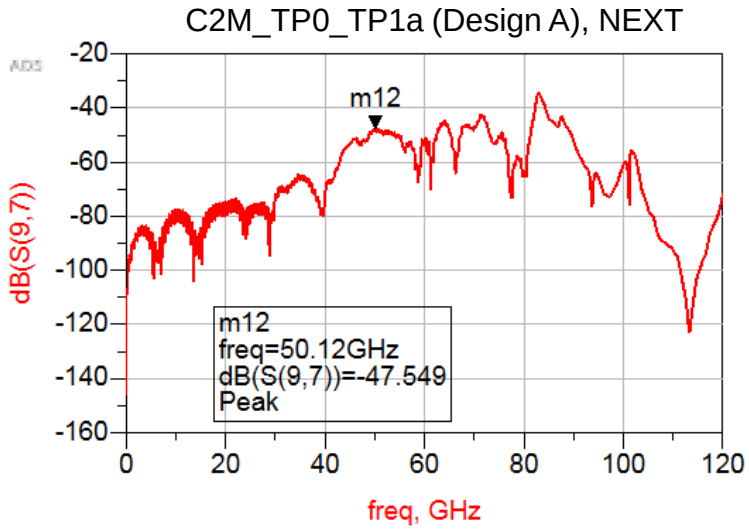




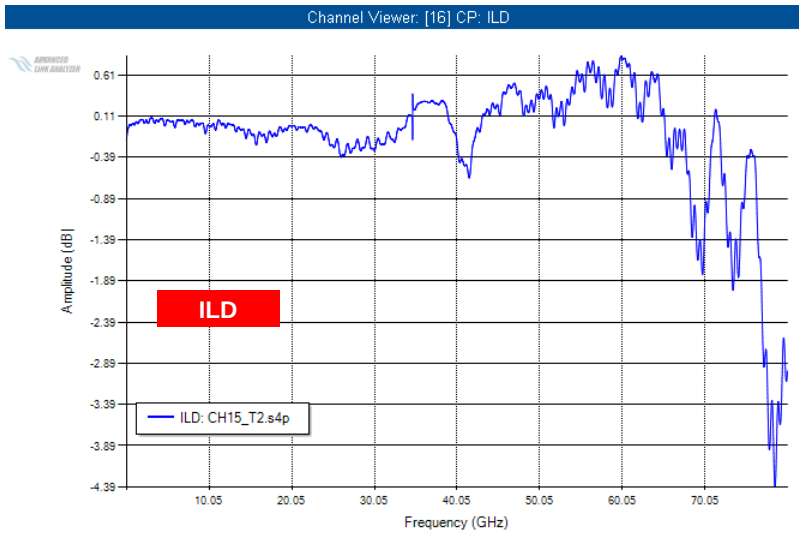
TP0-TP1a Characteristics (DC-53.125GHz)

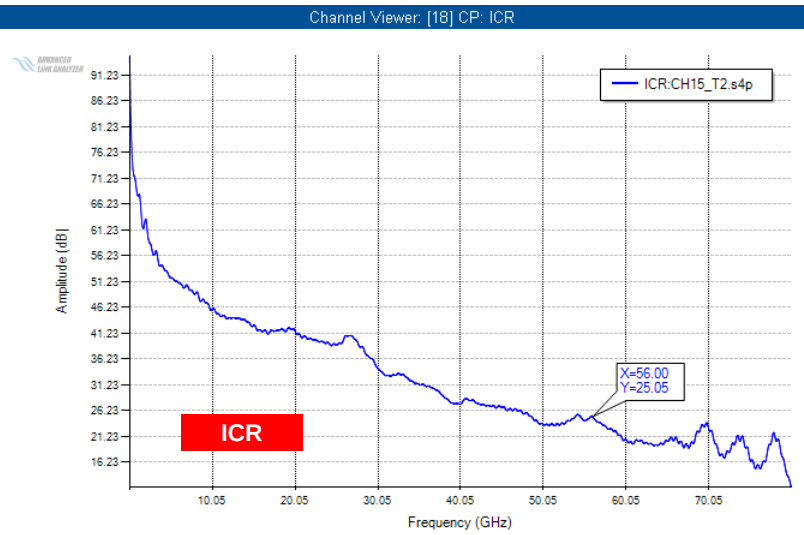
- **IL: 11.6dB @ 53.125GHz**
- RL ~= 12.0dB (<53.125GHz)
- FEXT < 37.3dB (<53.125GHz)
- NEXT < 47.5dB (<53.125GHz)

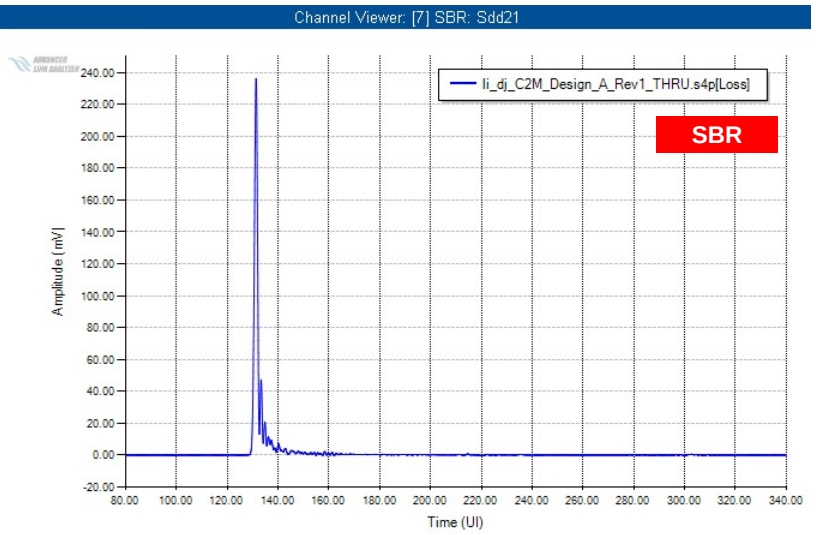




C2M Channel Design A Characteristics (II)

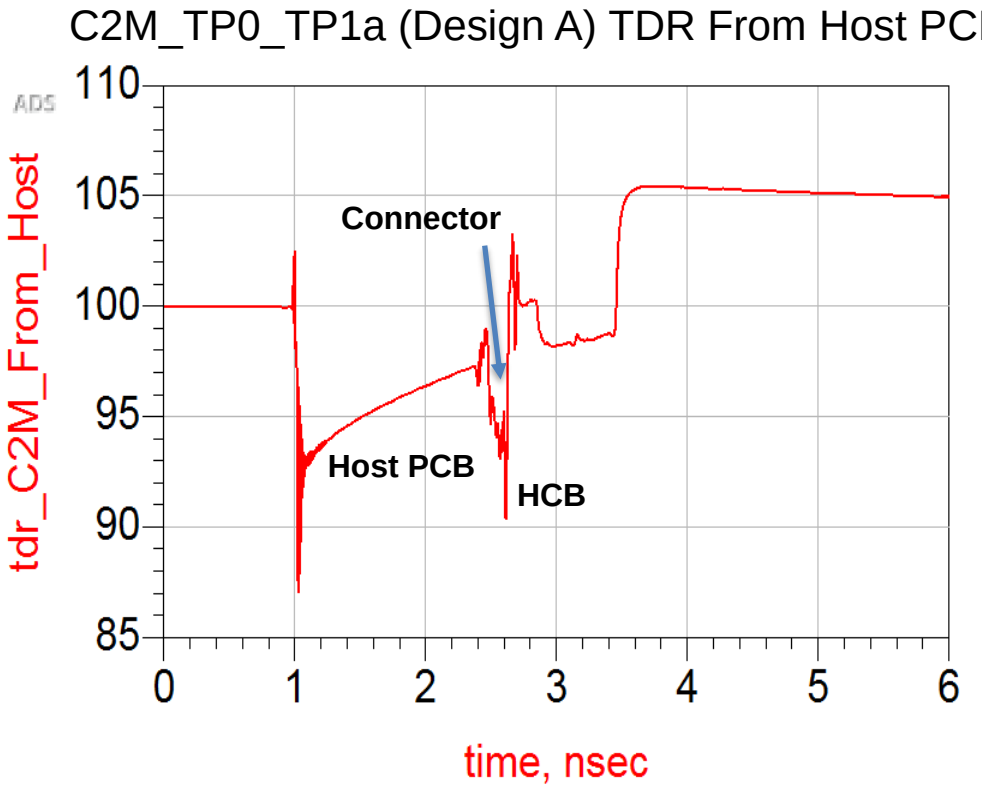


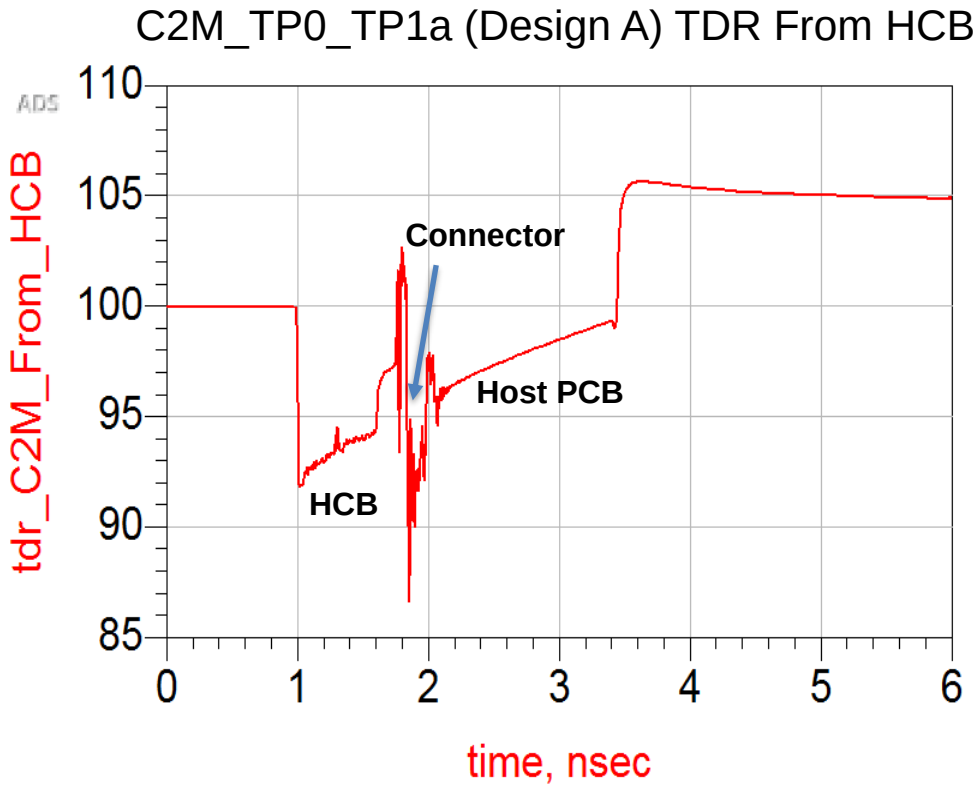




- **ILD < +- 1 dB (<53.125 GHz)**
- **ICR > 25 dB (<53.125 GHz)**

C2M Channel Design A Characteristics (III)





[S] parameter BW DC-120GHz

Summary

- We have created a C2M channel Design A supporting “Universal Port” at 212.5 Gbps-PAM4
- This C2M channel includes PCB-Via, PCB, connector, and HCB
- This C2M channel has:
  - An IL (TP0-TP1A) of ~11.6 dB at 53.125 GHz
  - RL <~ 12.0dB at <= 53.125 GHz
  - FEXT < 37.3dB, NEXT < 47.5dB, at <= 53.125 GHz
  - PCB IL of 5.7 dB/reach of 4.5 inch (with 1.27 dB/inch) at 53.125 GHz