Exploring Receiver Tradeoffs: 100Mbps and 3Gbps Implementations

Contribution to 802.3dm Task Force

January 21, 2024

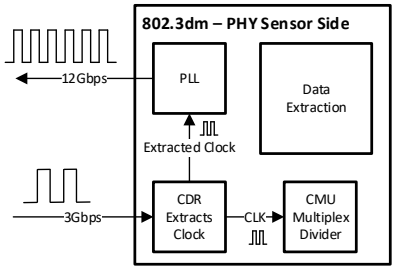
TJ Houck (Marvell)

Topics

- Why does TDD require 3Gbps to transfer only 100Mbps of data?
- Asymmetric Channel Efficiency from TDD
- Receiver Complexity 3Gbps TDD vs 100Mbps ACT

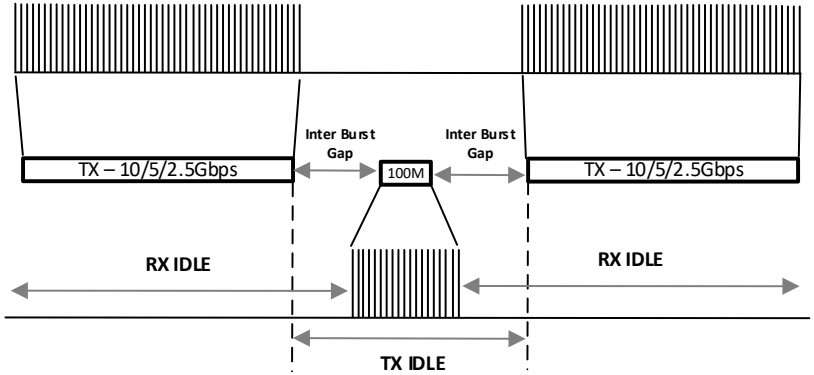
Why does TDD require 3Gbps to transfer only 100Mbps of data?

TDD – Time Division Duplex

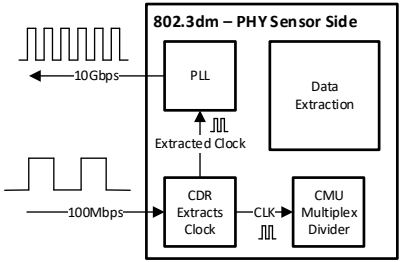


Line rate 12Gbps – 10Gbps Data Rate
Line rate 6Gbps – 5Gbps Data Rate
Line rate 3Gbps – 2.5Gbps Data Rate

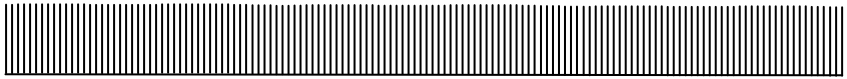
Line rate 3Gbps – 100Mbps Data Rate



ACT – (Asymmetric Concurrent Transmission) – GMSL and FPD-Link



Line rate 11.25Gbps – 10Gbps Data Rate
Line rate 5.6Gbps – 5Gbps Data Rate
Line rate 2.8Gbps – 2.5Gbps Data Rate



Line rate 117.1875Gbps – 100Mbps Data Rate
Manchester encoded to 234Mbps

Referenced: https://www.ieee802.org/3/dm/public/1124/Dalmia_Goel_3dm_01a_11112024.pdf

Asymmetric Channel Efficiency of TDD

- Inter Burst Gap (IBG)
  - Additional Delay to avoid interference
- Resync Headers
  - Happens every TX and RX cycle
- Overhead
  - Larger overhead due to Resync and IBG
- Actual Data throughput – 3.3%
  - Efficient use of the Receiver
- Packet size reduction
  - Can not support higher packet transfer

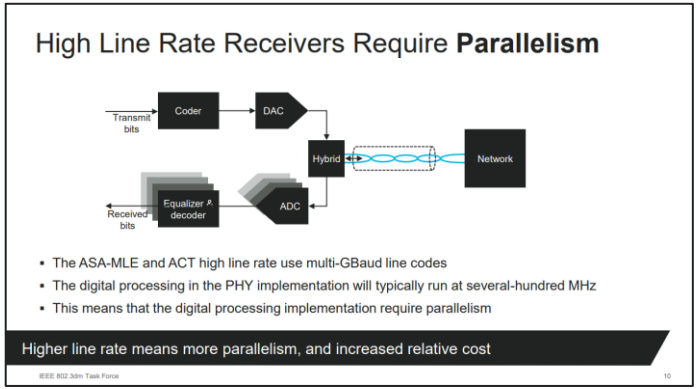
TDD – Time Division Duplex – 3Gbps Receive

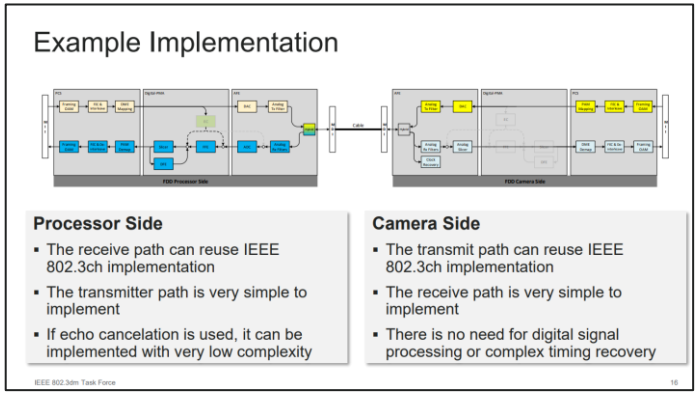
	3.0Gbps - TDD	100Mbps - (ACT)	GMSL2 - 187Mbps - (FDD)
Synchronization	Repeated synchronization headers in each RX phase	Once During 1st boot	Once During 1st boot
Resync Header	Overheaded happens every frame TX/RX	None	None
Idle Burst Gap	104nsec	None - not needed	None - not needed
Overhead Impact	>90% - 36%	~17%	~17%
Data Bandwidth	100Mbps	100Mbps	~155Mbps
Throughput	3.30%	85.47%	83%
Packet sizes	116bytes Requires buffer to meet 802.3 compliance 1500byte packet	64 - 1500 bytes bulk mode possible	Not Ethernet

Receiver Complexity 3Gbps TDD vs 100Mbps ACT

	3.0Gbps - TDD	100Mbps - (ACT)	GMSL2 - 187Mbps - (FDD)
AFE (Analog Front-End)	CTLE, LNA, PGA for 3Gbps	LNA and LPF for 234Mbps bandwidth	LNA and LPF for 187Mbps bandwidth
CDR (Clock Data Recovery)	~(3:1)	Simple ~(1:1)	Baseline
Equalization	1-3 tap DFE	None	None
Manchester Encoding	N/A	Very small	N/A
Deserializers	10:1 or higher	Basic	Basic
Estimated power Disppation	Higher than (4:1)	Similar to GMSL ~(1:1)	Baseline
Die Size	Higher than (4.5:1)	Similar to GMSL ~(1:1)	Baseline
Process node	More Aggressive	Less aggressive	older node

Numbers for 3Gbps - TDD are conversative – Automotive robustness will most likely increase complexity of circuitry and size





Referenced: https://ieee802.org/3/dm/public/0924/jonsson_razavi_3dm_01_09_15_24.pdf
Referenced: https://ieee802.org/3/dm/public/0924/jonsson_3dm_01_09_15_24.pdf

Summary

1. It is proposed to **minimize the 100Mbps receiver** to be competitive in the existing market space

2. It is proposed to **have efficient bandwidth** from Low speed and High-speed receiver

Essential technology, done right™