Exploring Receiver Tradeoffs: 100Mbps and 3Gbps Implementations

Contribution to 802.3dm Task Force

January 22, 2024

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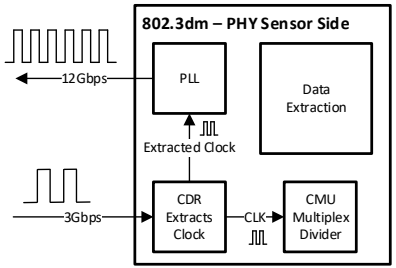
Topics

- Why does TDD require 3Gbps to transfer only 100Mbps of data?
- Asymmetric Channel Efficiency from TDD
- Receiver Complexity 3Gbps TDD vs 100Mbps ACT

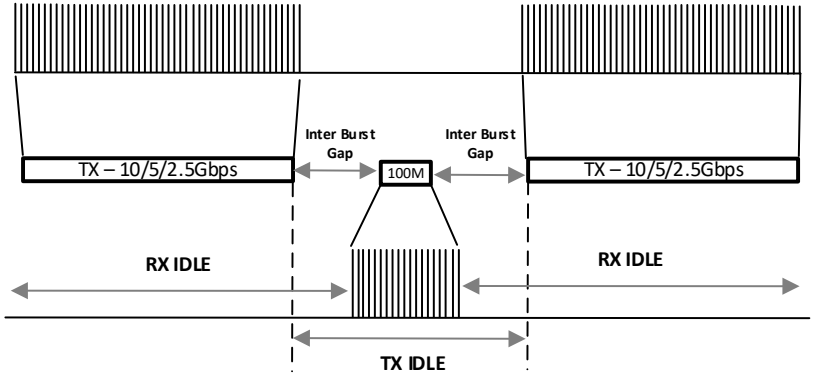
Why does TDD require 3Gbps to transfer only 100Mbps of data?

TDD – Time Division Duplex

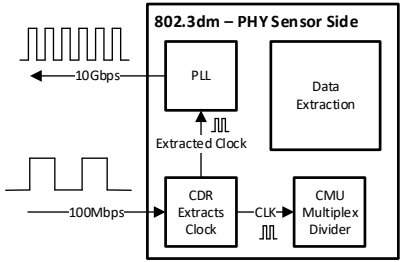


Line rate 12Gbps – 10Gbps Data Rate
Line rate 6Gbps – 5Gbps Data Rate
Line rate 3Gbps – 2.5Gbps Data Rate

Line rate 3Gbps – 100Mbps Data Rate



ACT – (Asymmetric Concurrent Transmission) – GMSL and FPD-Link (FDD)



Line rate 11.25Gbps – 10Gbps Data Rate
Line rate 5.6Gbps – 5Gbps Data Rate
Line rate 2.8Gbps – 2.5Gbps Data Rate

Line rate 117.1875Mbps – 100Mbps Data Rate
Manchester encoded to 234Mbps

Referenced: https://www.ieee802.org/3/dm/public/1124/Dalmia_Goel_3dm_01a_11112024.pdf

Asymmetric Channel Efficiency of TDD

- Inter Burst Gap (IBG)
  - Additional delay to avoid interference
- Resync Headers
  - Happens every TX and RX cycle
- Overhead
  - Larger overhead due to Resync and IBG
- Actual Data throughput – 3.3%
  - Inefficient use of the Receiver
- Requires Buffer from lack of throughput
  - Can not support 1500byte packet transfer

TDD – Time Division Duplex – 3Gbps Receive

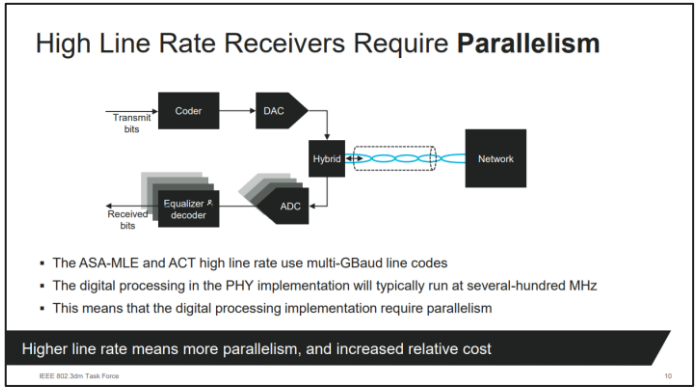
	3.0Gbps - TDD	100Mbps - (ACT)	GMSL2 - 187Mbps - (FDD)
Synchronization	Repeated synchronization headers in each RX phase	Once During 1st boot	Once During 1st boot
Resync Header	Overheaded happens every frame TX/RX	None	None
Idle Burst Gap	104nsec	None - not needed	None - not needed
Overhead Impact	>90% - Full Link time 36% - 100Mbps	~17%	~17%
Data Bandwidth	100Mbps	100Mbps	~155Mbps
Throughput	3.3% for 3Gbps	85.47% for 117Mbps	83% for 187Mbps
Packet sizes	116bytes Requires buffer to meet 802.3 compliance 1500byte packet	64 - 1500 bytes	Not Ethernet

Receiver Complexity 3Gbps TDD vs 100Mbps ACT

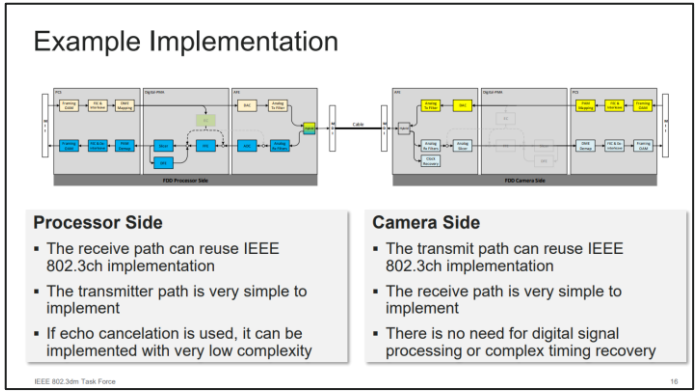
	3.0Gbps - TDD	100Mbps - (ACT)	GMSL2 - 187Mbps - (FDD)
AFE (Analog Front-End)	CTLE, LNA, PGA for 3Gbps	LNA and LPF for 234Mbps bandwidth	LNA and LPF for 187Mbps bandwidth
CDR (Clock Data Recovery)	x3	x1	Baseline
Equalization	1-3 tap DFE	None	None
Deserializers	High Speed required	Basic	Basic
Estimated power Disspation	Higher than x4	x1	Baseline
Die Size	Higher than x4.5	x1	
Process nodes	Lower Geometry	Any node	older node
Imager Integration	Difficult - Will require Lower Node	Easier to match node	possible - more difficult

Numbers for 3Gbps - TDD are conversative – Automotive robustness will most likely increase complexity of circuitry and size

TDD – High Level Block Diagram



ACT – Example Block Diagram



Referenced: https://ieee802.org/3/dm/public/0924/jonsson_razavi_3dm_01_09_15_24.pdf
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Summary

1. It is proposed to **minimize the 100Mbps receiver** to be competitive in the existing market space

2. It is proposed to **have efficient bandwidth** from Low speed and High-speed receiver

Contributors

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