Upstream Receiver

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The Reason for 802.3dm Task Force

- For asymmetrical operation on camera side, a PHY that has
  - Lower Cost
  - Lower Power

Camera Link Problem Statement

- Key characteristics:
  1. Efficiently support highly asymmetric data rates:
     - 1Gbps to 10Gbps or more from camera
     - Never more than 100Mbps towards camera
  2. Power constrains solution in camera module, to control temperature in the module
  3. Power delivery over the data link
  4. Very cost sensitive – needs an optimized solution

- Seamless integration with the overall automotive Ethernet network

https://www.ieee802.org/3/cfi/0723_1/CFI_01_0723.pdf

Broad Market Potential

Each proposed IEEE 802 LMSC standard shall have broad market potential. At a minimum, address the following areas:
a) Broad sets of applicability.
b) Multiple vendors and numerous users.

- Broad Sets of Applicability:
  - Migration of cameras, displays, and other imaging sensors to an automotive ethernet network present an inherently asymmetric data stream with gigabit rates in one direction and a typically low-rate control plane in the other direction.
  - These applications are highly cost and power sensitive and benefit from optimization, requiring a targeted solution
  - Market-adjacent sensor applications such as in-building sensors and other automotive sensors will benefit from the standardization of protocols for interfacing natively asymmetric physical layers, as many sensors are asymmetric and similarly constrained as automotive cameras.
- Multiple vendors and numerous users:
  - At the call for interest, 70 individuals from 49 affiliations indicated they would support this project. These included automotive OEMs, automotive Tier 1, networking OEMs, silicon, infrastructure, cabling, connector, and test equipment experts.
  - Data presented at the CFI indicate a substantial automotive camera market potential, exceeding 1 billion ports and adjacent automotive markets approaching 500 million ports in 2030.

Version 2.7 IEEE 802.3 Ethernet Working Group - CSD Page 4

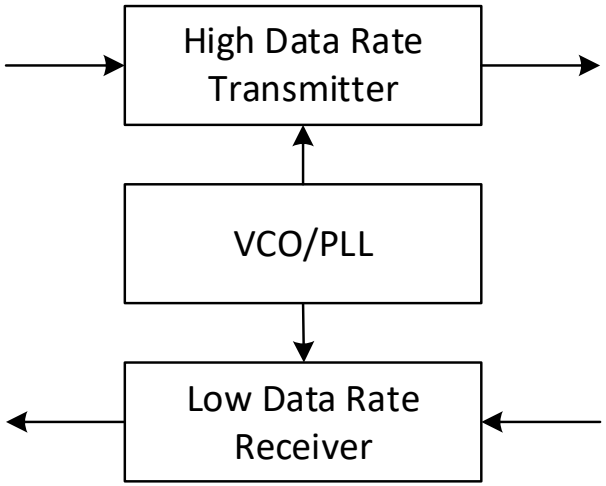
https://mentor.ieee.org/802-ec/dcn/24/ec-24-0074-00-ACSD-p802-3dm.pdf

Technical Feasibility

- ACT, TDD, and 802.3ch EEE all technically feasible over STP and Coax
- ACT
  - https://www.ieee802.org/3/dm/public/0724/sedarat_3dm_202407.pdf
  - https://www.ieee802.org/3/dm/public/0924/jonsson_razavi_3dm_01_09_15_24.pdf
- EEE
  - https://www.ieee802.org/3/dm/public/0524/Evaluation%20of%20802.3ch_Tran_050142024a.pdf
- TDD
  - No direct presentation on current proposed modulation scheme, but assumption is if it works for the EEE solution the same solution with echo cancellation removed may work as TDD.

Assumptions

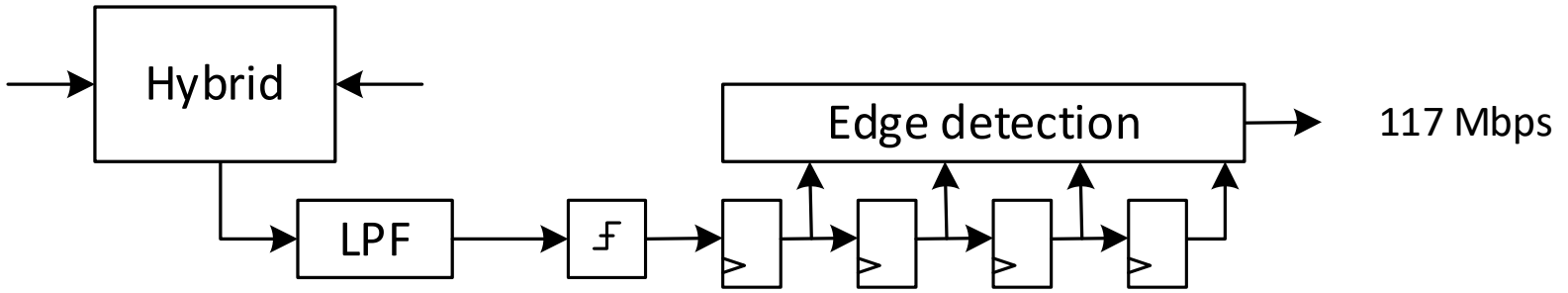
- Assume high data rate transmitters, VCO/PLL comparable between ACT and TDD on power and area
- ACT - 5.625 Gbaud PAM4, 100% duty cycle
- TDD – 6.0 or 6.25 Gbaud PAM4, 92% duty cycle
  - https://www.ieee802.org/3/dm/public/1124/Chini_3dm_01a_1124.pdf proposals 1 and 2.



- This presentation examines low data rate receive path power and area

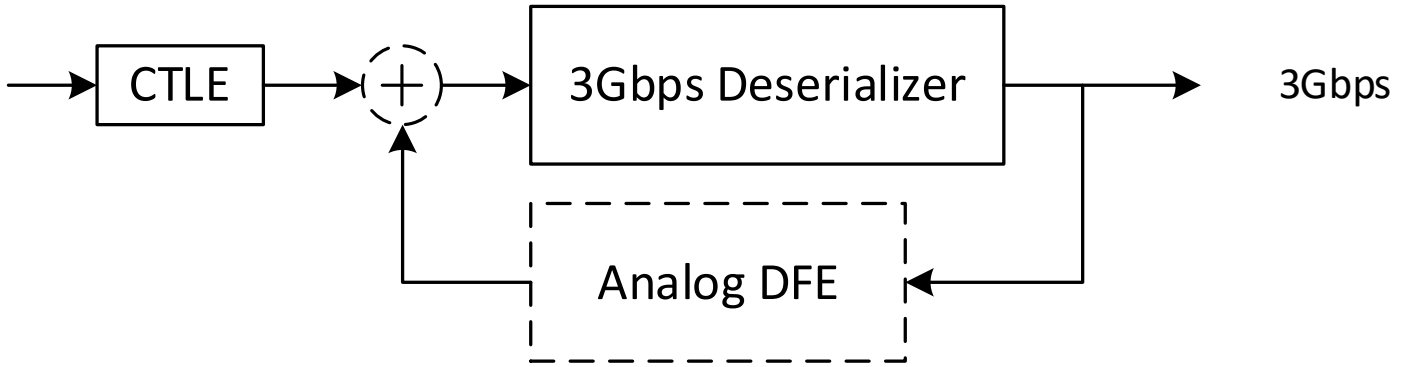
ACT Receiver Architecture

- Lightweight Hybrid
  - Cancel only at lower frequencies
- LPF – Simple passive low pass filter
- Slicer is a 1-bit low speed comparator
- Possible data recovery techniques
  - Oversample data – no tracking clock
  - Track sampling clock and baud rate sampling



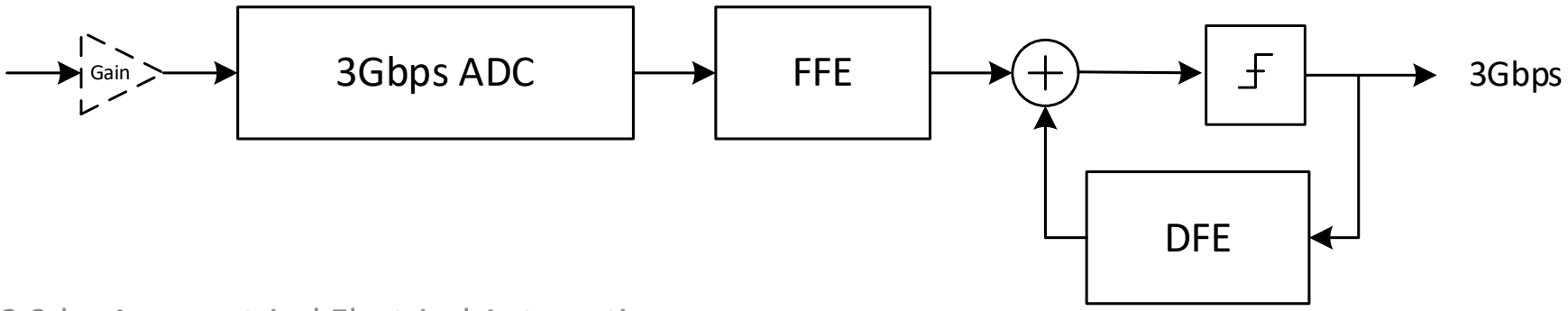
TDD Analog SERDES Receiver Architecture

- CTLE – Passive high pass filter or can be active filter
  - Is CTLE flexible enough to handle impairments? i.e. secondary reflections
- 3Gbps De-serializer
  - Clock and data recovery circuit
- Analog DFE – (probably needed)



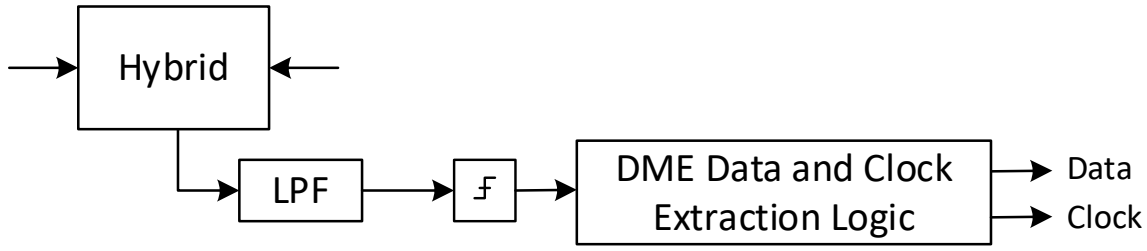
TDD ADC Receiver Architecture

- Gain – Active gain up to maximize ADC dynamic range (if needed)
  - Can also include some high pass filtering
- 3Gbps ADC – includes clock recovery (not shown)
  - Clock and data recovery circuit
- FFE and DFE



ACT Receiver Implementation and Test Conditions

- 16nm process with actual circuit layout
- Low pass filter with 250MHz cutoff
- Light hybrid cancelling between 10-250MHz
  - No cancelling needed at higher frequencies (lower power)
- Digital data and clock extraction logic
- No echo canceller needed
- 2dBm fast transmitter power
- -2dBm slow transmitter power
- 15 meter cable on STP
- 10GBASE-T1 downstream PAM4



Spice simulation on receiver

- -2dBm Transmit DME
- 2dBm 10GBASE-T1 Tx
- 15 meter cable STP

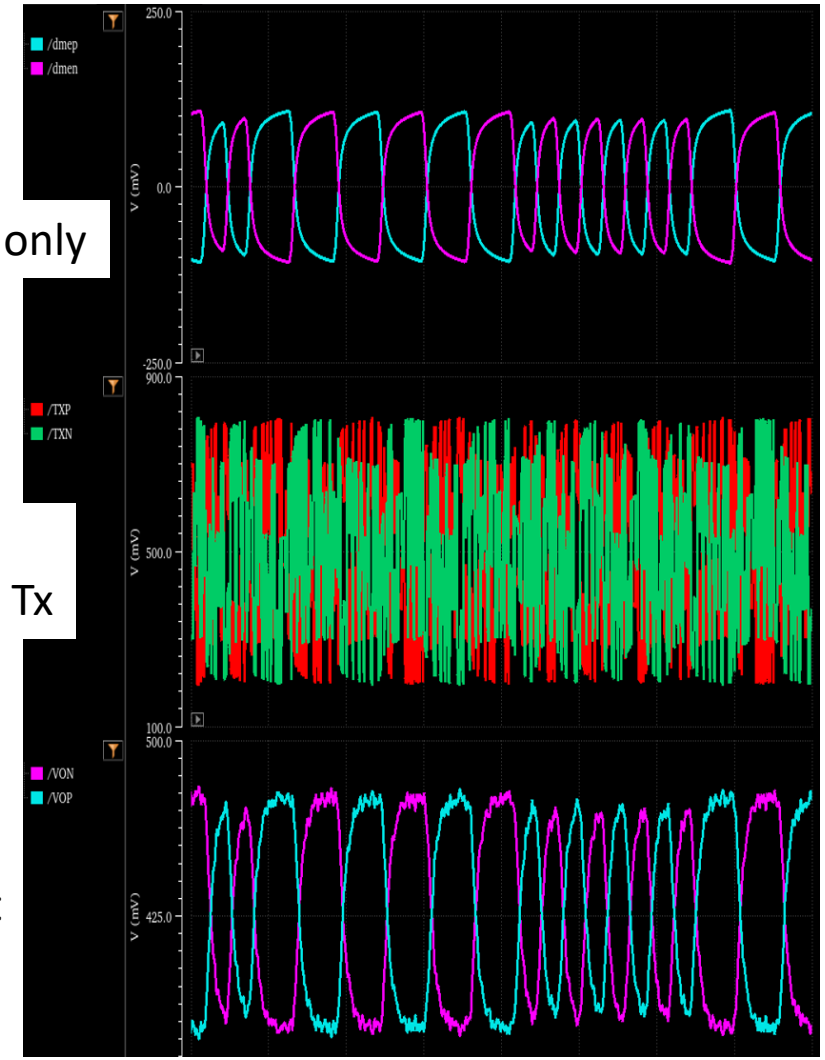
DME signal only

MDI @ Rx
DME + Fast Tx

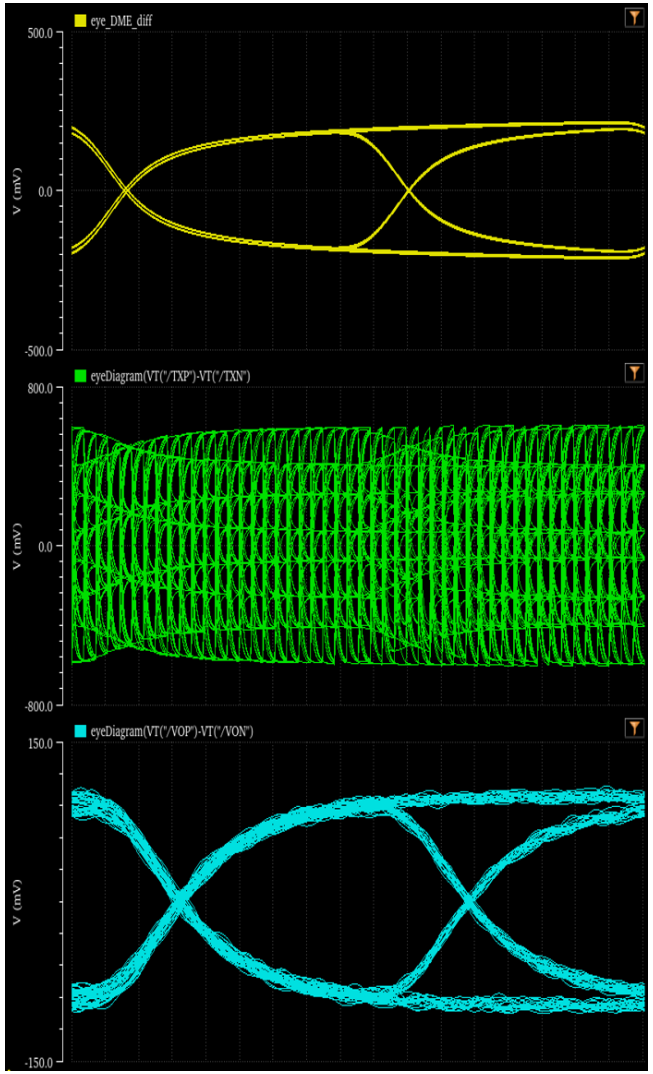
- Eye open

Slicer Input

Time Domain



Eye Diagram



No Echo Canceller Needed

- Add 10GBASE-T1 Echo 6dB above worst case

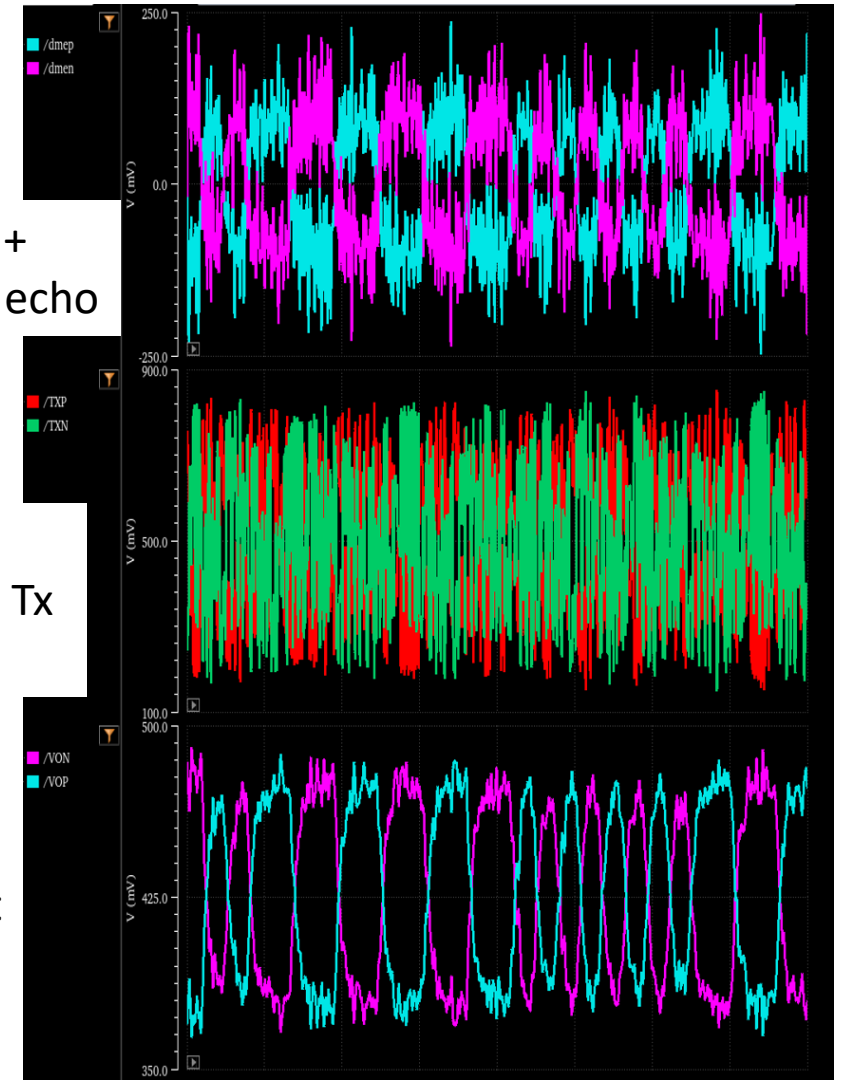
Time Domain

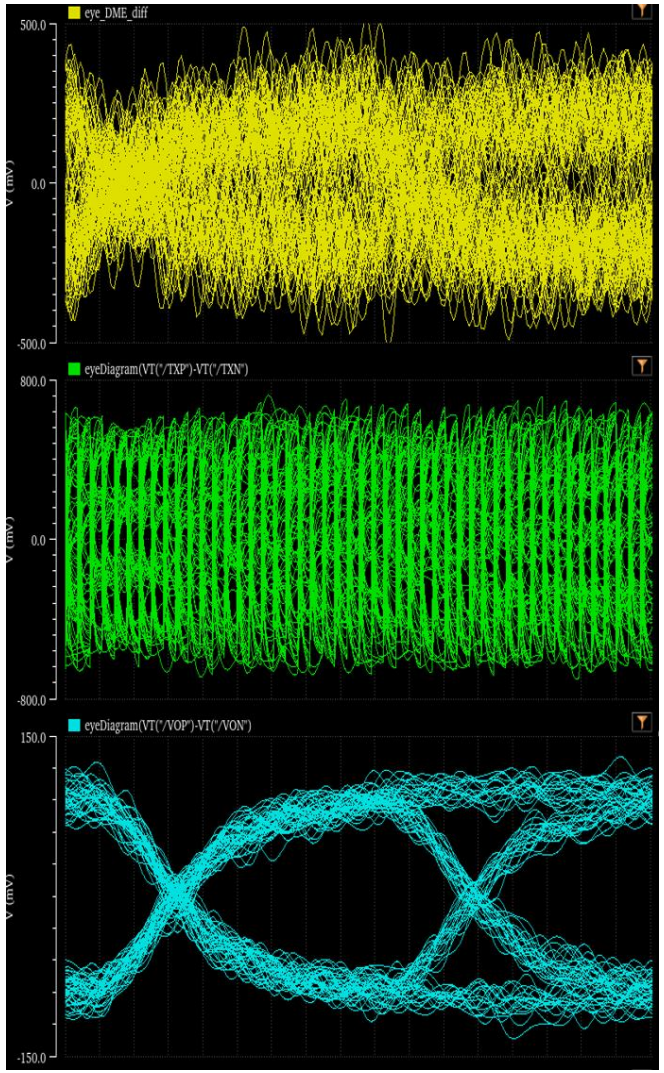
Eye Diagram

DME signal + High speed echo

MDI @ Rx DME + Fast Tx + Echo

Slicer Input





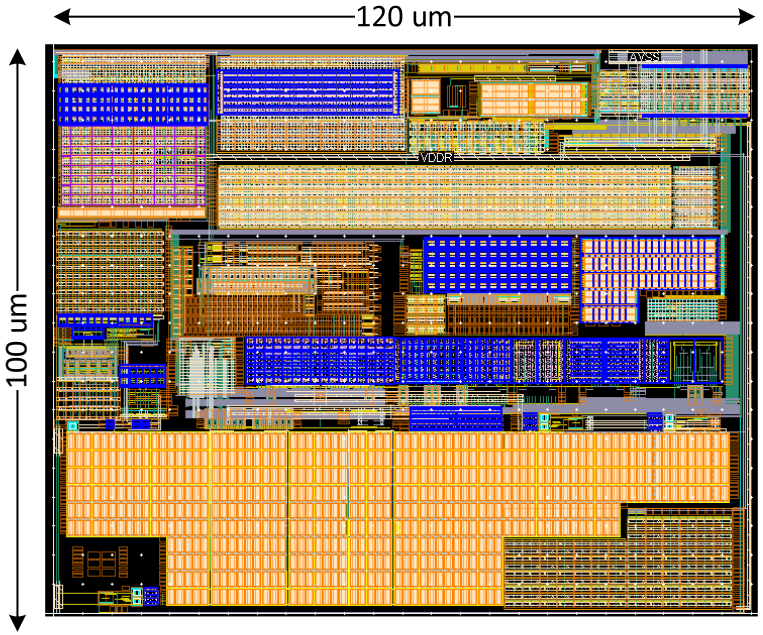
- Eye open without echo canceller

ACT Receiver Power and Area

- < 3 mW for receiver path

- Trial layout (unoptimized)

  120um x 100um = 0.012 mm^2



(diameter of human hair is around 100um)

Summary

- Goal for 802.3dm is for low power and low cost
- ACT camera side receiver does not require echo cancellation
- ACT camera side receiver has plenty of margin
- ACT camera side receiver has very low power and very small area

THANK YOU