ACT text proposal for IEEE 802.3dm

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2xx Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100M+2.5GMBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GMBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1

This is a draft proposal for how a Clause could be structured based on the P802.3dm project documents, including Objectives. This provides flexibility to have different requirements for the different speeds and cabling. Subclauses can be combined later if the requirements are the same, or the requirement can be put in the first subclause in the document and the one later in the document can refer back to it.

Due to the fact that we are limited to a maximum of five levels in the specification, the high speed and low speed requirements are in separate subclauses without a subsection above the pair. This is also the case for the coax and shielded balanced copper cabling.

2xx.1 Overview

May be added by Editor based on project details.

2xx.1.1 Nomenclature

May be added by Editor based on project details.

In order to efficiently describe the three PHYs, the nomenclature MultiG is used to abbreviate 2.5G/ 5G/10G when referring to the set of PHYs.

2xx.1.2 PHY/PMD types

I have included a table here to show the different PHYs to be defined and what all the characters that I am using in the names mean. These are subject to approval.

x+y – x is the transmit speed, y is the receive speed

T1 – single shielded balanced pair of conductors (SBP)

V1 – single coaxial cable (Coax)

PHY name	*Transmit speed*	*Receive speed*	Cable type
100M+2.5GMBASE-T1	*100M*	*2.5G*	*SBP*
2.5G+100MBASE-T1	*2.5G*	*100M*	*SBP*
100M+5GBASE-T1	*100M*	*5G*	*SBP*
5G+100MBASE-T1	*5G*	*100M*	*SBP*
100M+10GBASE-T1	*100M*	*10G*	*SBP*
10G+100MBASE-T1	*10G*	*100M*	*SBP*
100M+2.5GBASE-V1	*100M*	*2.5G*	*Coax*
2.5G+100MBASE-V1	*2.5G*	*100M*	*Coax*
100M+5GMBASE-V1	*100M*	*5G*	*Coax*
5G+100MBASE-V1	*5G*	*100M*	*Coax*
100M+10GBASE-V1	*100M*	*10G*	*Coax*
10G+100MBASE-V1	*10G*	*100M*	*Coax*

When talking about all high speed transmit PHYs, regardless of cable type, use:

MultiG+100MBASE-T1/V1.

When talking about all low speed transmit PHYs, regardless of cable type, use:

100M+MultiGBASE-T1/V1.

When talking about all PHYs communicating on shielded, balanced, pair of conductors, regardless of transmit speed, use:

MultiG+100M/100M+MultiGBASE-T1

When talking about all PHYs communicating on coaxial cable, regardless of transmit speed, use:

MultiG+100M/100M+MultiGBASE-V1

When talking about all PHYs, regardless of transmit speed or cable type, use:

MultiG+100M/100M+MultiGBASE-T1/V1

2xx.1.3 Relationship of MultiG+100M/100M+MultiGBASE-T1/V1 to other standards

May be added by Editor based on project details.

2xx.1.4 Operation of MultiG+100M/100M+MultiGBASE-T1/V1

Summary provided by contribution later in project

2xx.1.4.1 Physical Coding Sublayer (PCS), MultiG+100MBASE-T1/V1

For the high data rate direction, the MultiG+100MBASE-T1/V1 PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in 46, to the 2.5G+100MBASE-T1/V1, 5G+100MBASE-T1/V1, or 10G+100MBASE-T1/V1 Physical Medium Attachment (PMA) sublayer. In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the high data rate direction, the PCS functions as specified in 149.

2xx.1.4.2 Physical Coding Sublayer (PCS), 100M+MultiGBASE-T1/V1

In the **low data rate** direction, in normal mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block.

These 65-bit blocks are then aggregated into groups of 4 blocks. The contents of each group are contained in a vector tx_group4x65B. Next, a 16-bit OAM/Reserved field is appended to form a 276-bit block. Each of these 276 bit blocks is formed into an RS-FEC input frame, then encoded by the RS-FEC (50,46,6). The RS-FEC output superframe consists of 300 bits. The duration of the frame is 2560 ns. Finally, these bits are exclusive OR'd with a 33-bit self-synchronizing scrambler to create the 100M+MultiGBASE-T1/V1 payload. The low data rate direction PCS transmit functions are described in 2XX.3.2.2.

The tx_group4x65B <259:0> is defined as:

$$tx\_group4x65B\langle 65 \times i + j \rangle = tx\_coded_i\langle j \rangle$$

where i = 0 to 3 , j = 0 to 64, and tx_coded_i<64:0> is the i-th 64B/65B block where tx_coded0<64:0> is the first block transmitted.

In the training mode (see 2XX.4.2.4), the PCS transmits and receives DME training frames to synchronize to the PHY frame (and exchanges EEE and 100M+MultiGBASE-T1/V1 OAM capabilities).

Details of the PCS functions and state diagrams are covered in 2XX.3. The interface to the PMA is an abstract message-passing interface specified in 2XX.4.

2xx.1.4.3 Physical Medium Attachment (PMA) sublayer, MultiG+100MBASE-T1/V1

The PMA couples messages from the PCS service interface onto single balanced pair of conductors (T1) or single coaxial cables (V1) via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions.

The PMA provides asymmetric data rate communications with 5625 x S MBd high speed and 117.1875 MBd low speed. See Table 2XX–1 for the definition of S. The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled following the completion of Auto-Negotiation or PHY Link Synchronization and provides the startup functions required for successful

MultiG/100M-BASE-T1 operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link channel and communicates this status to other functional blocks. A failure of the receive channel causes the data mode operation to stop and Auto-Negotiation or Link Synchronization to restart.

PMA functions and state diagrams are specified in 2xx.6 and 2xx.7. The electrical parameters of the PMA, i.e., test modes and electrical specifications for the transmitter and receiver, are specified in 2xx.8 and 2xx.9.

The PMA functions for the high data rate direction are as specified in 149.4 with the exceptions in this clause.

2xx.1.4.4 Physical Medium Attachment (PMA) sublayer -L

NOTE: It is probably sufficient to have single section for low speed *and* high speed *for this section.*

2xx.1.4.5 EEE Capability

May want to include and indicate there is no EEE Capability if it is decided this is not needed/required/desired.

2xx.1.4.6 Link Synchronization

The Link Synchronization function is used when Auto-Negotiation is disabled or not implemented to detect the presence of the link partner, time and control link failure, and act as the data source for the PHY control state diagram. Link Synchronization operates in a half-duplex fashion. Link Synchronization is defined in <REF>.

2xx.1.4.7 Link Synchronization

NOTE: This section is probably redundant since there should be single section for low speed *and* high speed.

2xx.1.5 Signaling, MultiG+100MBASE-T1/V1

MultiG+100MBASE-T1/V1 signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over single balanced pair of conductors (T1) or single coaxial cable (V1). The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM4 symbols in the high speed transmit path.
c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions.
f) Block framing and other control signals.
g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
h) Ability to automatically detect and correct for incorrect polarity in the connection.
i) Optionally, ability to support refresh, quiet, and alert signaling during LPI operation.

The PHY may operate in three basic modes: the normal data mode, the training mode, or an optional LPI mode.

In high speed direction, the PCS operates according to Clause 149.

2xx.1.6 Signaling, 100M+MultiGBASE-T1/V1

100M+MultiGBASE-T1/V1 signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over single balanced pair of conductors (T1) or single coaxial cable (V1). The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to DME symbols in the high speed transmit path.
c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions.
f) Block framing and other control signals.
g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
h) Ability to automatically detect and correct for incorrect polarity in the connection.
i) Optionally, ability to support refresh, quiet, and alert signaling during LPI operation.

The PHY may operate in two basic modes: the normal data mode or the training mode.

In low speed direction and normal mode, the PCS generates a continuous stream of DME symbols that are transmitted via the PMA. In training mode, the PCS is directed to generate only TBD_training symbols for transmission by the PMA. (See Figure <REF>)

2xx.1.7 Interfaces

All MultiG+100M/100M+MultiGBASE-T1/V1 PHY implementations are compatible at the MDI and at the XGMII, if implemented. Implementation of the XGMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not. The MDI for single balanced pair of conductors (T1) or single coaxial cable (V1), are different.

2xx.1.8 Conventions in this clause

Standard text

2xx.2 MULTIG+100MBASE-T1/V1 service primitives and interfaces

Service primitives and interfaces the high speed direction are as described in Clause 149.2.

2xx.3 100M+MultiGBASE-T1/V1 service primitives and interfaces, low speed channel

100M+MultiGBASE-T1/V1 transfers data and control information across the following four service interfaces:

a) 10 Gigabit Media Independent Interface (XGMII)

b) Technology Dependent Interface

c) PMA service interface

d) Medium Dependent Interface (MDI)

The XGMII is specified in Clause 46; the Technology Dependent Interface is specified in 98.4. The PMA service interface is defined in <REF> and the MDI is defined in <REF>.

2xx.3.1 Technology Dependent Interface

This section is only needed if Auto-Negotiation is supported

2xx.3.1.1 PMA_LINK.request

2xx.3.1.2 PMA_LINK.indication

2xx.3.2 PMA service interface

MultiG/100MBASE-T1/V1-L service interface is as specified in 149.2.2, with the exceptions given in this subclause.

2xx.3.2.1 PMA_TXMODE.indication

The transmitter in a MultiG/100MBASE-T1/V1-L link normally sends over the MDI symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

~~*NOTE: Update figure 149-3 with MII instead of XGMII.*~~

2xx.3.2.2 PMA_CONFIG.indication

As specified for MultiGBASE-T1 PHYs in 149.2.2.2.

2xx.3.2.3 PMA_UNITDATA.request

PMA_UNITDATA.request(tx_symb)

During low data rate transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb the value of the symbols to be sent over the MDI. The tx_symb may take on one of the following values:

- The DME in normal operation.
- 0 when zeros are to be transmitted in the following two cases:

when PMA_TXMODE.indication is SEND_Z during PMA training, and

after data mode is reached, the transmit function is in the LPI transmit mode, and lpi_tx_mode is QUIET.

2xx.3.2.4 PMA_UNITDATA.indication

The low data rate PMA generates PMA_UNITDATA.indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the low data rate PMA_UNITDATA.indication primitive is S_up x 11250 MHz; as governed by the recovered clock.

2xx.3.2.5 PMA_SCRSTATUS.request

As specified for MultiGBASE-T1 PHYs in 149.2.2.5.

2xx.3.2.6 PMA_PCSSTATUS.request

As specified for MultiGBASE-T1 PHYs in 149.2.2.6.

2xx.3.2.7 PMA_RXSTATUS.indication

As specified for MultiGBASE-T1 PHYs in 149.2.2.7.

2xx.3.2.8 PMA_REMRXSTATUS.request

As specified for MultiGBASE-T1 PHYs in 149.2.2.8.

2xx.3.2.9 PMA_PCSDATAMODE.indication

As specified for MultiGBASE-T1 PHYs in 149.2.2.9.

2xx.3.2.10 PMA_PCS_RX_LPI_STATUS.request

If EEE is supported.

2xx.3.2.11 PMA_PCS_TX_LPI_STATUS.request

If EEE is supported.

2xx.3.2.12 PMA_ALERTDETECT.indication

If EEE is supported.

2xx.4 Physical Coding Sublayer (PCS) functions, MultiG+100MBASE-T1/V1

The PCS functions for MultiG/100MBASE-T1/V1-H are as specified for MultiGBASE-T1 PHYs in 149.3.

2xx.5 Physical Coding Sublayer (PCS) functions, 100M+MultiGBASE-T1/V1

2xx.5.1 PCS service interface (XGMII)

The low data rate PCS service interface allows the 100M+MultiGBASE-T1/V1 PCS to transfer information to and from a PCS client. The PCS service interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

2xx.5.2 PCS functions

~~*NOTE: Copy of Figure 149-4 needs to be updated to reflect MII instead of XGMII.*~~

2xx.5.2.1 PCS Reset function

The low data rate PCS reset function shall be as specified in Clause 149.3.2.1

2xx.5.2.2 PCS Transmit function

The PCS transmit functions for 100M+MultiGBASE-T1/V1 for the low data rate direction is described in this sub-clause.

After mapping the 8-XGMII transfers to 64B/65B blocks, the subsequent functions of the PCS Transmit process take 4 65B blocks and append 16-bit OAM/Reserved field to each group. This forms the input to the RS-FEC which adds 24 parity bits. The resulting 300 bits are then scrambled.

These bits are then mapped, to DME symbols. Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive. In each symbol period, when communicating with the PMA, the PCS Transmit generates a DME symbol that is transferred to the PMA via the PMA_UNITDATA.request primitive. The symbol period, T, is 1000 / (11.250 × S_up) ps. See Table 2XX–1 for the definition of S_up.

The operation of the PCS Transmit function is controlled by the PMA_TXMODE.indication message received from the PMA PHY Control function. If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit shall generate a sequence (Tn) defined in 149.3.5.1 to the PMA via the PMA_UNITDATA.request primitive. These code-groups are used for training mode and only transmit the values #TBD_training.

During training mode an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes requests for remote transmitter settings. (See 149.4.2.4.)

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the normal mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control. During transmission, the 4 blocks of 64B encoded bits are appended with 16-bit OAM/Reserved field to form the RS-FEC input frame.

During data encoding, PCS Transmit utilizes Reed-Solomon encoders to generate and append 24 parity check bits to form 300 bit RS(50, 46, 6) RS-FEC frames.

Each RS-FEC input frame consists of 276 bits, or 46 Reed-Solomon message symbols. After encoding, the RS-FEC frames from each encoder are recombined into one single interleaved RS-FEC frame, which consists of 50 symbols, or 300 bits. The bits of the RS-FEC frame are then scrambled by the PCS using an additive scrambler, encoded in DME symbols, and transferred to the PMA.

A block diagram of the PCS Transmit functions is shown in Figure 2XX–5.

2xx.5.2.2.1 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into an RS-FEC frame, and vice versa, using a 65B RS-FEC coding scheme. The PMA training frame synchronization allows establishment of RS-FEC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS.

2xx.5.2.2.2 65B RS-FEC transmission code

The low speed direction RS-FEC is RS(50,46,6).

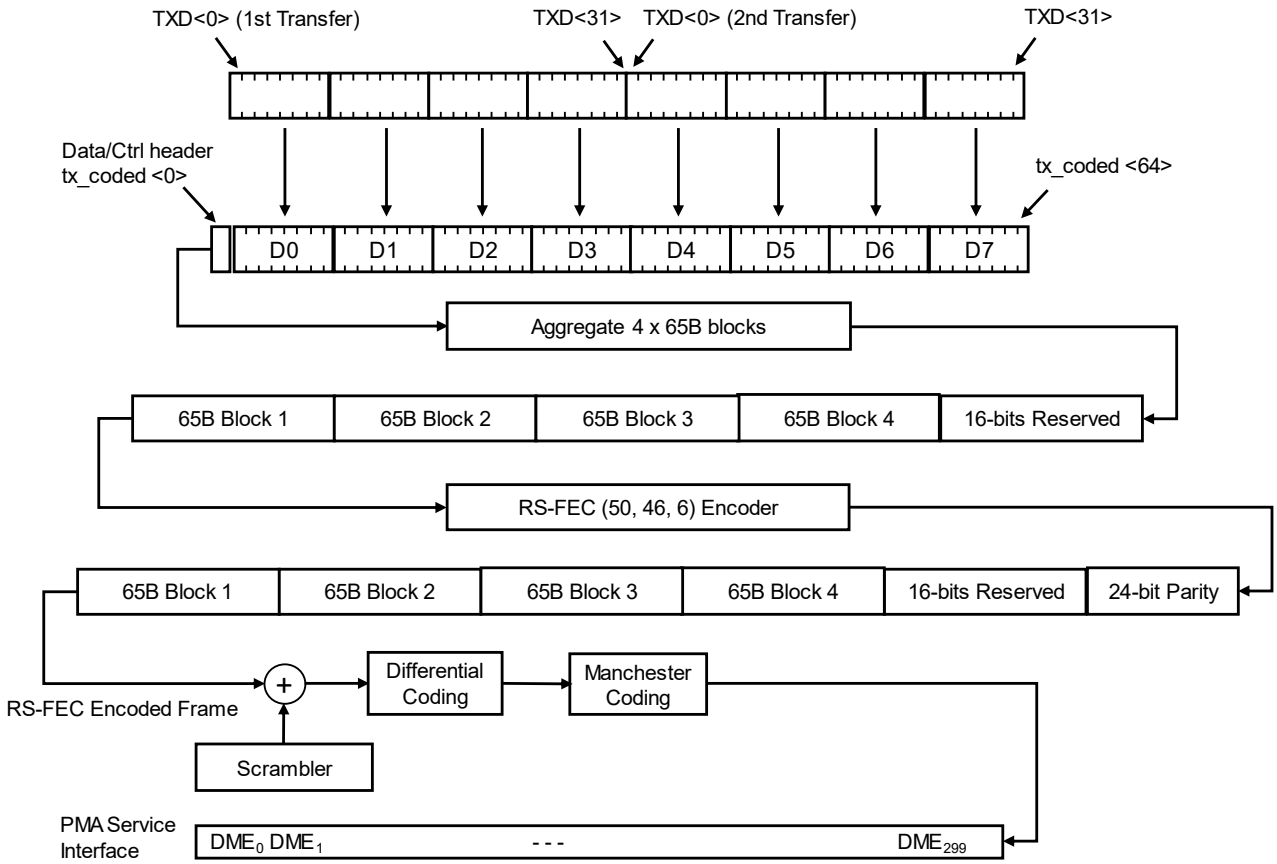


Figure 2XX–5 – PCS Transmit bit ordering

2xx.5.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7. Control characters other than /O/, /S/, and /T/ are labeled C_0 to C_7. The control character for ordered set is labeled as O_0 or O_4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S_0 or S_4 for the same reason. The control character for terminate is labeled as T_0 to T_7.

For 100M+MultiGBASE-T1/V1, two XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfer(s).

2xx.5.2.2.4 Block structure

The low data rate block structure shall be as specified in Clause 149.3.2.2.4

2xx.5.2.2.5 Control codes

The low data rate control codes shall be as specified in Clause 149.3.2.2.5

2xx.5.2.2.6 Ordered sets

The low data rate ordered sets shall be as specified in Clause 149. 3.2.2.6

2xx.5.2.2.7 Idle (/I/)

The low data idle shall be as specified in Clause 149.3.2.2.7

2xx.5.2.2.8 LPI (/LI/)

The low data rate LPI shall be as specified in Clause 149.3.2.2.8

2xx.5.2.2.9 Start (/S/)

The low data rate start shall be as specified in Clause 149.3.2.2.9

2xx.5.2.2.10 Terminate (/T/)

The low data rate terminate shall be as specified in Clause 149.3.2.2.10

2xx.5.2.2.11 Ordered set (/O/)

The low data rate ordered set shall be as specified in Clause 149.3.2.2.11

2xx.5.2.2.12 Error (/E/)

The low data rate error shall be as specified in Clause 149.3.2.2.12

2xx.5.2.2.13 Transmit process

The transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. 8 XGMII data transfers are encoded into an RS-FEC frame. It takes 300 PMA_UNITDATA transfers to send an RS-FEC frame of data. Therefore, for 100MBASE-T1/V1, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly 2:75, then the transmit process does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 2XX and Figure 2XX). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the transcoder and scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

2xx.5.2.2.14 RS-FEC framing and RS-FEC encoder

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 2XX–6 for transmit and Figure 2XX–7 for receive. These figures illustrate the processing of a multiplicity of blocks containing 32 data octets. See 2xx.4.2.2.4 for information on how blocks containing control characters are mapped.

2xx.5.2.2.15 Reed-Solomon encoder

The group of 300 bits are encoded using a Reed-Solomon encoder operating over the Galois Field GF(2^6) where the symbol size is 6 bits. The encoder processes 46 6-bit RS-FEC message symbols to generate 4 6-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 50 6-bit

RS-FEC symbols. For the purposes of this clause, the particular Reed-Solomon code is denoted as RS-FEC(50,46,6).

2xx.5.2.2.16 PCS scrambler

The bits of the interleaved RS-FEC superframe are scrambled using an additive scrambler. For each bit, D_n, a scrambler bit is generated from the side-stream scrambler. The scrambler bit, DS_n, is equal to Scrn[0] defined in 149.3.4.

DSn is applied as additive scrambler sequences to incoming data bits D_n to generate the scrambled data bit A_n as shown in Equation (2XX–4).

$$A_n = DS_n \oplus D_n \qquad \text{(2xx-4)}$$

2xx.5.2.2.17 Differential Manchester encoding (DME)

The scrambled data bit, A_n, is encoded using Differential Manchester Encoding (DME).

2xx.5.2.2.18 EEE capability

Only need if supporting EEE

2xx.5.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure <REF> and Figure <REF>, and the PCS Receive bit ordering in Figure <REF> including compliance with the associated state variables as specified in <REF>.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received DME symbols are demapped and descrambling is performed.

Following descrambling, the L-interleaved RS-FEC superframe is de-interleaved and the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. The RS-FEC decoded frame is then separated into a 16-bit OAM/Reserved field and 4 64B/65B blocks. This process generates the 64B/65B block vector rx_coded<64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure <ref> and Figure <ref>). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received TBD framing and signals the reliable acquisition of the descrambler state by setting the scr_status parameter of the PMA_SCRSTATUS.request primitive to OK.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If 40 consecutive RS-FEC frame errors are detected, the block_lock flag is de-asserted. The block_lock flag is re-asserted upon detection of a valid RS-FEC frame. When block_lock is asserted and hi_rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication(loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-Lnits via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training frame includes an alignment bit every TBD symbols, which is aligned with the PCS partial PHY frame boundary, as well as an Infofield, which is inserted in the 16th PCS partial PHY frame. When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.

2xx.5.2.3.1 Frame and block synchronization

When operating in the data mode, the receiving PCS shall form a DME stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from rx_DME_0 to rx_DME_299 (see Figure <REF>). It obtains block lock to the PHY frames during training using synchronization bits provided in the training frames.

2xx.5.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process for generation of RXD<31:0> to the XGMII. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial per Equation (149–6) and the SLAVE PHY shall employ the receiver descrambler generator polynomial per Equation (149–5).

2xx.5.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exist:

a) The block type field contains a reserved value.

b) Any control character contains a value not in Table <REF>.

c) Any O code contains a value not in Table <REF>.

d) The block contains information from the payload of an invalid RS-FEC frame.

The PCS Receive function shall check the integrity of the RS-FEC parity bits defined in <REF>. If the check fails the RS-FEC frame is invalid.

The R_BLOCK_TYPE of an invalid block is set to E.

2xx.5.3 Test-pattern generators

For 100M+MultiGBASE-T1/V1 test-pattern generator follows Clause 149.3.3, with the exception that the transmission follows illustration in Figure <REF> instead or Figure 149-6 and Figure <REF> instead of Figure 149-7.

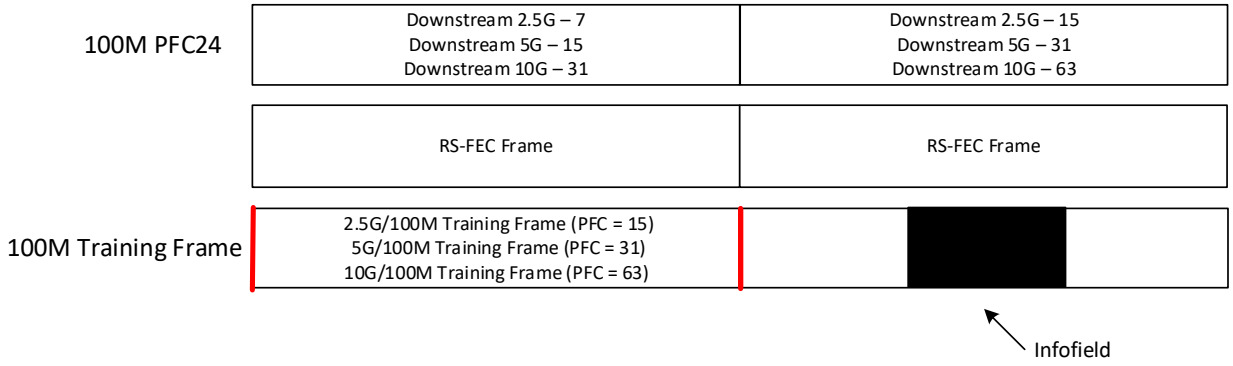
2xx.5.4 Side-stream scrambler polynomials

For 100M+MultiGBASE-T1/V1 side-stream scrambler is as specified in 149.3.4.

2xx.5.5 PMA training frame

During PMA training, the training frames are embedded with indicators to establish alignment to the RS-FEC. Each training frame is composed of 2 partial PHY frames. Each partial PHY frame has the same duration as one RS_FEC frame. The second partial PHY frame is embedded with an information field used to exchange messages between link partners. The timing relationship among training frame, partial frame, RS-FEC frame, and partial PHY frame count (PFC24) are shown in Figure 2XX.

Figure XXX—Timing relationship to PFC24



PMA training frame encoding is based on the generation, at time *n*, of the bit *Sn*. The first bit is inverted in each partial PHY frame. The 100th bit to the 195th bit (counting from 0) of the second partial PHY frame are XORed with the contents of the Infofield. Each partial PHY frame is 300 bits long, beginning at *Sn* where (*n* mod 300) = 0. See Equation (2xx).

$$S_n = \begin{cases} Scr_n[0] \oplus InfoField_{(\text{n mod } 100)} & 400 \le (n \bmod 600) \le 495 \\ Scr_n[0] \oplus 1 & \text{else if } (n \bmod 300) = 0 \\ Scr_n[0] & \text{otherwise} \end{cases}$$

One 100M training frame has the same duration as 1, 2, and 4 downstream training frames for 2.5G, 5G, and 10G respectively. To keep the PFC24 update rate in sync with between the upstream and downstream training frames, the value in the PFC24 field shall be (m+1)*2q – 1 where m is the mth training frame and q is 8, 16, or 32 when the downstream is 2.5G, 5G, and 10G respectively. Each partial frame increments at a rate of q, with the PFC of (m+1)*2q – 1 – q for the first partial frame of the training frame and (m+1)*2q – 1 for the second partial frame.

2xx.5.5.1 Generation of symbol T_n

The 100M+MultiGBASE-T1/V1 T_n symbol is TBD.

2xx.5.5.2 PMA training mode descrambler polynomials

The 100M+MultiGBASE-T1/V1 training mode descrambler is TBD.

2xx.5.6 LPI signaling

Only need if supporting EEE

2xx.5.7 Detailed functions and state diagrams

2xx.5.7.1 State diagram parameters

2xx.5.7.1.1 Constants

2xx.5.7.1.2 Variables

2xx.5.8 PCS management

2xx.5.9 100M+MultiGBASE-T1/V1 operations, administration, and maintenance (OAM)

Only if OAM is used in low speed direction.

2xx.6 Physical Medium Attachment (PMA) sublayer, MultiG+100MBASE-T1/V1

I did not include all subclauses as they can vary with implementation. You can look at any PHY project that is similar to see which may be needed. Other subclauses may be added as baselines are chosen.

The high speed PMA functions are as specified in 149.4.

2xx.7 Physical Medium Attachment (PMA) sublayer, 100M+MultiGBASE-T1/V1

I did not include all subclauses as they can vary with implementation. You can look at any PHY project that is similar to see which may be needed. Other subclauses may be added as baselines are chosen.

The low speed PMA Transmit function comprises a transmitter to generate a DME signal on the MDI interface.

2xx.7.1 PMA functional specifications

2xx.7.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link

Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure <REF>, shows how the operating functions relate to the messages of the PMA service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure <REF>.

2xx.7.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power for the device containing the PMA has not reached the operating state.

b) The receipt of a request for reset from the management entity.

PMA Reset sets pma_reset = ON while any of the above reset conditions hold TRUE. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The MultiG/100MBASE-T1/V1-L PMA takes no longer than TBD ms to enter the PCS_DATA state after exiting from reset or low power mode (see Figure 149–32).

2xx.7.2.2 PMA Transmit

The PMA Transmit function comprises a transmitter to generate a DME modulated signal on the single balanced pair of conductors (T1) or Coaxial cable (V1). When the PHY Control state diagram (Figure 149–32) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by tx_symb onto the MDI. During Link Synchronization, when sync_link_control = DISABLE and Auto-Negotiation is either not enabled or is not implemented, the sync_tx_symb output by the PHY Link Synchronization function shall be used in place of tx_symb as the data source for PMA Transmit. The signals generated by PMA Transmit shall comply with the electrical specifications given in 149.5.2.

When the PMA_CONFIG.indication parameter config is MASTER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 149.5.2.3. The MASTER-SLAVE relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 149.4.2.8 while meeting the jitter requirements of TBD.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

When the PMA_transmit_disable variable is set to TRUE, this function shall turn off the transmitter so that the average launch power of the transmitter is less than –53 dBm.

2xx.7.2.3 PMA Receive function

The low speed PMA Receive function comprises a receiver for DME signal on the MDI. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI and to present these sequences to the PCS Receive function. The PMA translates the signals received at

the MDI into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 2 x after RS-FEC decoding, over a channel meeting the requirements of 149.7.

The low speed direction PMA Receiver function uses the parameters pcs_status and scr_status, along with other applicable receiver status, and generates the loc_rcvr_status variable accordingly The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other value (see the PHY Control state diagram in Figure 149–32). The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for pair polarity swaps.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.193.7.

2xx.7.2.4 PHY Control function

The 100M+MultiGBASE-T1/V1 PHY control functions are as specified in 149.4.2.4.

2xx.7.2.5 Link Monitor function

The 100M+MultiGBASE-T1/V1 link monitoring functions are as specified in 149.4.2.5.

2xx.7.2.6 PHY Link Synchronization

The 100M+MultiGBASE-T1/V1 link synchronization is TBD.

2xx.7.2.7 Refresh monitor function

Only needed if EEE is implemented.

2xx.7.2.8 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RFER indicated in 2xx.7.2.4 is achieved. The received clock signal is expected to be stable and ready for use when training has been completed. The received clock signal is supplied to the PMA Transmit function by received_clock.

2xx.7.3 MDI, T1

The MDI signals are as specified *in 149.4.3, with the exception that* low speed *signaling uses DME instead of PAM4.*

2xx.7.4 MDI, V1

The MDI signals are as specified in *149.4.3, with the exception that* low speed *signaling uses DME instead of PAM4, and that the signals are single ended instead of differential.*

2xx.7.5 State variables

The 100M+MultiGBASE-T1/V1 state variables are as specified in 149.4.4.

2xx.7.6 State diagrams

The 100M+MultiGBASE-T1/V1 state diagrams are as specified in 149.4.4.

2xx.8 Physical Medium Dependent (PMD) sublayer, T1

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests, for differential balanced pair (T1).

2xx.8.1 Test modes

The MultiG+100M/100M+MultiGBASE-T1 test modes, including the test fixtures, are as specified in 149.5.1.

2xx.8.2 Transmitter electrical specifications

The MultiG+100M/100M+MultiGBASE-T1 transmitter electrical specifications are as specified in 149.5.2, with the exceptions listed in this sub-clause.

2xx.8.2.1 Maximum output droop

As specified for MultiGBASE-T1 PHYs in 149.5.2.1.

2xx.8.2.2 Transmitter linearity

As specified for MultiGBASE-T1 PHYs in 149.5.2.2.

2xx.8.2.3 Transmitter timing jitter

As specified for MultiGBASE-T1 PHYs in 149.5.2.3.

2xx.8.2.4 Transmitter power spectral density (PSD) and power level

The MultiG+100MBASE-T1 transmitter power spectral density (PSD) and power level are as specified in 149.5.2.4.

The 100M+MultiGBASE-T1 transmitter power spectral density (PSD) when measured using test mode 3 and the test fixture shown in Figure 147–16, or equivalent, the transmitter Power Spectral Density (PSD) shall be between the upper and lower masks specified in Equation (2xx.8–1) and Equation (2xx.8–2).

$$\mathrm{UpperPSD(f)} = \begin{Bmatrix} -78 & 3 \le \mathrm{f} < 150 \\ -57 - 0.14\mathrm{f} & 150 \le \mathrm{f} < 250 \\ -92 & 250 \le \mathrm{f} < 400 \end{Bmatrix} \mathrm{dBm/Hz} \quad \text{(2xx.8-1)}$$

and

$$\mathrm{LowerPSD(f)} = \begin{Bmatrix} -104 + 0.2f & 50 \le f < 100 \\ -64 - 0.2f & 100 \le f < 150 \end{Bmatrix} \mathrm{dBm/Hz} \quad \text{(2xx.8-2)}$$

where *f* is the frequency in MHz.

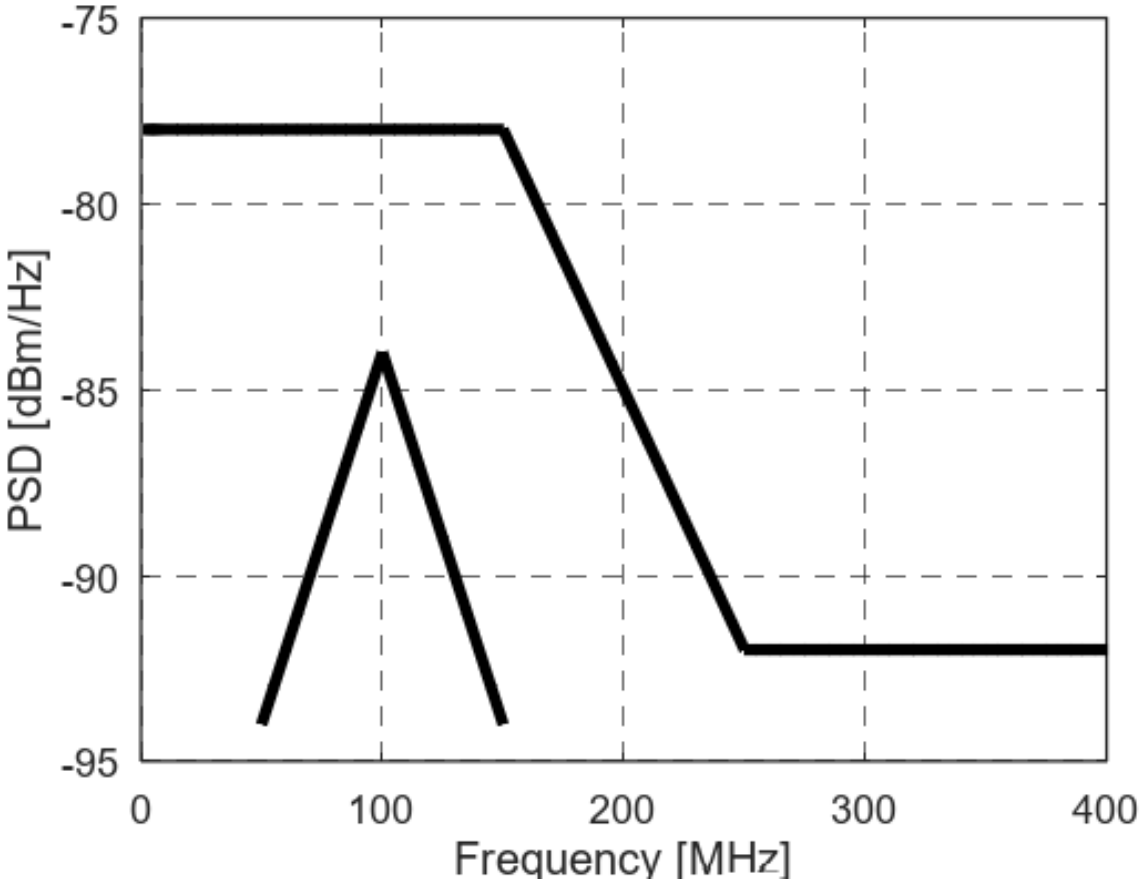


Figure 2XX.9-1—PSD masks for low speed as specified by Equations (2xx.8-1) and (2xx.8-2)

2xx.8.2.5 Transmitter peak differential output

As specified for MultiGBASE-T1 PHYs in 149.5.2.5.

2xx.8.2.6 Transmitter clock frequency

As specified for MultiGBASE-T1 PHYs in 149.5.2.6.

2xx.8.3 Receiver electrical specifications

The MultiG+100M/100M+MultiGBASE-T1 Receiver electrical specifications are as specified in 149.5.3, with the exception listed in this sub-clause.

The cabling used is according to Clause 2xx.11, instead of Clause 149.7.

2xx.8.3.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 2xx.8.2 and have passed through a link specified in 2xx.11 shall be received with a BER less than 10 –12 after RS-FEC decoding, and sent to the XGMII after link reset completion. This specification can be verified by a frame error ratio less than 7.8 × 10–9 for 800 octet frames with minimum IPG or greater than 220-octet IPG.

2xx.8.3.2 External noise rejection

As specified for MultiGBASE-T1 PHYs in 149.5.3.2.

2xx.8.4 MDI

2xx.8.4.1 MDI signals transmitted by the PHY

2xx.8.4.3 Signals received at the MDI

2xx.9 Physical Medium Dependent (PMD) sublayer, V1

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests, for coaxial cables (V1).

2xx.9.1 Test modes

2xx.9.1.1 Test fixtures

2xx.9.2 Transmitter electrical specifications

2xx.9.2.1 Maximum output droop

2xx.9.2.2 Transmitter linearity

2xx.9.2.3 Transmitter timing jitter

2xx.9.2.4 Transmitter power spectral density (PSD) and power level

When measured using test mode 3 and the test fixture shown in Figure <REF>, or equivalent, the transmitter Power Spectral Density (PSD) shall be between the upper and lower masks specified in Equation (2xx.9–1) and Equation (2xx.9–2).

$$\mathrm{UpperPSD(f)} = \begin{Bmatrix} -81 & 3 \le \mathrm{f} < 150 \\ -60 - 0.14\mathrm{f} & 150 \le \mathrm{f} < 250 \\ -95 & 250 \le \mathrm{f} < 400 \end{Bmatrix} \mathrm{dBm/Hz} \quad \text{(2xx.9-1)}$$

and

$$\mathrm{LowerPSD(f)} = \begin{Bmatrix} -107 + 0.2f & 50 \le f < 100 \\ -67 - 0.2f & 100 \le f < 150 \end{Bmatrix} \mathrm{dBm/Hz} \quad \text{(2xx.9-2)}$$

where f is the frequency in MHz.

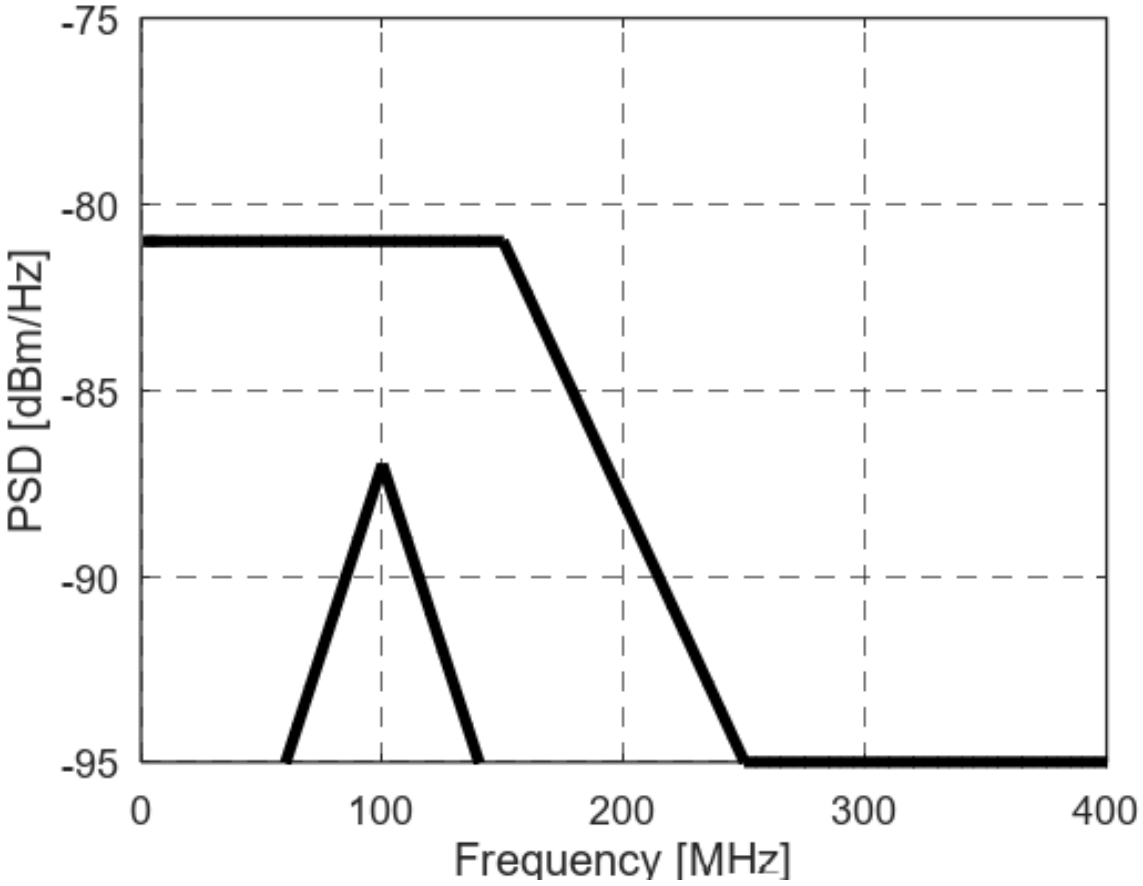


Figure 2XX.9-1—PSD masks for low speed as specified by Equations (2xx.9-1) and (2xx.9-2)

2xx.9.2.5 Transmitter peak output

2xx.9.2.6 Transmitter clock frequency

2xx.9.3 Receiver electrical specifications

2xx.9.3.1 Receiver input signals

2xx.9.3.2 External noise rejection

2xx.9.4 MDI

2xx.9.4.1 MDI signals transmitted by the PHY

2xx.9.4.3 Signals received at the MDI

2xx.10 Management interface

2xx.11 Link segment characteristics, T1

2xx.11.1 Link transmission parameters

2xx.11.1.1 Insertion loss

2xx.11.1.2 Differential characteristic impedance

2xx.11.1.3 Return loss

2xx.11.1.4 Coupling attenuation

2xx.11.1.5 Screening attenuation

2xx.11.1.6 Maximum link delay

2xx.11.2 Coupling parameters between link segments

2xx.11.2.1 Power sum alien near-end crosstalk (PSANEXT)

2xx.11.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

2xx.12 Link segment characteristics, V1

2xx.12.1 Link transmission parameters

2xx.12.1.1 Insertion loss

2xx.12.1.2 Differential characteristic impedance

2xx.12.1.3 Return loss

2xx.12.1.4 Coupling attenuation

2xx.12.1.5 Screening attenuation

2xx.12.1.6 Maximum link delay

2xx.12.2 Coupling parameters between link segments

I wasn't sure what the correct parameters are, so I just copied the T1 crosstalk titles for placeholders.

2xx.12.2.1 Power sum alien near-end crosstalk (PSANEXT)

2xx.12.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

2xx.13 MDI specification, T1

2xx.13.1 MDI connectors

2xx.13.2 MDI electrical specification

2xx.13.2.1 MDI return loss

2xx.9.4.1 MDI return loss

The differential impedance at the MDI for each transmit/receive channel shall be such that any reflection due to signals incident upon the MDI from the cabling relative to the incident signal are per the relationship shown in Equation (2XX-1). For coaxial cabling a nominal characteristic impedance of 50Ω is used.

$$MDI\_Return\_Loss(f) \leq \begin{cases} 18 - 20\log10\left(\frac{f}{50}\right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13\log10\left(\frac{f}{400}\right) & 400 \leq f < Fmax \end{cases} \text{(dB)} \qquad (200\text{–}1)$$

where

f is the frequency in MHz.

NOTE: The equation above is the agreed text, but there is an error in the sign of the second term in the frequency range from 10Mbps to 50Gbps. It should be "18+20 log10(f/50)".

For MultiG+100M/100M+MultiGBASE-T1 the maximum applicable frequency, *Fmax*, for the MDI return loss is 4000 MHz.

Note: Fmax should scale with baud rate once the transmit signals are established.

The MDI return loss for 10G+100MBASE-T1 and 100M+10GBASE-T1 is illustrated in Figure 2XX-2.

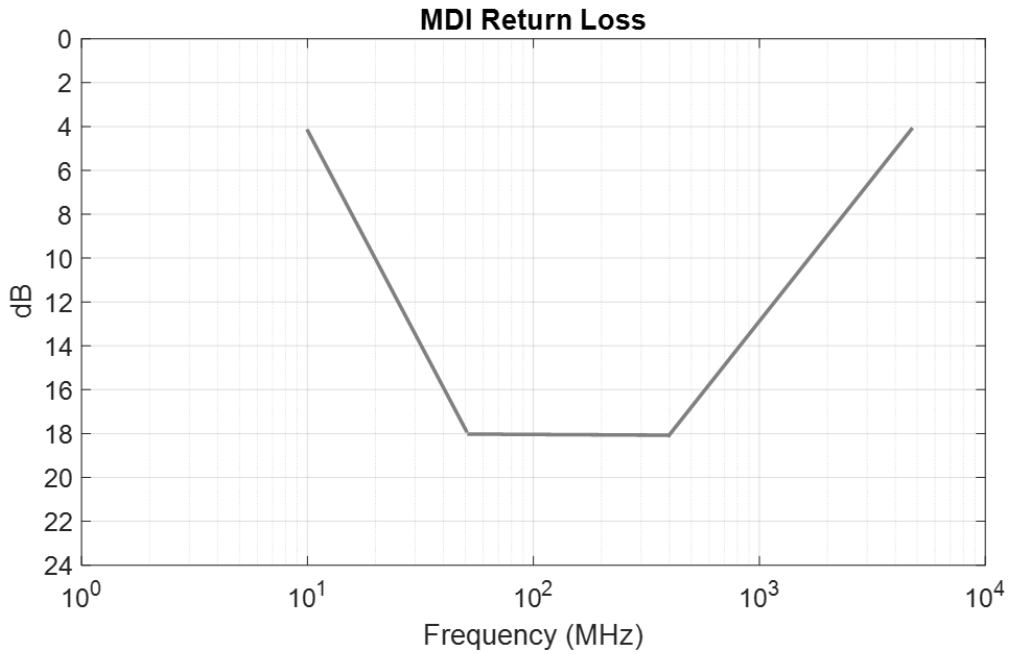


Figure 2XX-2—MDI return loss calculated using Equation (2XX-1)

2xx.13.3 MDI fault tolerance

2xx.14 MDI specification, V1

2xx.14.1 MDI connectors

2xx.14.2 MDI electrical specification

2xx.14.2.1 MDI return loss

The MDI return loss for coax cables is as specified in 2xx.13.2.1.

2xx.14.3 MDI fault tolerance

2xx.15 Environmental specifications

The environmental specifications for *MultiG+100M/100M+MultiGBASE-T1/V1* are as specified in 149.9.

2xx.15.1 General safety

2xx.15.2 Network safety

2xx.15.2.1 Environmental safety

2xx.15.2.2 Electromagnetic compatibility

2xx.16 Delay constraints

The delay constraints for *MultiG+100M/100M+MultiGBASE-T1/V1* are as specified in 149.10 with the exceptions and extensions in this sub-clause.

The delay limits for 100Mb/s low speed direction are TBD.

2xx.17 Protocol implementation conformance statement (PICS) proforma for Clause 2xx