Linkup Process for a TDD based Camera Link

March 10, 2025

Atlanta, Georgia

Ahmad Chini, Mehmet Tazebay

Broadcom Corporation

Contributors and Supporters

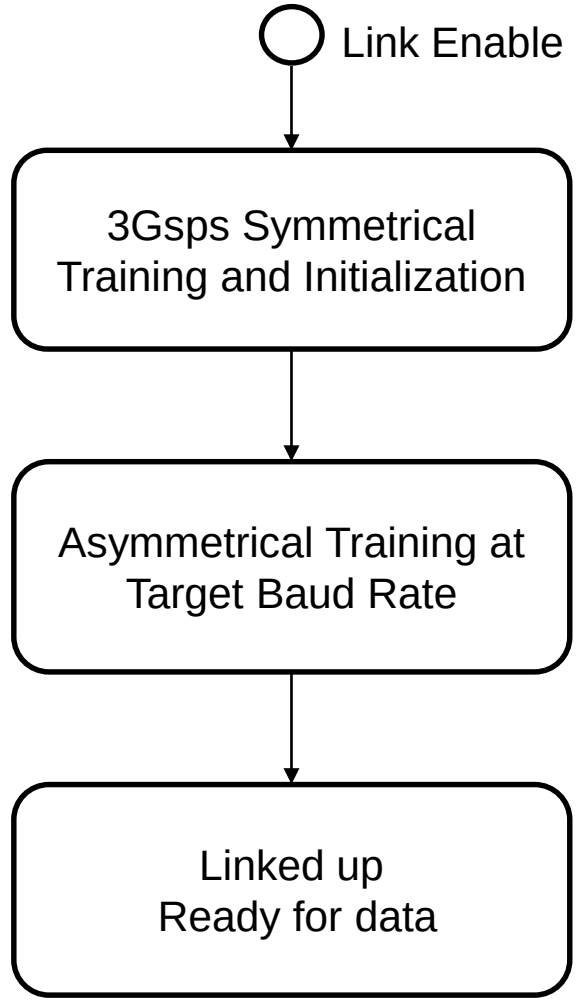
- Scott Muma, Microchip
- Ramanjit Ahuja, Onsemi
- Frank Wang, Realtek
- Kamal Dalmia, Avivalinks
- Wei Lou, Broadcom
- Mehdi Kilani, Broadcom

Linkup process for TDD Top States

A linkup process for a TDD-based[1] camera link is proposed.

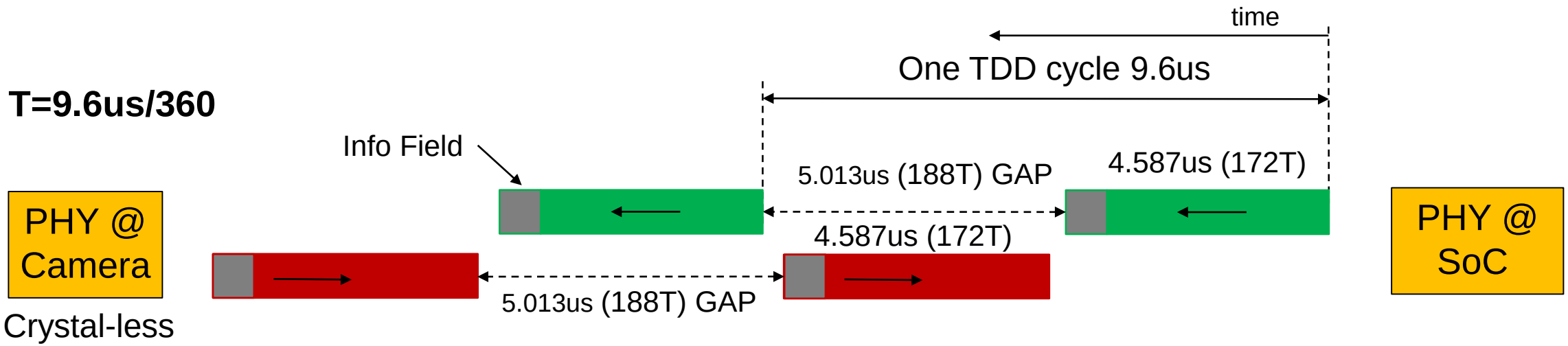
The process involves a symmetrical training at both side of a link at 3Gsps. This stage includes clock synchronization, equalization and capability exchange.

The next step, is to train SoC side PHY's equalizer at higher baud rates and target modulation level before the link is ready for normal mode operation.



1- https://www.ieee802.org/3/dm/public/0125/Chini_3dm_01a_0125.pdf

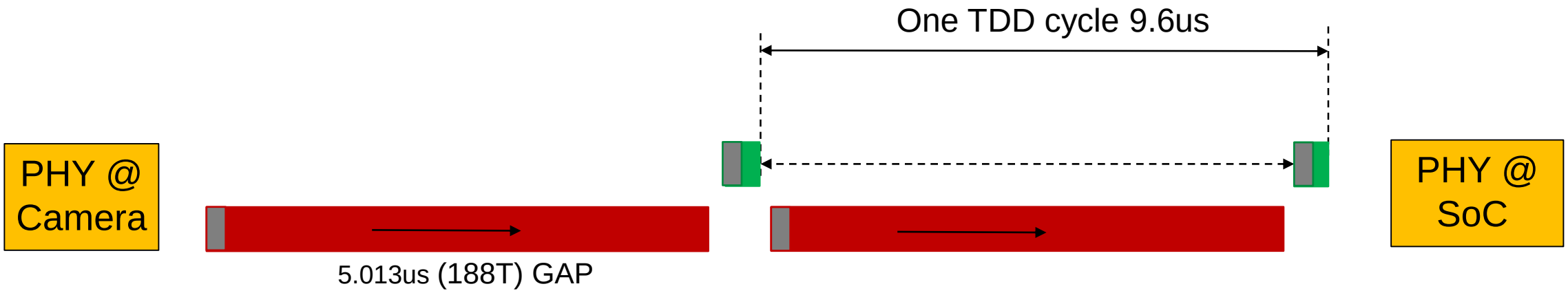
3Gsps Symmetrical Training and Initialization



1. SoC side PHY transmits bursts, synchronous with TDD cycles (PAM2, 3Gsps).
2. Camera side PHY, uses the on/off cycles (~104KHz) of received bursts to adjust its reference clock (coarse tuning).
3. Camera side PHY adapts its equalizer and reference clock on the 3Gsps received signal (CDR, fine tuning).
4. Camera side PHY transmits bursts 133ns (5T) after finished receiving a burst from the SoC side PHY.
5. SoC side PHY trains its equalizer on the received bursts from the Camera side PHY.
6. Propagation delay is measured by SoC side PHY (round trip delay divide by 2).
7. Info field is used to exchange capability, link preferences and optional camera initialization.
8. Go to the next state (info field count down).

- If Camera side PHY has a local reference, either side configured as a leader starts the linkup process.

Asymmetrical Training at Target Baud Rate



1. Adjust the bursts size and baud rate:
   - Bursts sizes are adjusted as in the Normal mode (Modulation remains PAM2).
   - SoC side PHY sends bursts at 3Gsps while the Camera side PHY sends bursts at the target link speed (3Gsps or 6Gsps) and set power level according to 2.5Gbps or 5Gbps link.
   - Camera transmit bursts (106.66ns minus propagation delay) after received a burst.
2. SoC side PHY adapts equalizer at the target baud rate.
3. If target forward link speed in the Camera side PHY is not 10Gbps and both sides are ready, set the link status to “Link_Up”.
4. If forward link speed is 10Gbps, continue training at PAM4 level before setting the link status to “Link_Up”.

Thank you for your attention!

Questions?