Insertion Loss, Return Loss, Secondary Reflections, and ISI as it relates to 802.3dm

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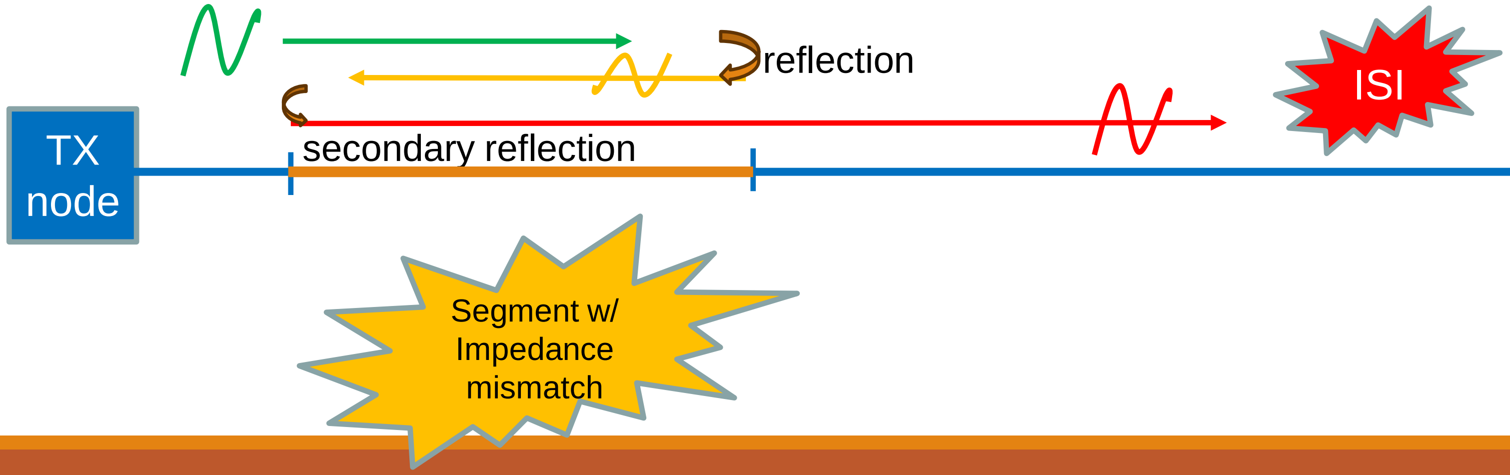
Problem Statement

Mismatches in cable segments and connectors in a harness can potentially cause large secondary reflections

- This is the cause of R. Jonsson's "bad connector" (jonsson_3dm_02_09_15_24.pdf
- This is also the cause of C. Zerna's increased return loss limit (Zerna_802.3dm_01_250122_IL_RL.pdf)
- Secondary reflections can be characterized by the periodicity in the return loss, typical of the delay between point reflections



reflection

ISI

secondary reflection

TX node

RX node

Segment w/ Impedance mismatch

ILD in the Frequency Domain

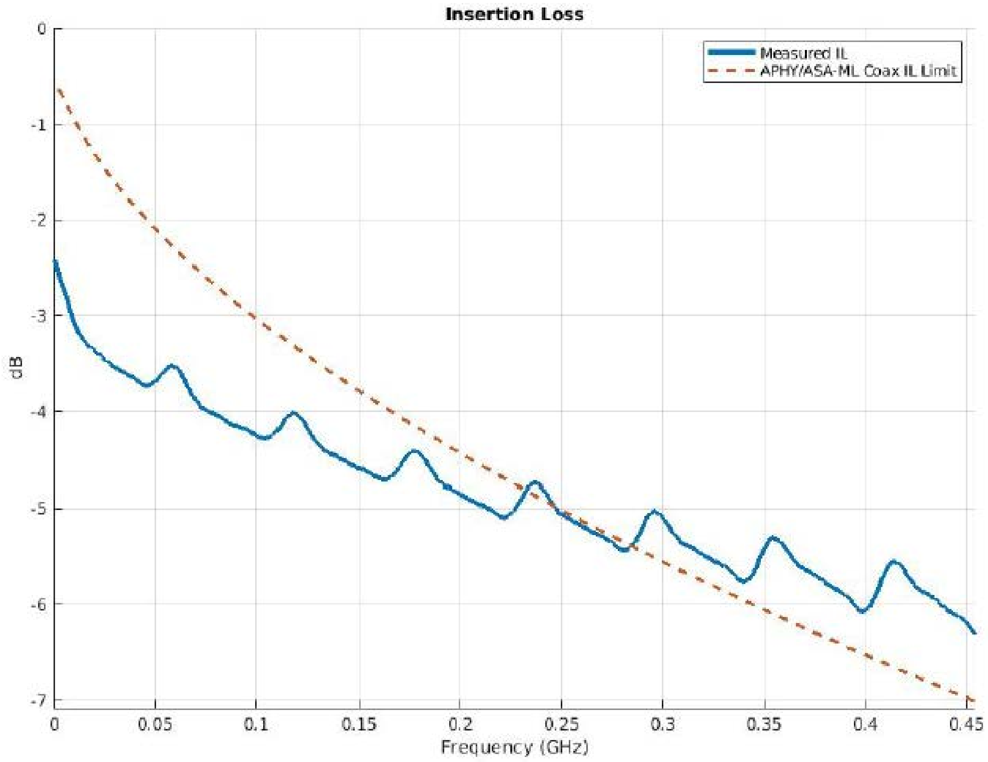
Insertions Loss Deviations from a smooth decreasing profile in the frequency domain

- Often periodic (but not always)

Potential Causes:

- Bad connectors
- Mismatched cable segments
- Point defects (e.g., repair spots)

Increased Equalization Difficulty



[ahuja_8023dm_01e_11112024_poorreturnloss_equalization.pdf]

The Periodicity is the signature of Point Reflections at the Connectors

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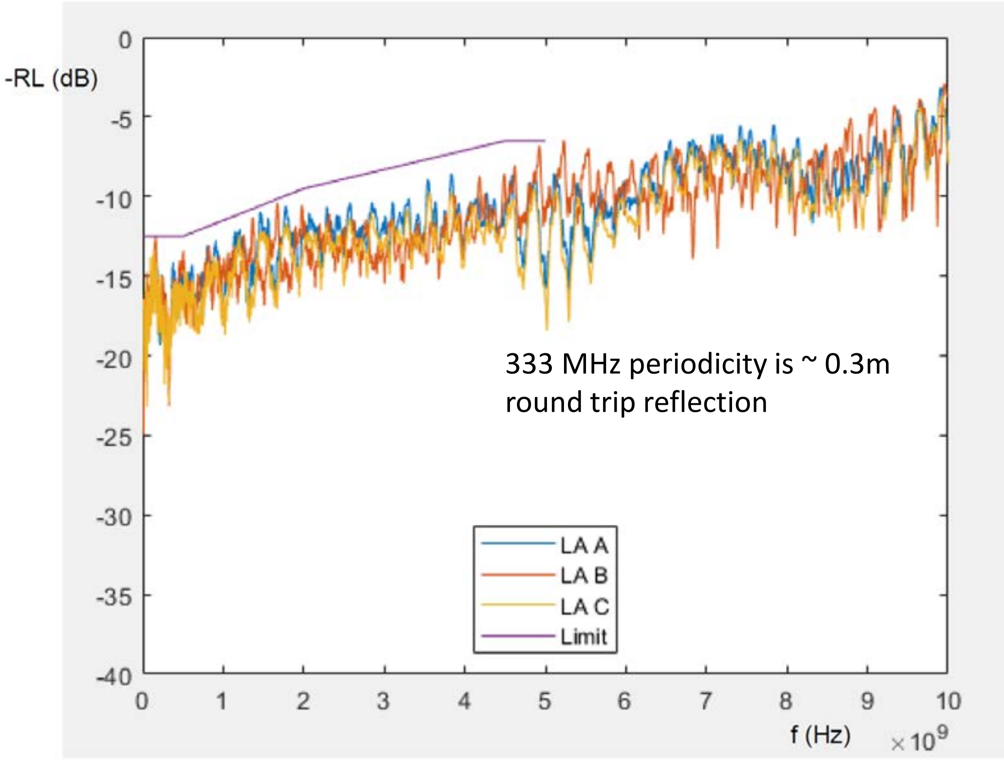
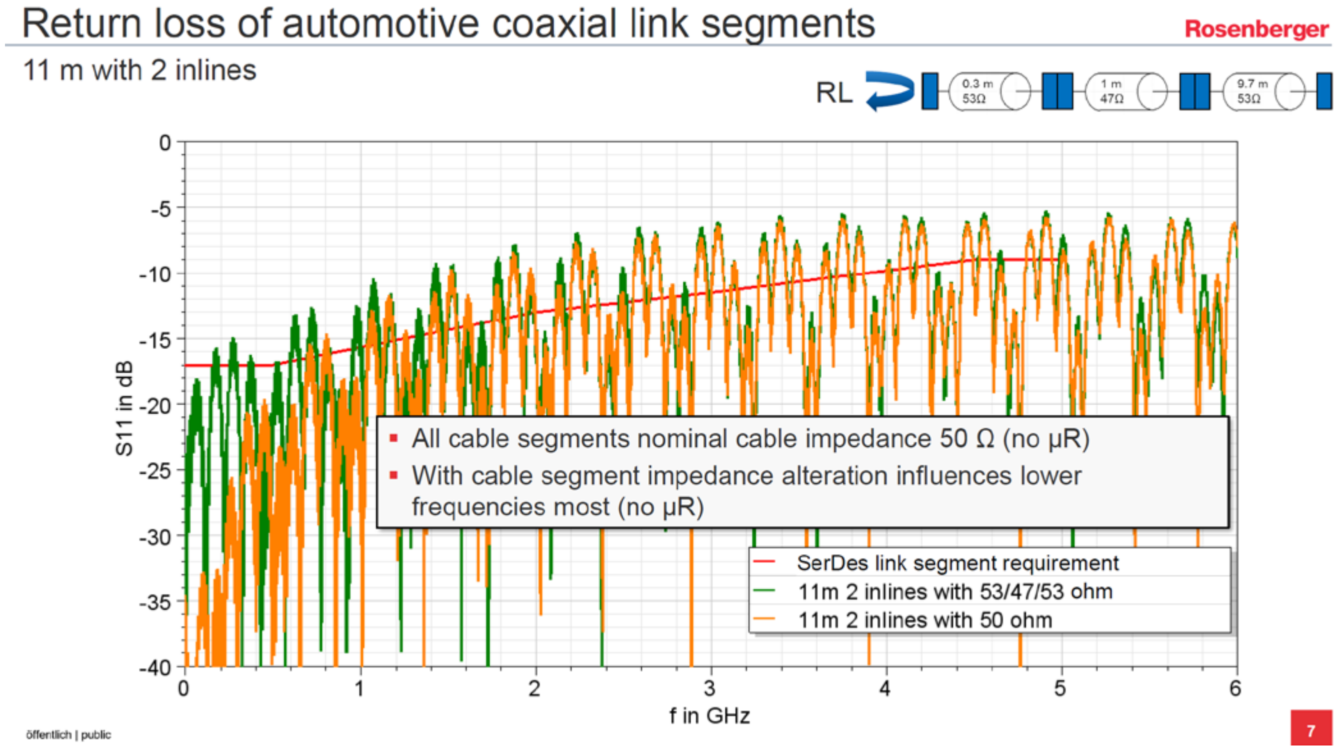
Periodicity in spectral peaks are signatures of point reflections



333 MHz periodicity is ~ 0.3m round trip reflection

Zerna_802.3dm_01_250122_IL_RL.pdf



Return loss of automotive coaxial link segments

Rosenberger

11 m with 2 inlines

- All cable segments nominal cable impedance 50 Ω (no µR)
- With cable segment impedance alteration influences lower frequencies most (no µR)

öffentlich | public

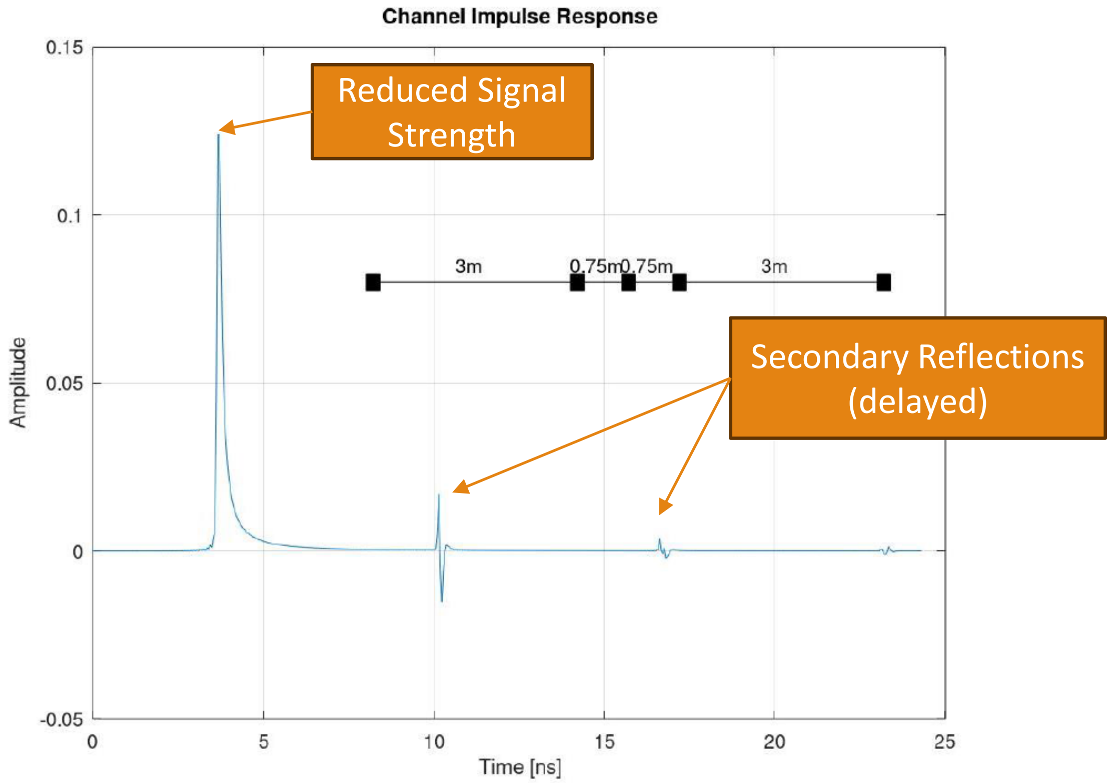
7

mueller_3dm_01a_07_01_24.pdf

Time Domain View

Secondary Reflections create ISI at the round-trip delay of the mismatched segment

- Secondary reflections increase equalization complexity
- Increase PHY power & relative cost



Reduced Signal Strength

Secondary Reflections (delayed)

jonsson_3dm_01a_08_28_24.pdf

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Why isn’t ILD in “BASE-T” PHYs?

In traditional (LAN) BASE-T PHY link segments:

- Insertion loss has largely been determined solely by the longest, most lossy line
- Return loss has largely been considered as it impacts echo cancellation
  - Sometimes Return Loss is even scaled to require better performance on long link segments
- Intersymbol interference (ISI) of “Secondary reflections” concerns have been dominated by MDI return loss considerations on short / low-loss lines
  - Forces equalizer designs that mitigate moderate ILD as well

ILD isn’t limiting in LAN PHY applications because:

- Groups like TIA TR42 specify component and segment-wise performance at the inline connections to reduce secondary reflections impact on equalization
- Signaling is slow enough and processing power high enough to correct for the remaining impact

Compromises with Increasing Speed

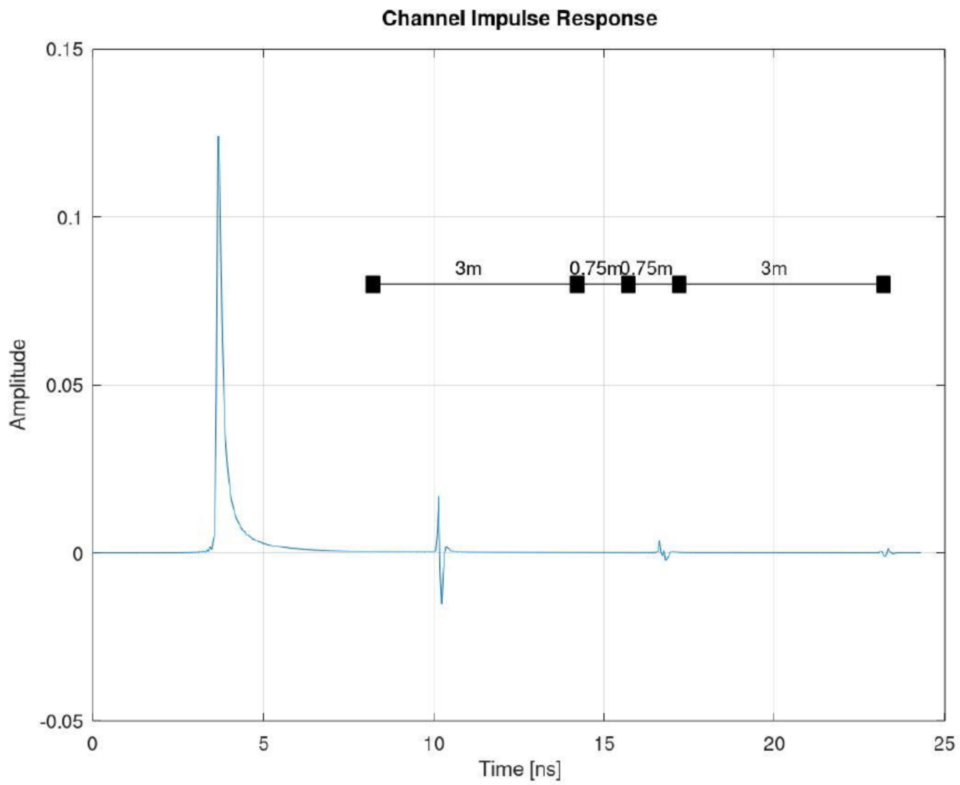
Complexity is Constrained

- Power requirements shorten Feedforward equalizers
- Timing closure shortens DFE Feedback lengths

Use of CTLEs or analog equalizers compounds these

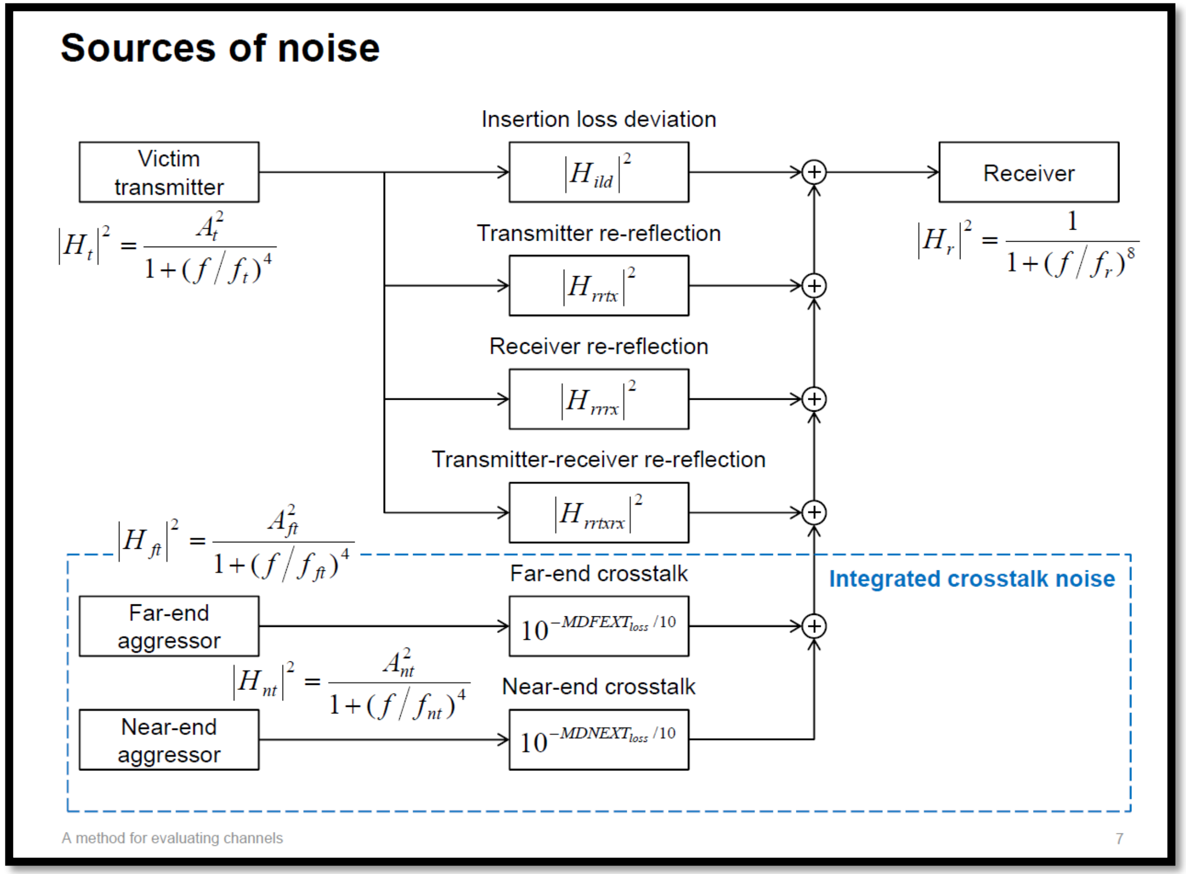
- Generally matched to the "fit"

Reflections outside the filter span are uncancelled ISI



jonsson_3dm_01a_08_28_24.pdf

ILD is a recognized source of noise in SERDES PHYs ($H_{ild} = H - H_{fit}$)



Sources of noise

Insertion loss deviation

Victim transmitter

$|H_{ild}|^2$

Receiver

$$|H_t|^2 = \frac{A_t^2}{1+(f/f_t)^4}$$

Transmitter re-reflection

$|H_{rrtx}|^2$

$$|H_r|^2 = \frac{1}{1+(f/f_r)^8}$$

Receiver re-reflection

$|H_{rrrx}|^2$

Transmitter-receiver re-reflection

$|H_{rrtxrx}|^2$

$$|H_{ft}|^2 = \frac{A_{ft}^2}{1+(f/f_{ft})^4}$$

Far-end crosstalk

Integrated crosstalk noise

Far-end aggressor

$10^{-MDFEXT_{loss}/10}$

$$|H_{nt}|^2 = \frac{A_{nt}^2}{1+(f/f_{nt})^4}$$

Near-end crosstalk

Near-end aggressor

$10^{-MDNEXT_{loss}/10}$

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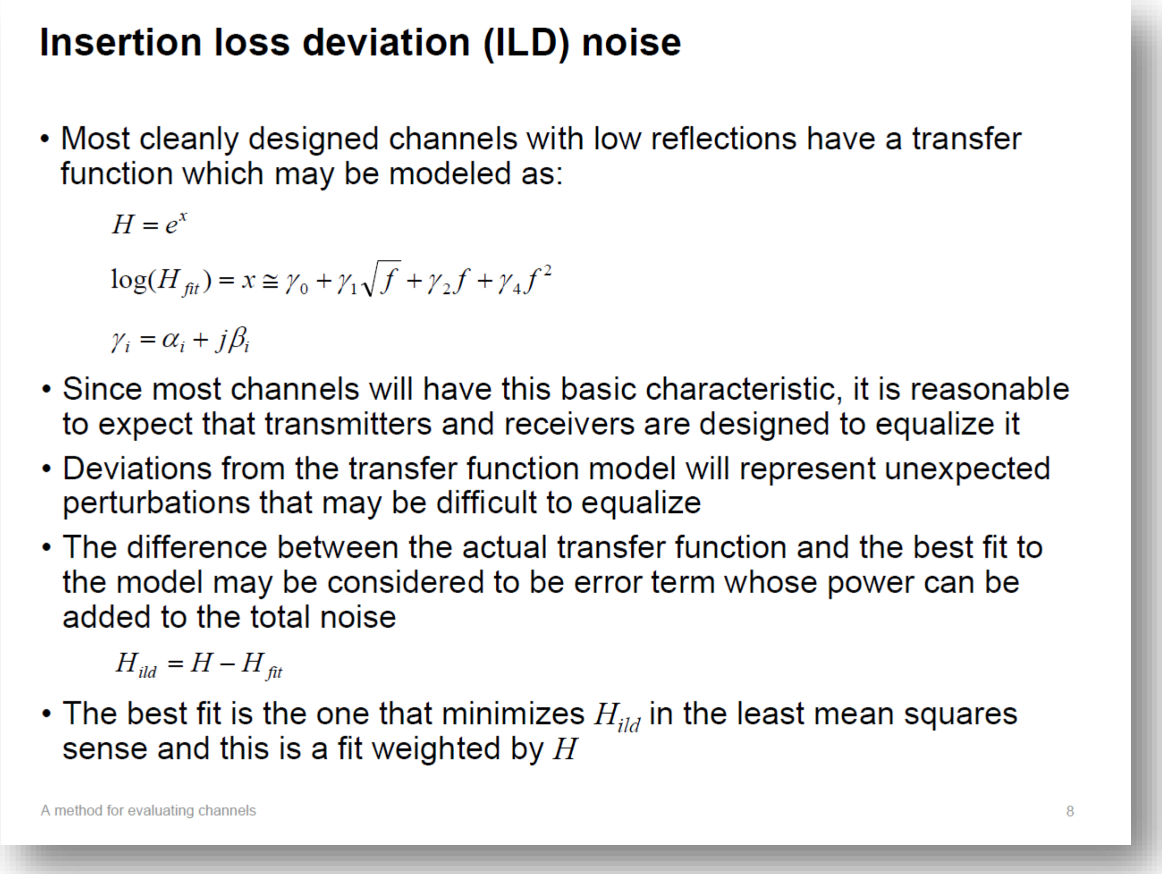

Insertion loss deviation (ILD) noise

- Most cleanly designed channels with low reflections have a transfer function which may be modeled as:

$$H = e^x$$

$$\log(H_{fit}) = x \cong \gamma_0 + \gamma_1\sqrt{f} + \gamma_2 f + \gamma_4 f^2$$

$$\gamma_i = \alpha_i + j\beta_i$$

- Since most channels will have this basic characteristic, it is reasonable to expect that transmitters and receivers are designed to equalize it
- Deviations from the transfer function model will represent unexpected perturbations that may be difficult to equalize
- The difference between the actual transfer function and the best fit to the model may be considered to be error term whose power can be added to the total noise

$$H_{ild} = H - H_{fit}$$

- The best fit is the one that minimizes H_{ild} in the least mean squares sense and this is a fit weighted by H

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https://www.ieee802.org/3/100GCU/public/mar11/moore_01_0311.pdf

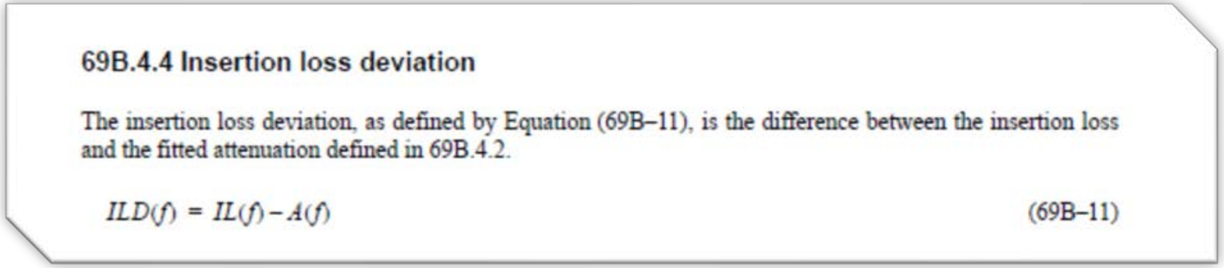
SERDES technology specifies ILD

Discussed for SERDES in IEEE Std 802.3 rates from 1 Gbps on up:

- IEEE P802.3ba 40 Gb/s and 100 Gb/s Ethernet Task Force
  - https://www.ieee802.org/3/ba/public/nov08/diminico_02_1108.pdf
  - https://www.ieee802.org/3/ba/public/jan09/healey_01_0109.pdf
- IEEE P802.3bj 100 Gb/s Backplane and Copper Cable Task Force.
- IEEE P802.3cb 2.5Gb/s and 5Gb/s Operation over Backplane Task Force
  - https://www.ieee802.org/3/cb/public/may16/Wu_3cb_05_0516.pdf
- IEEE Std 802.3-2022 at:
  - 1 GBd to 5 GBd Rates (1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KX4) – (informative) Annex 69B
  - 10 GBd rates (10GBASE-KR, 40GBASE-KX4, 40GBASE-CR4,100GBASE-CR10): Annex 69B, Clause 85, Annex 85A
  - 13 GBd rates (100GBASE-KP4): Clause 94
  - 25 GBd rates (25GBASE-KR, 100GBASE-CR4, 100GBASE-KR4): Clause 93
  - Channel Specifications: 93A.4: Annex 93A (normative) Specification methods for electrical channels

How is ILD specified?

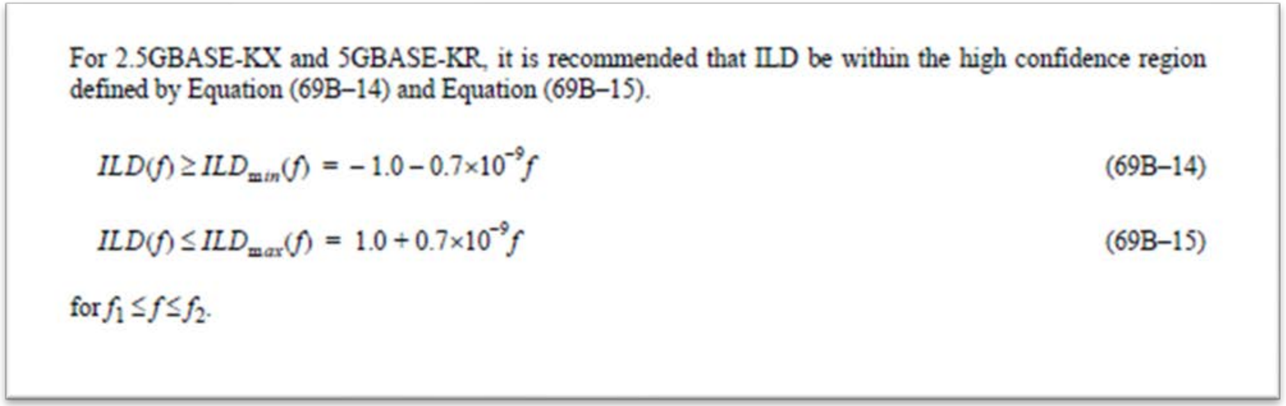
1. Fit an insertion loss to a smooth curve
2. Take the difference
3. Constrain the difference
    - Multiple ways the constraint is formed…



69B.4.4 Insertion loss deviation

The insertion loss deviation, as defined by Equation (69B–11), is the difference between the insertion loss and the fitted attenuation defined in 69B.4.2.

$$ILD(f) = IL(f) - A(f) \qquad (69B\text{–}11)$$

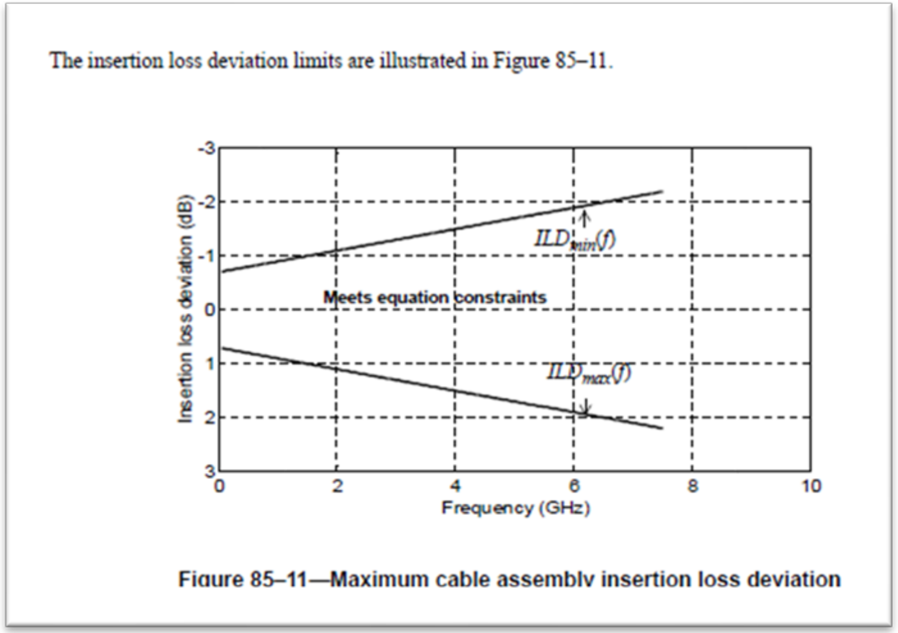


For 2.5GBASE-KX and 5GBASE-KR, it is recommended that ILD be within the high confidence region defined by Equation (69B–14) and Equation (69B–15).

$$ILD(f) \geq ILD_{min}(f) = -1.0 - 0.7\times10^{-9}f \qquad (69B\text{–}14)$$

$$ILD(f) \leq ILD_{max}(f) = 1.0 + 0.7\times10^{-9}f \qquad (69B\text{–}15)$$

for $f_1 \leq f \leq f_2$.



The insertion loss deviation limits are illustrated in Figure 85–11.

Figure 85–11—Maximum cable assembly insertion loss deviation

Why does this matter now?

802.3dm is striving for a highly optimized design at high rates… compromises will be made

Repeatability of performance will suffer without an ILD specification

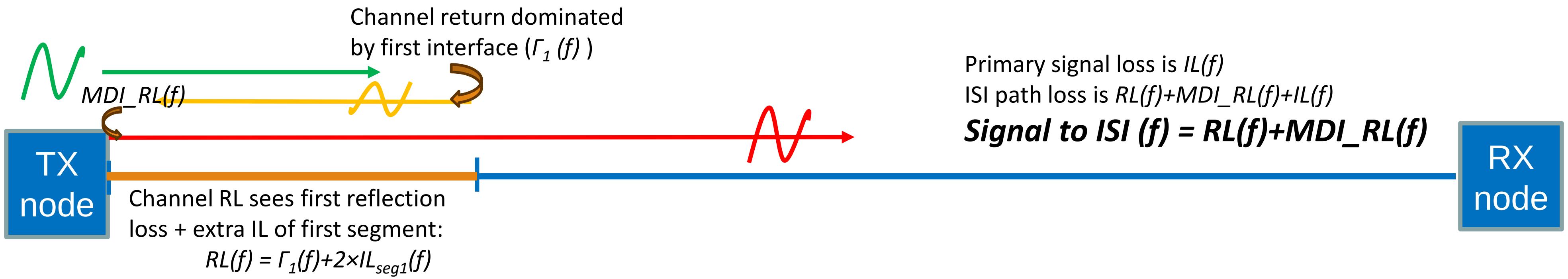
Specifying ILD is likely to change our RL models too!

- Constraining reflections will constrain the random matches of cables in the models discussed in Zerna_802.3dm_01_250122_IL_RL.pdf
  - Oscillations and peaks will be smoothed out
  - Will improve the RL seen in simulations and monte-carlo combinations of inline segments by excluding some mismatches
  - How much? *Hard to tell without complete access to the data*

Do Secondary Reflections Matter?

Simple, Bad Case (not provably worst):

- First connector dominates channel RL, secondary reflection is off the MDI



Channel return dominated by first interface ($\Gamma_1(f)$)

Primary signal loss is *IL(f)*

ISI path loss is *RL(f)+MDI_RL(f)+IL(f)*

Signal to ISI (f) = RL(f)+MDI_RL(f)

Channel RL sees first reflection loss + extra IL of first segment:

$RL(f) = \Gamma_1(f)+2\times IL_{seg1}(f)$

Signal to ISI can be evaluated by integrating RL(f)+MDI_RL(f) over the Nyquist bandwidth

- Can be performed both for linear equalization and using the Salz DFE (logarithmic) bound

How do our Return Loss metrics stand up?

- ASA 2.0 Equation 4-31
- Zerna proposal (Zerna_802.3dm_01_250122_IL_RL.pdf, slide 10)
- Boyer proposal (boyer_sharma-3dm_02_RevA_01-22-25.pdf slide 11)

	ASA 2.0		Zerna		Boyer	
BW MHz	**Linear EQ/ISI dB**	**Salz DFE S/ISI dB**	**Linear EQ/ISI dB**	**Salz DFE S/ISI dB**	**Linear EQ/ISI dB**	**Salz DFE S/ISI dB**
300	35.00	35.00	30.50	30.50	32.00	32.00
1500	29.05	30.46	25.76	26.70	26.25	27.65
3000	22.93	25.68	19.75	22.32	20.54	23.17

6 to 10 dB lower SNR than PHY-noise limited performance analysis (page 7 Chini_3dm_02a_0125.pdf)

Observations and what to do next

This phenomenon is unlikely to have been seen on PHYs with Nyquist bandwidths below 1.25 Gbaud (2.5GBASE-T1 and lower rate 802.3 PHYs)

Experience with early cables for 802.3 and ASA PHYs, plus measurements made indicate cables can be made, BUT, standards need to last – interoperability is undermined by assuming a spec is met always

Suggest that PHY and Cabling experts collaborate to develop a specification based on experience that can be met without excessive burden in yield or test and yet provides guarantee for minimal PHY impact for consideration in the 802.3dm specification

Reports are the windowed time-domain measurements are being used to qualify harnesses for secondary reflections today. Perhaps these can be adapted in a standardized way.

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Thank you

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Some references from SERDES specifications

802.3ba (10Gb/s & 40Gb/s, https://www.ieee802.org/3/ba/public/)

- nov08/diminico_02_1108.pdf, jan09/healey_01_0109.pdf

802.3_100GCU (100Gb/s Backplane SG https://www.ieee802.org/3/100GCU/public/):

- mar11/moore_01_0311.pdf

802.3cb (2.5Gb/s & 5Gb/s Backplane, https://www.ieee802.org/3/cb/public/):

- may16/Wu_3cb_05_0516.pdf

MathWorks®: Creating Compliance Masks in Serial Link Designer

DesignCon 2020: Finding Reflective Insertion Loss Noise and Reflectionless Insertion Loss; (Samtec)