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Evaluation of 802.3ch for Automotive Sensor PHY

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Supporters

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Agenda

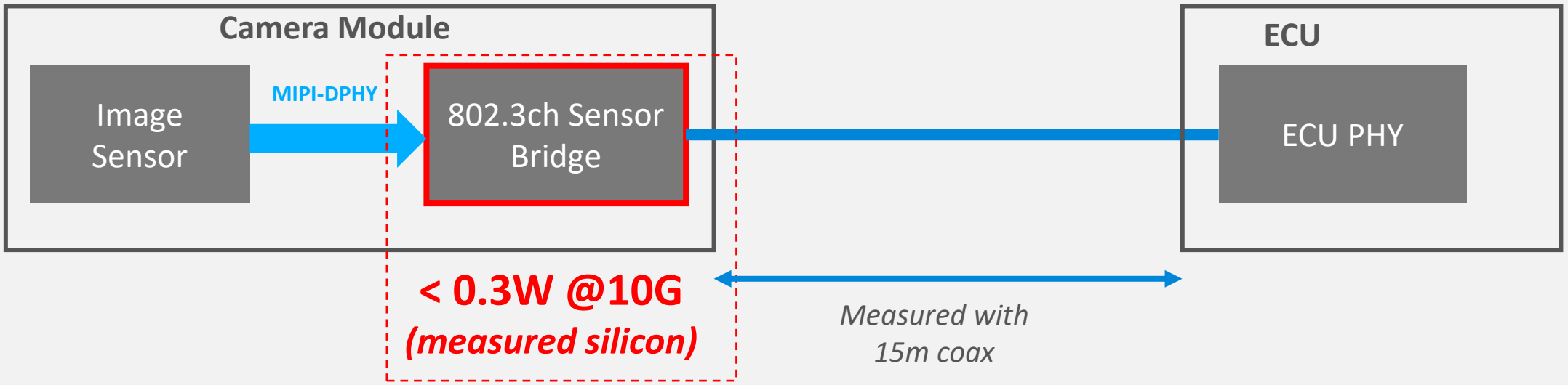
- Motivation of the contribution
- Key evaluation factors
  - Power consumption of 802.3ch PHY with EEE for asymmetric link
  - Coax performance
  - Check 802.3ch PHY against ISAAC objectives
- Conclusion

Motivation

- Provide silicon test results of 802.3ch PHY as a reference data point for 802.3dm task group
- Evaluate 802.3ch PHY against 802.3dm objectives
- Identify potential areas of improvement

Power Consumption Evaluation

10Gbps CSI-2 to 802.3ch Bridge Chip Power



Parameter	Value	Comment
Bridge chip Power	**< 0.3W**	Whole chip, all supplies/circuits. TT, room temp
PHY Power	**< 0.2W**	PHY port + supporting circuitry. Implemented with EEE as specified by 802.3ch
% time in full duplex data mode	< 0.5%	Detailed value sensitive to packetization/tunneling scheme. IEEE1722 is used for this data point. However, in general it is *a very small ratio*

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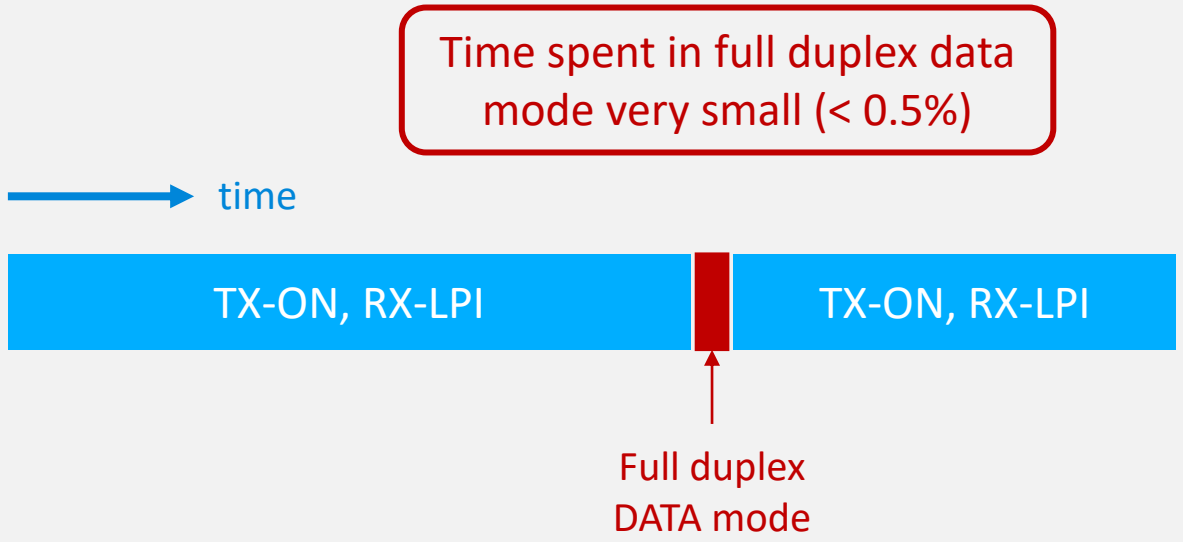
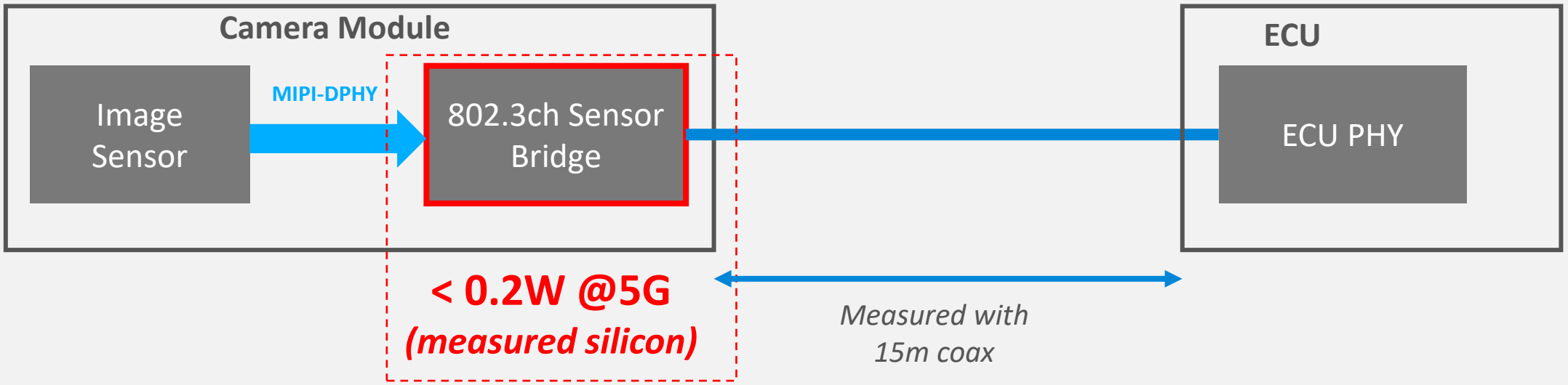
Full duplex time for uplink

- RX power is low for typical camera serializer applications
  - Only small intervals to transmit i2C, Frame sync uplink
  - Can get 100Mbps equivalent uplink with negligible power impact



5Gbps CSI-2 to 802.3ch Bridge Chip Power



Parameter	Value	Comment
Bridge chip Power	**< 0.2W**	Whole chip, all supplies/circuits. TT, room temp
PHY Power	**< 0.15W**	PHY port + supporting circuitry. Implemented with EEE as specified by 802.3ch
% time in full duplex data mode	< 0.5%	Detailed value sensitive to packetization/tunneling scheme. IEEE1722 is used for this data point. However, in general it is *a very small ratio*

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Is < 0.3W @ 10Gbps/15m Low Enough?

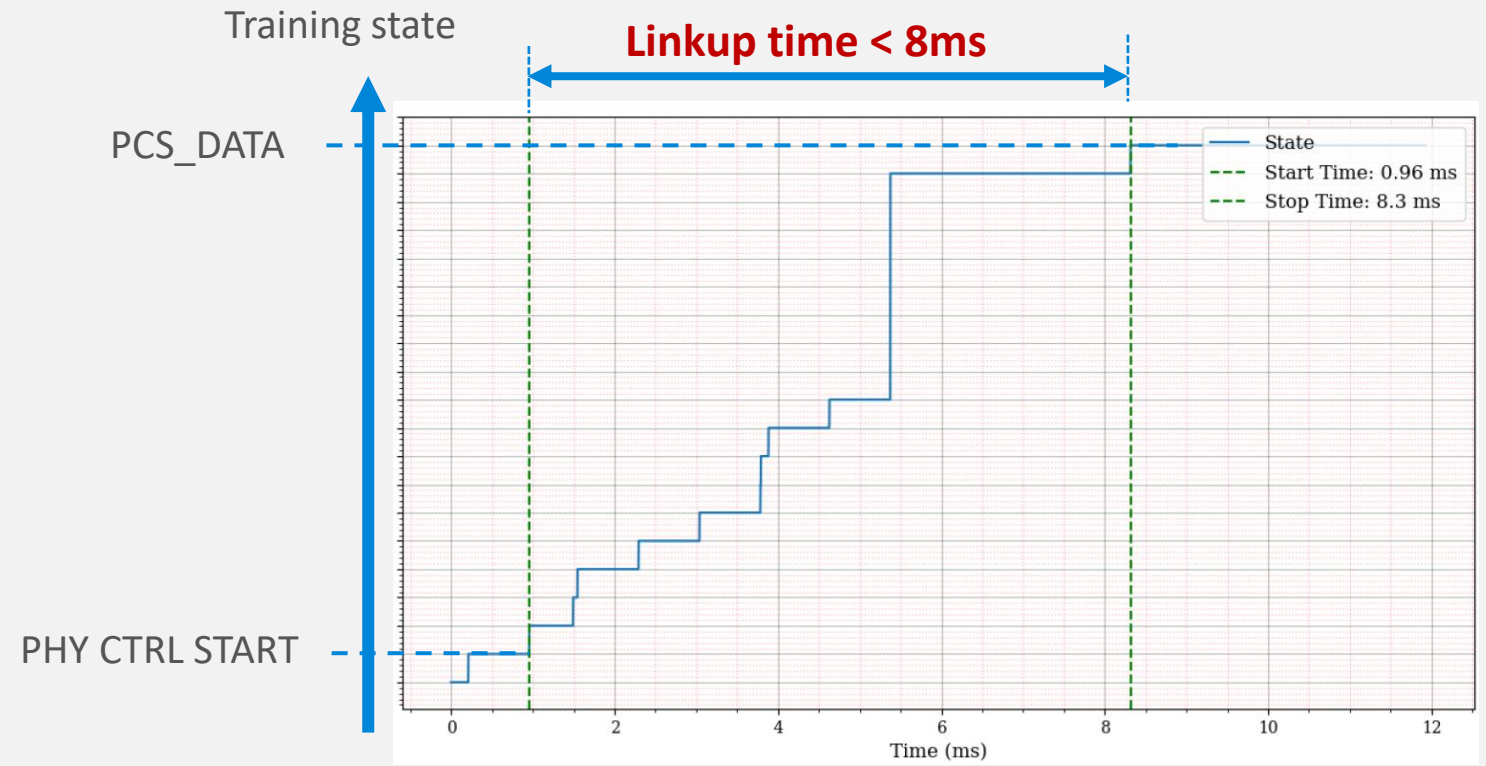
Chip	Payload downstream (Gbps)	Line rate (Gbps)	Reach (m)	Power * (W)	Source
CSI-802.3ch Bridge	10	11.25	15	**< 0.3**	
Proprietary Serializer A3	NA	12	NA	**NA**	https://www.analog.com/en/resources/analog-dialogue/articles/gigabit-multimedia-serial-link-gmsl-cameras.html
Proprietary Serializer A2	5.2	6	NA	**0.18**	https://www.analog.com/media/en/technical-documentation/data-sheets/max96717.pdf
CSI-802.3ch Bridge	5	5.625	15	**< 0.2**	
Proprietary Serializer B3	NA	4.16	NA	**0.29**	https://www.ti.com/product/DS90UB635-Q1

- OEMs, Tier1s and Tier2s have proven design to accommodate 0.3W serializer power envelope.
- * Typical operating condition. Unclear if power on proprietary serializer datasheet quoted at max reach. Process node may vary between different implementations.

Silicon Measured 802.3ch Link Up Transient

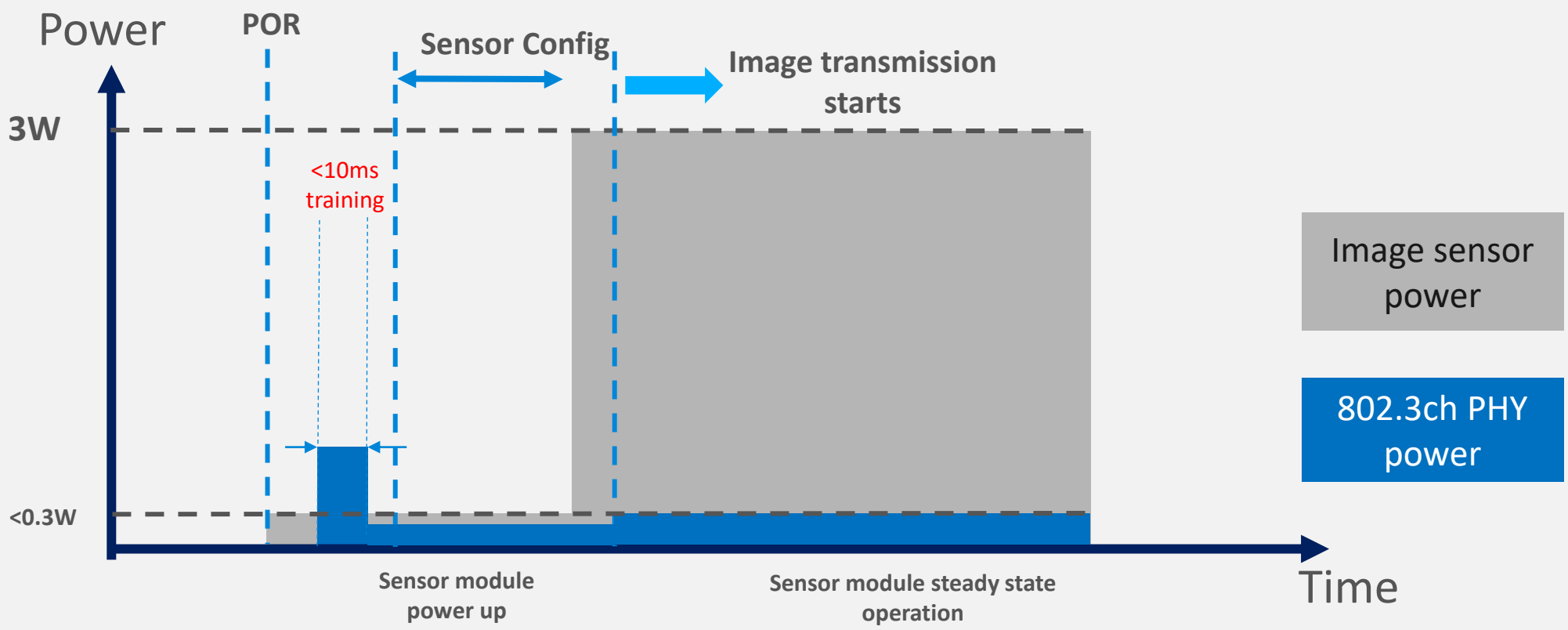
- Standard allocates 97ms
- Silicon measurement shows 802.3ch can link up much (>10X) faster

Measured Silicon link up time, 15m coax, 10Gbps



Camera Module Power Profile with 802.3ch Sensor PHY

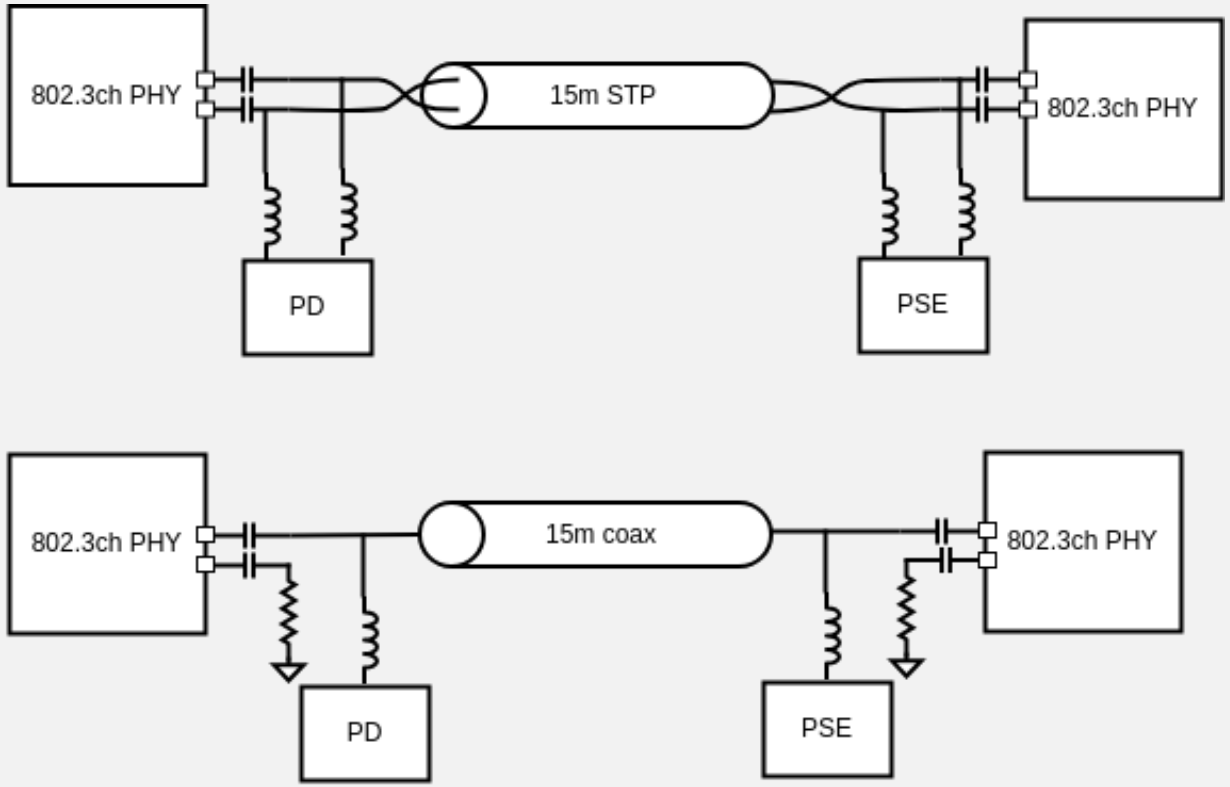
- Typical Camera module power profile vs. time



Coaxial Cable Support

Coax / PoC Support

- "The IEEE 802.3CH specification does not address but also does not prohibit the use of coaxial cables." [Source: https://www.ieee802.org/3/ad_hoc/ngrates/public/23_05/20230516a_DataCollection_PotentialCFI.pdf]
- We would like to evaluate its suitability of 802.3ch PHY on coax medium
- Using coax allows PoC, simplifies power delivery
- Smaller PoC inductors can be used compared to those required by existing FDD SerDes



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Measured 802.3ch PHY STP vs. Coax Link Margin

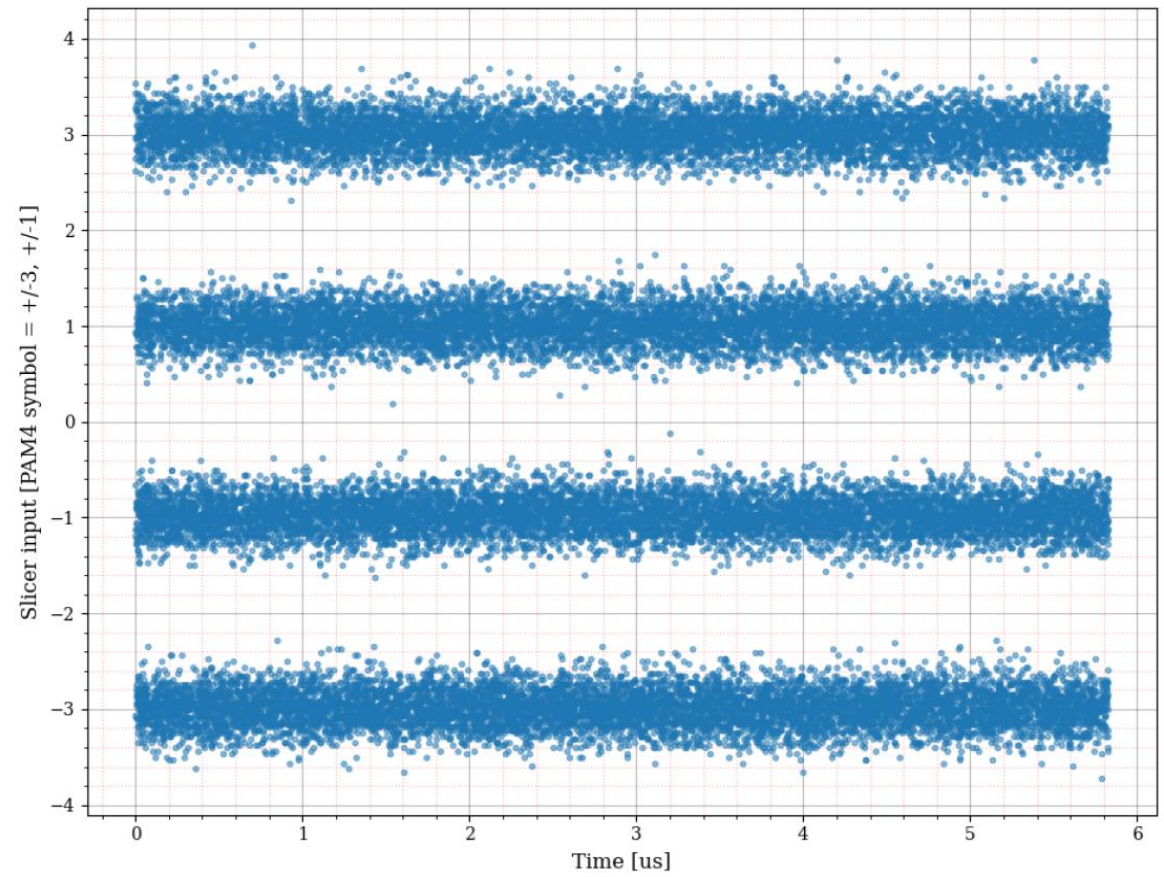
- Preliminary measurement shows 802.3ch PHY can meet link margin requirements on both STP and Coax at 15m reach
  - DP-SNR = Decision Point SNR
  - 17-18dB DP-SNR => meet post-FEC BER requirement of < 1e-12

Cable length	DP-SNR, Coax	DP-SNR, STP
8m	23.5dB	24dB
15m	21.3dB	21.5dB

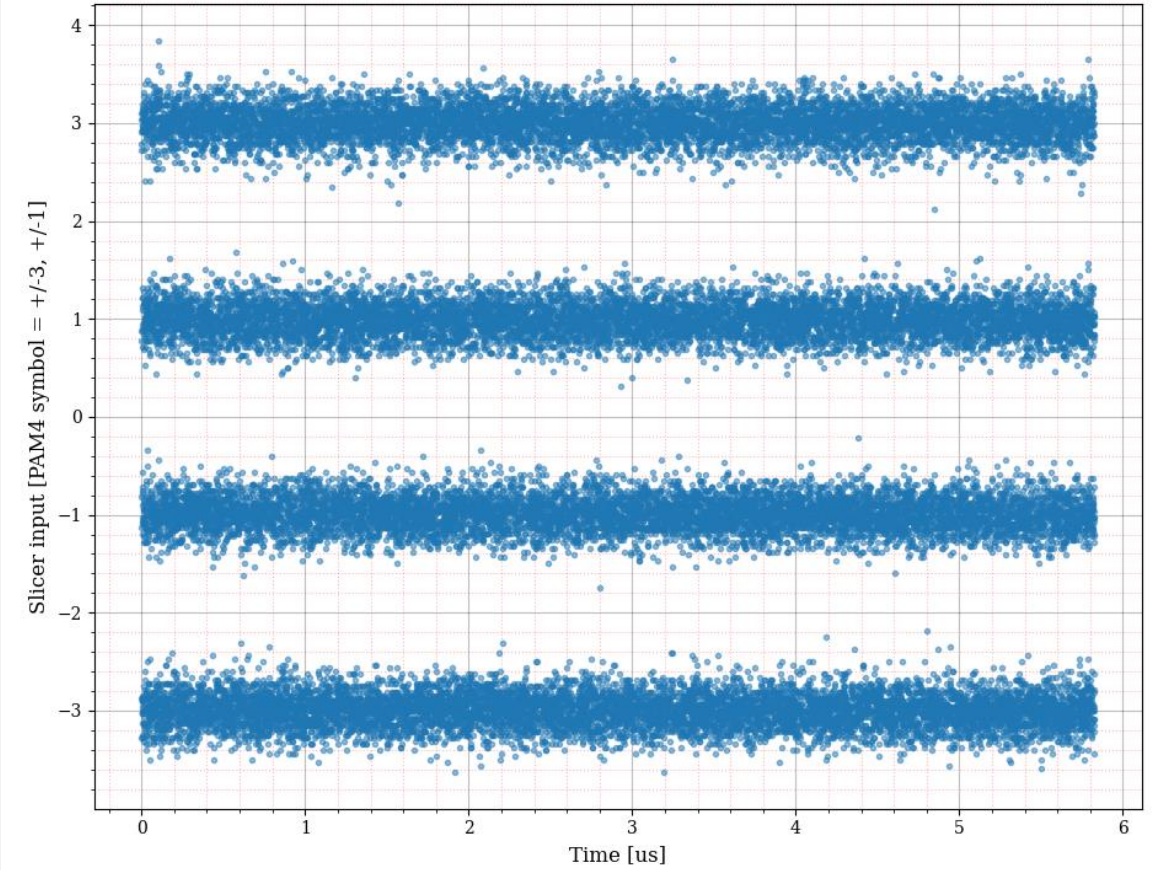
Measured slicer input

- We measure the PAM 4 slicer input in silicon for Coax and STP channel

STP, 15m



Coax, 15m



Conclusion

- 802.3ch PHY can perform well with coax cabling = 15m

Check Against 802.3dm Objectives

#	Objective	802.3ch	Comment
0	Support the IEEE 802.3/Ethernet frame format at the MAC client service interface	☺	
1	Support the minimum and maximum frame size of the current IEEE 802.3 standard	☺	
2	Support operation in automotive environments (e.g., EMC, temperature)	☺	
3	Do not preclude meeting FCC and CISPR EMC requirements	☺	
4	Do not preclude power delivery over balanced and unbalanced link segments	?	Shown to be feasible in silicon with native ch PHY
5	Define optional startup procedure which enables the time from power_on=FALSE to a state capable of transmitting and receiving valid data to be less than 100 ms	☺	

Check Against 802.3dm Objectives continued

#	Objective	802.3ch	Comment
6	Define performance characteristics of link segments suitable for use with automotive balanced-pair cabling and automotive unbalanced coaxial cabling supporting use of up to 4 inline connectors and up to at least 15m reach on at least one type of automotive cabling	?	Shown to be feasible in silicon with native ch PHY
7	Define an electrical PHY to support up to 10 Gbps data rate point-to-point operation in one direction and up to 100 Mbps point-to-point operation in the other direction over the defined balanced-pair link segment.	☺	
8	Define an electrical PHY to support up to 10 Gbps data rate point-to-point operation in one direction and up to 100 Mbps point-to-point operation in the other direction over the defined unbalanced coaxial link segment.	?	Shown to be feasible in silicon with native ch PHY
9	Define an electrical PHY to support up to 5 Gbps data rate point-to-point operation in one direction and up to 100 Mbps point-to-point operation in the other direction over the defined balanced-pair link segment.	☺	

Check Against 802.3dm Objectives continued

#	Objective	802.3ch	Comment
10	Define an electrical PHY to support up to 2.5 Gbps data rate point-to-point operation in one direction and up to 100 Mbps point-to-point operation in the other direction over the defined balanced-pair link segment.	☺	
11	Define an electrical PHY to support up to 2.5 Gbps data rate point-to-point operation in one direction and up to 100 Mbps point-to-point operation in the other direction over the defined unbalanced coaxial link segment.	?	Shown to be feasible in silicon with native ch PHY

Conclusion

- Existing CSI to 802.3ch Bridge chip with EEE mode as sensor PHY can achieve **< 0.2W PHY** power and **< 0.3W** serializer power based on silicon measurement
- Native 802.3ch PHY can support unbalanced coaxial cable operation
- This presentation provides a baseline to evaluate alternate solutions

References

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- https://standards.ieee.org/wp-content/uploads/2023/10/14-realizing-asymmetric-datarates.pdf

Additional references for Asymmetry

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  - https://www.ieee802.org/3/ch/public/jul18/souvignier_3ch_01a_0718.pdf
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