# Assessing Transceiver Complexity and Power for Automotive Imaging Sensors

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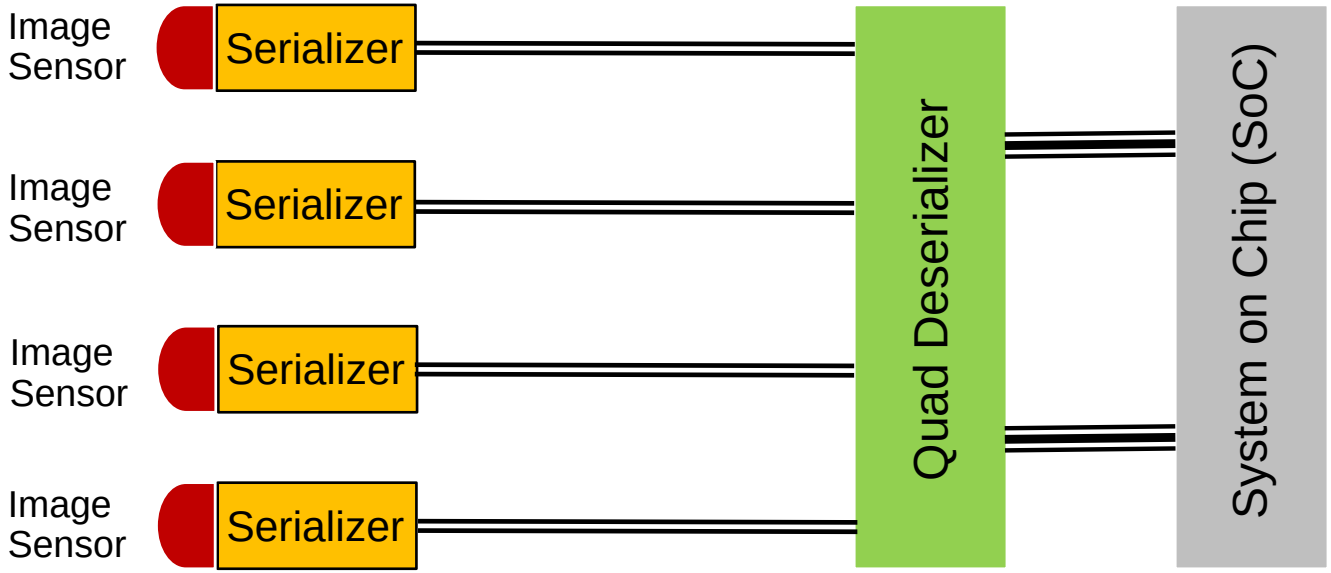
# Foreword

- The main goal of IEEE 802.3dm is to specify an asymmetric physical layer which is optimized for complexity and power for automotive imaging sensor links.
- A typical automotive camera solution includes two major devices; namely a serializer and a deserializer.
- The focus of this presentation is the camera-side transceiver and in particular, the receiver although a serializer ASIC has many other blocks (video interface, multiplexing circuits, PLL).

# Outline

- A typical Automotive Camera Network
- Example of an Existing Product
- Evolution of Multi-gig Wireline SerDes Technology
- 10Gig SerDes Technology; Area and Power Trend
- Link Budget for a 2.5Gbps Camera-side Receiver using SerDes Technology with CTLE+DFE.
- Camera-side Receiver Advantages of a TDD Link versus EEE using ADC/DSP.
- Conclusions

# A Typical Automotive Camera Network




- Serializers are frequency locked to the deserializer.
- All cameras may be initialized (shutter synch) at the same time to allow video combination and generation of a 360 car view.

- Image sensors are connected to individual serializers through a low power video interface.
- Serailizers time multiplex multiple virtual video streams and control signals before sending them to a deserializer. Both serializer and deserializer include buffers and logic interfacing video and control data with the line.
- A quad deserializer receives data, separates video streams and control signals, aggregates video streams and send them to a SoC through a low power interface.

# Examples of the Existing Products for a Serializer & Quad Deserializer

Following data is obtained from datasheet of an automotive SerDes product which is publicly available.

- Forward link of 3 Gbps/6Gbps with 9bit to 10bit encoding and the reverse link of 187.5Mbps (net forward data rate is ~2.5Gbps/5 Gbps)
- Adaptive Equalizer both sides of the link (updated every ~1s)
- Echo cancellation circuit are used on both the serializer and deserializer
- Maximum channel insertion loss of -19.5dB at 1.5GHz for 3Gbps and -21dB at 3GHz for 6Gbps baud rates.
- Cable length up to 20m.

**Power calculated from supply voltages and currents (for 3Gbps deserializer)**

| | Serializer | | Deserializer/Channel | |
|---|---|---|---|---|
| | **Typical** | **Maximum** | **Typical** | **Maximum** |
| Analog Power,1.8V | ~83mW | ~100mW | ~126mW | ~154mW |
| Digital Power, 1.0V | ~98mW | ~234mW | ~56mW | ~177mW |
| Sum | **~181mW** | ~334mW | **~182mW** | ~331mW |

Excluding I/O power

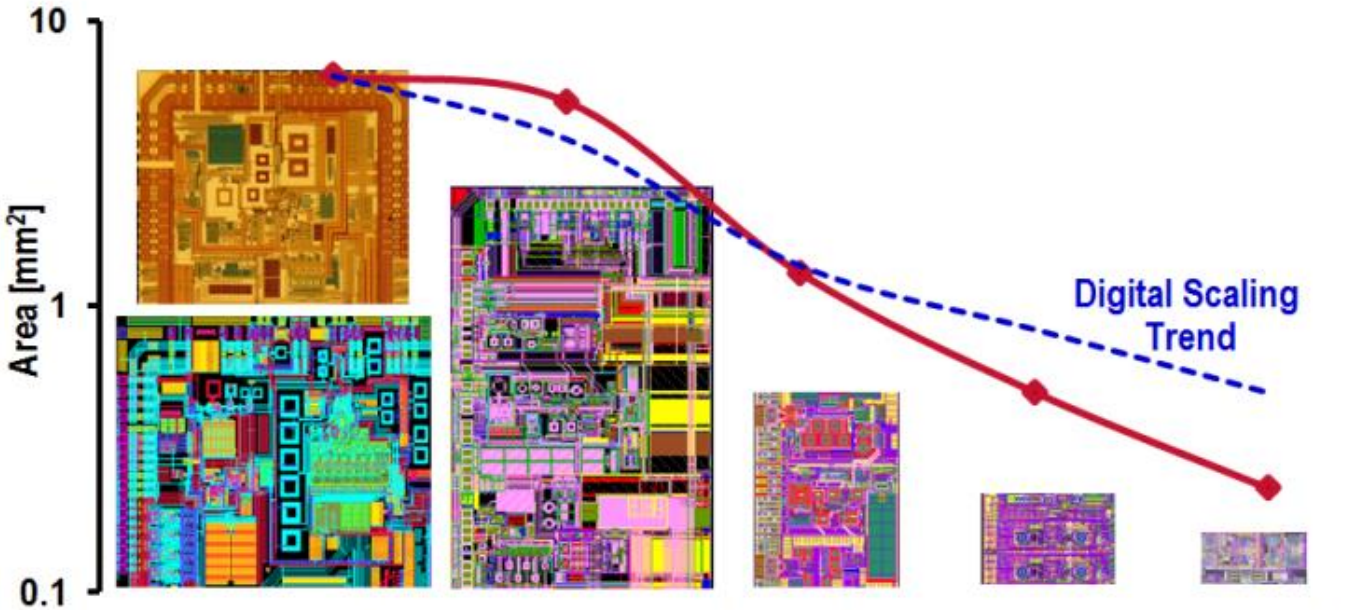
Deserializer takes only ~12mW/ channel more in 6Gbps mode

https://www.analog.com/media/en/technical-documentation/data-sheets/max96717.pdf
https://www.analog.com/media/en/technical-documentation/data-sheets/max96724.pdf

# Evolution of Multi-Gigabit Wireline SERDES Technology

- The wireline SerDes technologies were primarily developed for backplane applications where signals are transmitted and received on separate differential pairs.
- The performance and evolution path of these technologies can shed light on the complexity and power of 802.3dm transceivers.
- Starting from a simple CTLE implementation, SerDes technologies evolved to solutions that include DFE which significantly improved performance. These solutions did not initially use high speed ADCs.
- As the link speed started to go over 25Gbps and then into 50Gbps, ADC/DSP-based solutions were also used. For data rates exceeding 50Gbps on channels with larger than 25dB loss, ADC/DSP-based architecture provides lower power consumption and die area.
- The plot in the next slide shows evolution of 10Gbps SerDes technology.

# 10G SerDes Technology Evolution




| Year | 2000 [ISSCC02] | 2003 | 2010 [ISSCC11] | 2012 | 2013 [VLSI13] |
|---|---|---|---|---|---|
| Tech. | 180 nm | 130 nm | 65 nm | 40 nm | 28 nm |
| Power, Area | 780 mW, 6.4 mm$^2$ | 360 mW, 5.2 mm$^2$ | 150 mW, 1.3 mm$^2$ | 125 mW, 0.5 mm$^2$ | 50 mW, 0.23 mm$^2$ |
| Ch. Loss | 6 dB | 15 dB | 15 dB | 30 dB | 30 dB |

**CTLE+DFE**

- The size and power estimates shown are for the following blocks; **transmitter, PLL and receiver**
- Digital scaling trend may be used to estimate the area and power for 16nm and smaller process nodes.
- DFE is typically implemented in analog signal processing (no ADC, no unrolling)
- The estimates shown here do not apply to ADC/DSP-based implementations

Reference: “Evolution of Multi-Gigabit Wireline Transceivers in CMOS”, Ichiro Fujimori, IEEE CSICS, 2014

# Link Budget Analysis for a 2.5Gbps Receiver (For automotive applications w/coaxial cabling)

- A low complexity receiver using CTLE+DFE equalizer provides a good noise margin for automotive applications with a net bit rate of 2.5Gbps or raw bit rate of 3Gbps.
- Following assumptions and calculations are provided to estimate ingress noise margin:
  1. A 3Gbps receiver has about 5dB lower noise floor than a 10Gbps receiver (10log(3/10)).
  2. A single ended channel has 6dB signal loss as compared to a differential channel.
  3. Consider a TDD solution with no overlap between transmit and receive signals; i.e. no echo cancellation is needed and no headroom for added transmit and receive signaling.
  4. Cross talk is expected to be below receiver noise and negligible for an automotive grade coaxial channel.
  5. Consider an insertion loss of 16dB for a 15m link at 105C and 1.5GHz.

# Link Budget Analysis (Continued)

- If a similar technology as in SerDes (CTLE+DFE) with 30dB IL budget is used for a 3Gbps link, the remaining margin is 30dB - 6dB + 5dB - 16dB = 15dB.
- 15dB net margin covers for ingress noise headroom, baseline wander and a portion of the eye height allocated to the ingress noise.
- Obviously, the margins for a 6Gbps (5Gbps net) link would be lower and does not provide same level of performance in automotive noise environment.
- Although there are mixed mode equalizer solutions available that support higher insertion loss, ADC/DSP-based solutions may also be considered for 5Gbps/10Gbps data rates.
- The solutions based on ADC+DSP allow for adaptive notching which provides a good protection for CW noise types. However, one should always note of short pulse RF noises (3-6 us) that can not be easily rejected.

# Camera Transceiver Advantages as Compared to EEE Implementations Based on ADC+DSP

- Comparing time division duplexing with EEE, up to 95% in DSP area is saved in the camera side of the link.
  - Removing echo canceller saves up to 80% of the DSP area
  - Less than 20% of DSP area is used by equalizer which may be reduced down to about 5% if 2.5Gbps is used instead of 10Gbps in the reverse link.
- During active periods, the DSP power is also reduced by 95%.
- The ADC power and area is reduced by up to 75% if 2.5Gbps is used instead of 10Gbps in the reverse link.
- No significant saving is expected in PLL and transmitter blocks of the transceiver.
- A 2.5Gbps link with periodic LPI could provide a net 100Mbps data rate for a camera bound traffic. The power savings in LPI is evident as the receiver needs to be powered only for 5% of the time.

# Conclusions

- EEE provides power improvement for FDX asymmetric applications. However, further improvement can be attained for complexity and power by avoiding the concurrent transmit and receive, i.e. TDD.
- TDD provides a good solution for higher resolution cameras and image sensor integration. Compared to P802.3ch EEE, up to 95% savings in complexity and power is expected using a ADC/DSP-based solution and even more savings using a CTLE+DFE for equalization.
- Additional complexity and power optimization can be also achieved in BoM cost which is not discussed in this presentation.
- While implementation and complexity (silicon area) of transceivers and in particular camera receiver addressed in this presentation, it is important to consider an overall camera link complexity and power. Optimizing receiver beyond certain points may not make a material difference in overall complexity of a solution.

Thank you for your attention

Questions?