On MDI Return Loss and Power Delivery

Contribution to 802.3dm Task Force

July 15, 2024

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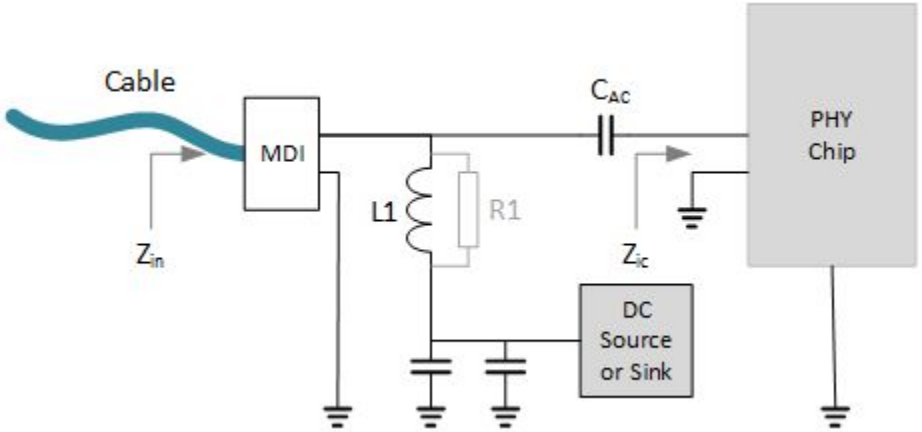
Introduction

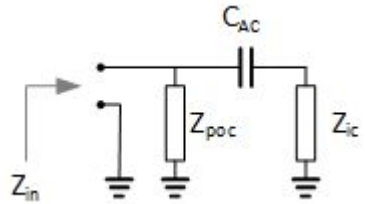
- The 802.3dm development should define MDI Return Loss (RL) limits that are competitive with existing and planned practices
- Specific MDI RL limits are suggested for 802.3dm

MDI RL and PoC

- The PoC circuit is going to impact the return loss at the MDI
- It is very important to control the relative cost of the PoC, so the MDI RL can not be too restrictive
- The diagrams on the right show simplified PCB diagram and simplified MDI impedance models that will be used for reference on the following slides



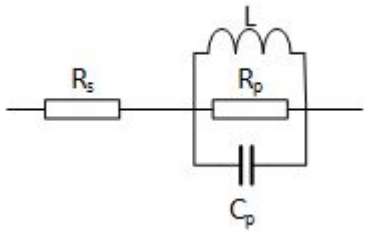
Simplified PCB diagram, including PoC

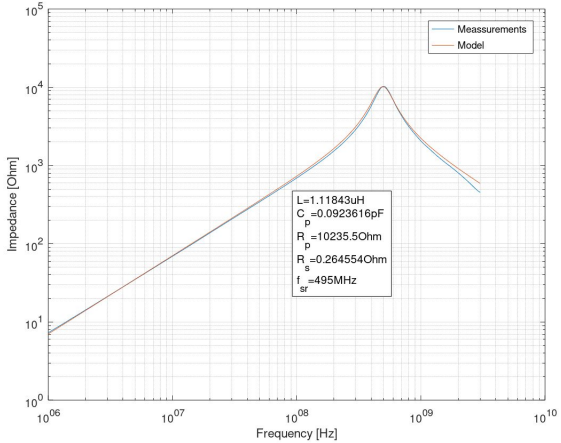


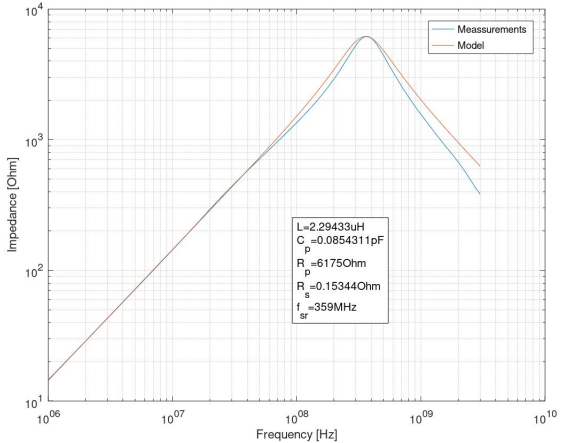
Simplified MDI impedance model

PoC Inductor Parasitic

- Real inductors have parasitic resistance and capacitance that will significantly change the inductor impedance at high frequency
- The circuit diagram below shows a realistic model of real inductors
- The plots on the right shows how this model matches measurements for real inductors:
  - 1.2uH on top
  - 2.2uH on bottom

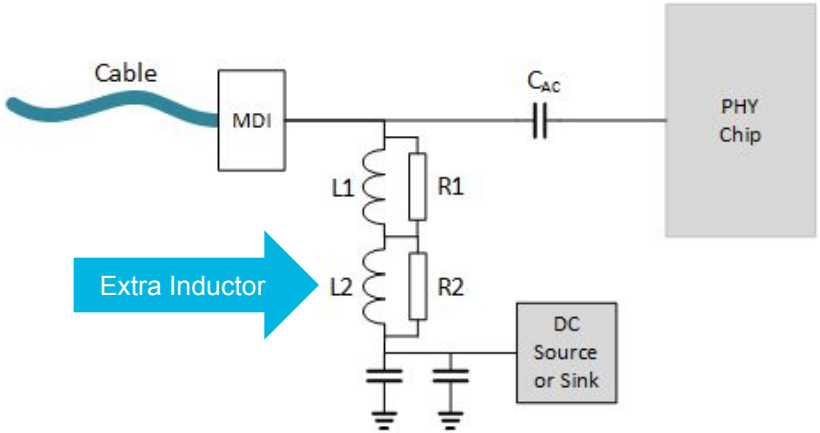






Counteracting Inductor Parasitic

- In some PoC designs, second or third inductors are needed to counteract the inductor parasitics
- This will increase the relative cost of the PHY
- It is important to have the relative cost of the PoC circuitry in mind when defining MDI RL limit



It is important to choose the MDI RL limit such that extra inductors are not needed

Proposed MDI Return Loss Limit for 802.3dm

The proposed MDI Return Loss Limit is

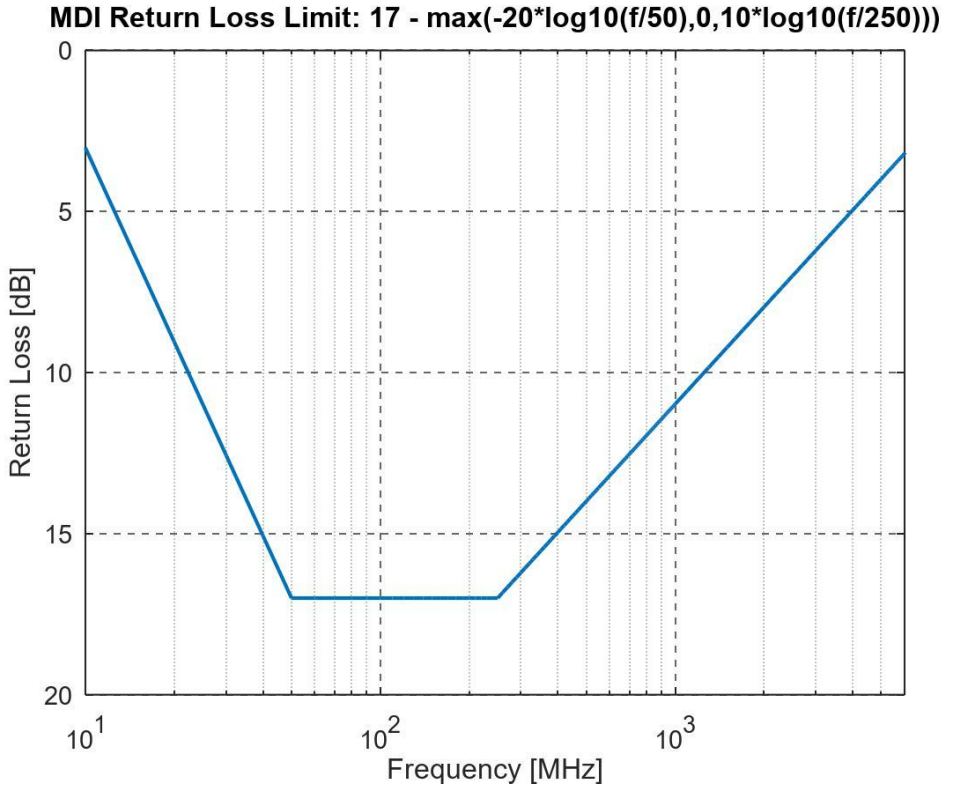
$$RL(f) > \begin{cases} 17+20\log_{10}\left(\frac{f}{50}\right) & f \le 50 \\ 17 & 50 < f \le 250 \\ 17-10\log_{10}\left(\frac{f}{250}\right) & f > 250 \end{cases}$$

where f is in MHz and the limit is defined in the frequency range

10MHz < f < F_{max}

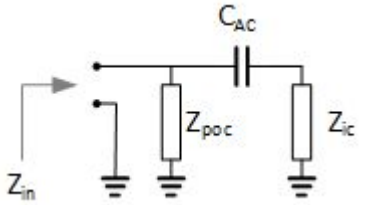
This limit should apply to both coax cables and balanced pairs

NOTE: F_{max} is expected to be few GHz

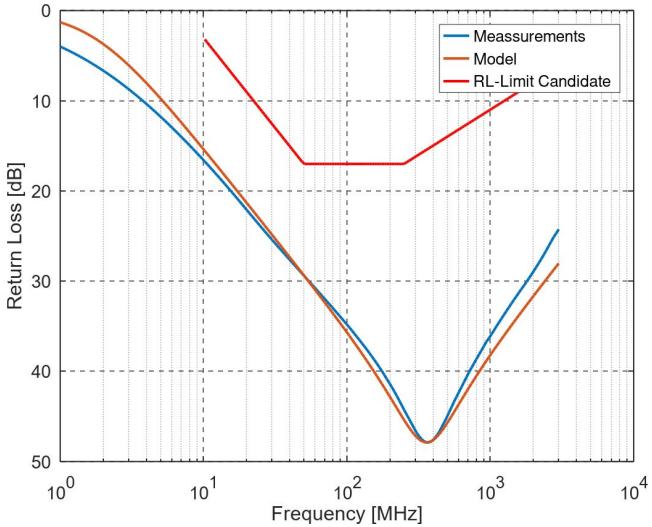


MDI Return Loss vs Simple Inductor Model

- The circuit diagram on top right shows a simplified model of the MDI input impedance
- The plot on the lower right shows return loss for this simplified model, assuming the 2.2uH inductor from previous slide
- The plot demonstrates that single inductor can be used in a PoC circuitry that is compliant with the proposed MDI RL limit



Simplified MDI impedance model

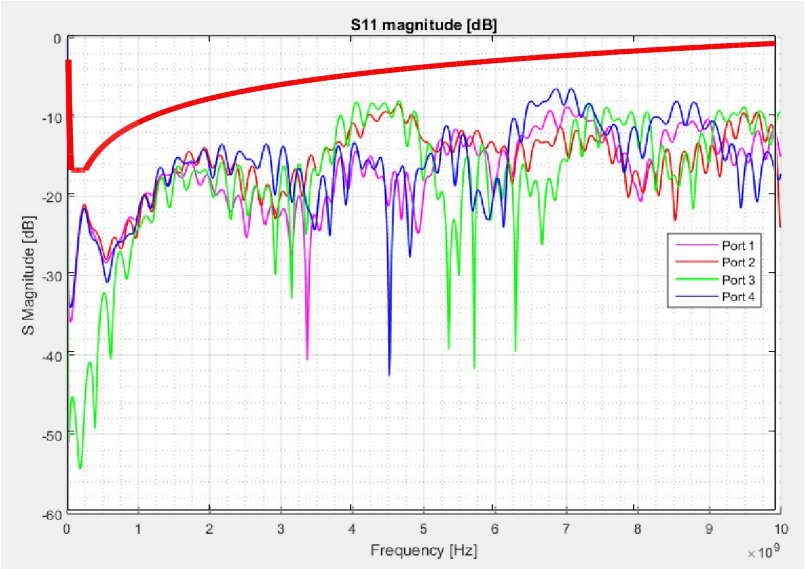


Single inductor PoC can meet the suggested RL limit

MDI Return Loss Limit vs MDI Measurements

Presentation felso_3dm_01_2405.pdf provides Return Loss measurements for PCB boards with single inductor

The plot on the right is taken from Slide 13 of the presentation, with proposed MDI Return Loss Limit overlayed in red



Plot from Slide 13 of https://www.ieee802.org/3/dm/public/0524/felso_3dm_01_2405.pdf

Measured RL from felso_3dm_01_2405.pdf can meet the suggested RL limit

Summary

- Specific MDI Return Loss limit is proposed
- The limits are slightly more relaxed than corresponding RL limits for ASA (see liaison from ASA) and A-PHY (see IEEE 2977-2021)
- The limit was chosen such that it would not introduce too restrictive requirements for the PoC design

Feedback on the proposed RL limits would be greatly appreciated

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