Buffering in an automotive camera communication system

IEEE 802.3dm

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Motivation

- Page 16 of https://www.ieee802.org/3/dm/public/0524/sedarat_3dm_02_202405.pdf gives the impression that a TDD system is at a significant disadvantage in respect to latency and FIFO when compared with an FDD or an FDD/CM system.

- On page 12 of https://www.ieee802.org/3/ISAAC/public/091423/Lo_01_0923.pdf a buffer placement chart gives a similar impression.

- This presentation looks at the complete buffer situation from an automotive camera system perspective for various duplexing schemes.

- It shows that the buffering situation in an automotive camera application is dominated by the buffering requirements primarily driven by the application and second from MAC. While there are some differences in PHY related buffering, with FDD potentially involving smaller buffers, the overall impact of the various duplexing schemes is relatively small.

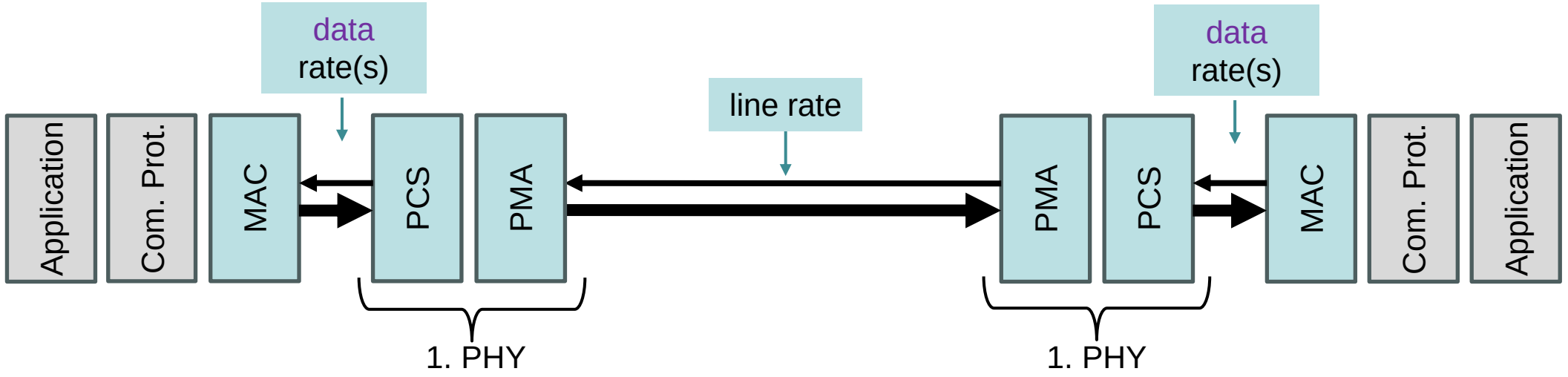
Content

- System overview

- Buffer aspects to consider
  1. PHY and PHY duplexing related buffering
  2. MAC and other layer 2 buffering
  3. Buffering from camera application (informative)

- Summary and conclusion

System overview



2. MAC requires the complete Ethernet packet in order to generate/evaluate the CRC

3. Application related buffering, not part of IEEE 802.3 specifications, therefore informative

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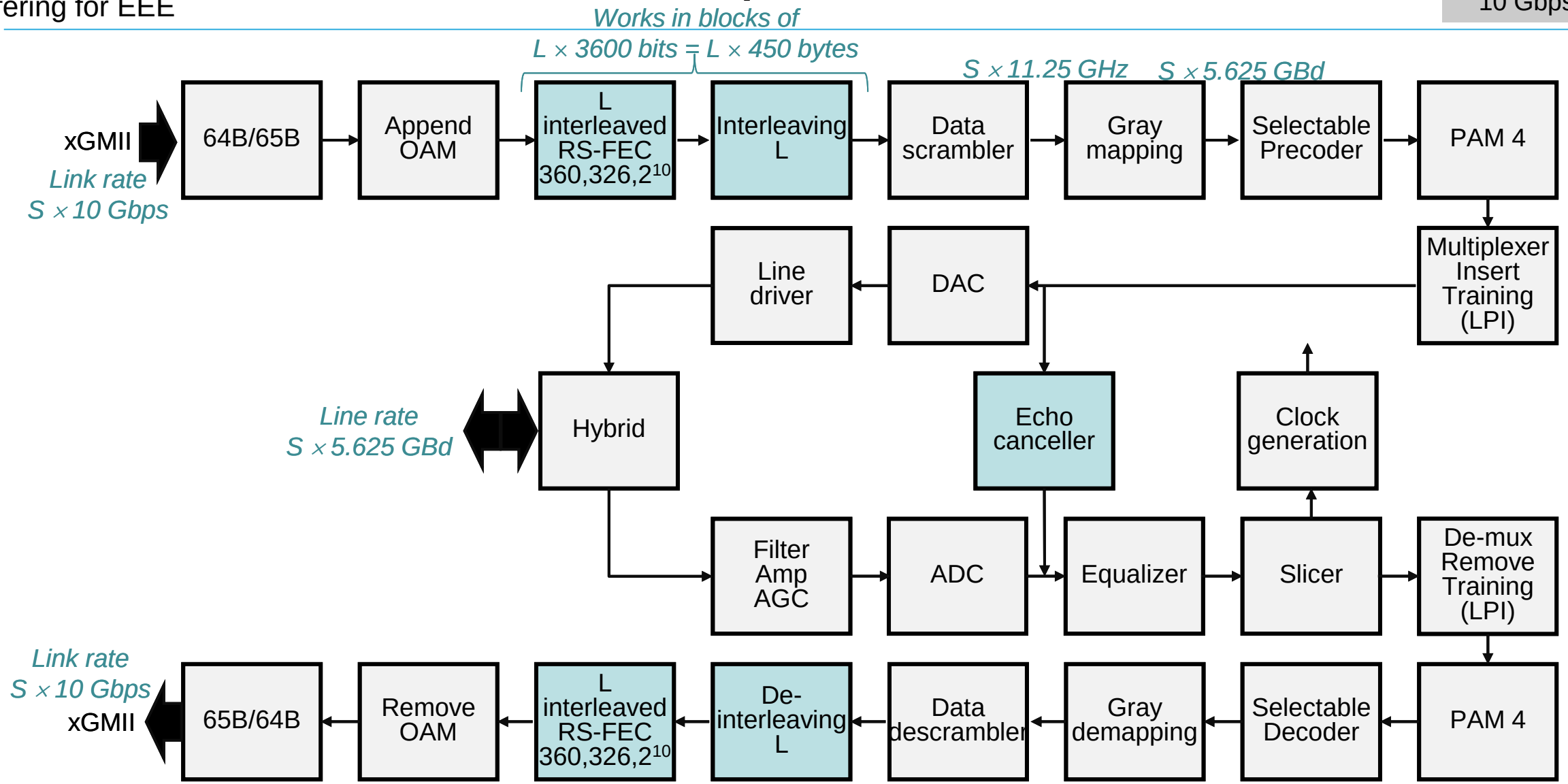
Link rate	S
2.5 Gbps	0.25
5 Gbps	0.5
10 Gbps	1

Requires buffering

Not included:
Buffering for EEE

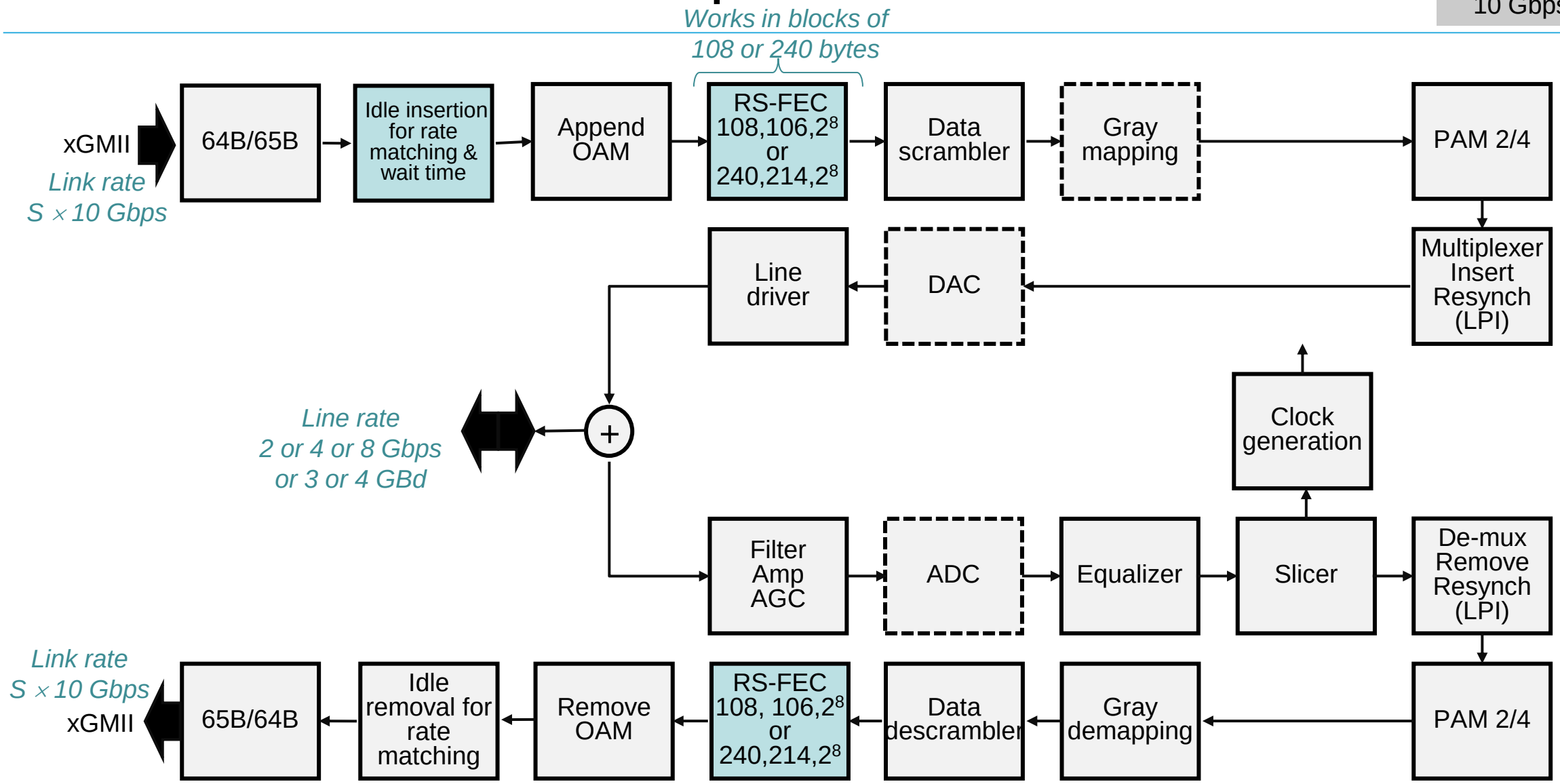
PHY example for 802.3ch



Link rate	S
2.5 Gbps	0.25
5 Gbps	0.5
10 Gbps	1

Requires buffering

PHY example for ASA-MLE



Some general observations for FDD

- Currently, there is no FDD Ethernet PHY. Therefore, the following makes certain assumptions for the purpose of analysis.
- The DS transceiver (camera-side) differs significantly from the US transceiver (ECU-side) and the therefore, the two have to be considered separately.
- For an FDD system, transceivers transmit and receive at the same time. Higher overlap in DS and US frequencies results in stronger need for echo cancellation. As an example, for DS 2.5Gbps with PAM4 and US 100 Mbps echo cancellation requirements are more stringent than for 10 Gbps with PAM 4, which in turn is more complex than10 Gbps with PAM 2.
- The DS transmitter and DS receiver will likely need buffering for an FEC or other ways of error mitigation. The US transmitter and US receiver might not define an FEC.
- The DS receiver will likely need an echo canceller with buffering, as the high-speed receiver is more susceptible and as an echo canceller improves the SNR. The US receiver might only need a light echo canceller or live with performance reduction/less margin, with respectively small buffering needs.

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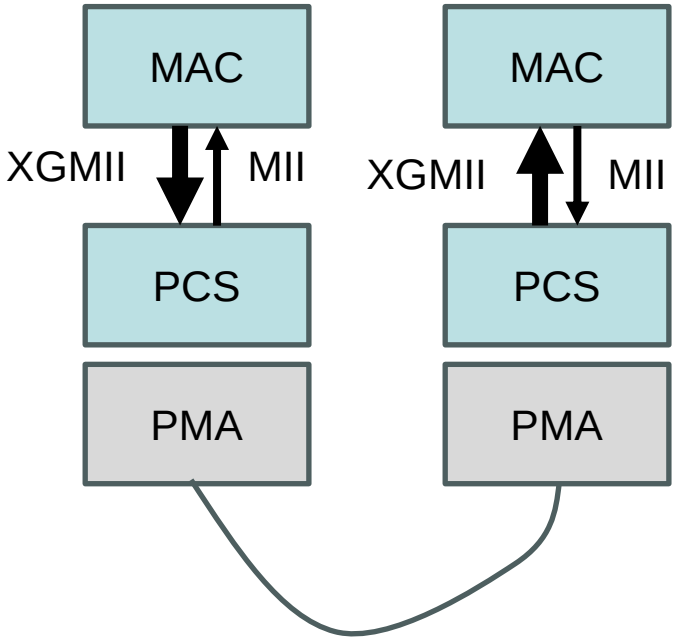
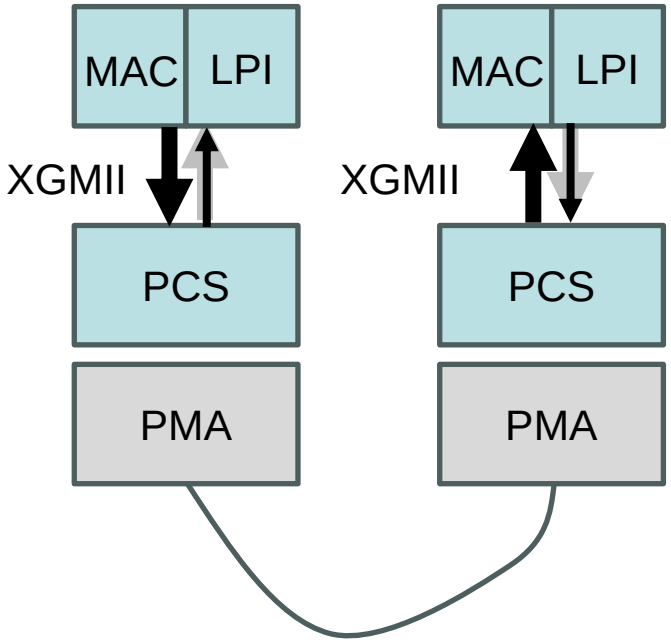
Options for MAC interface with asymmetric rates

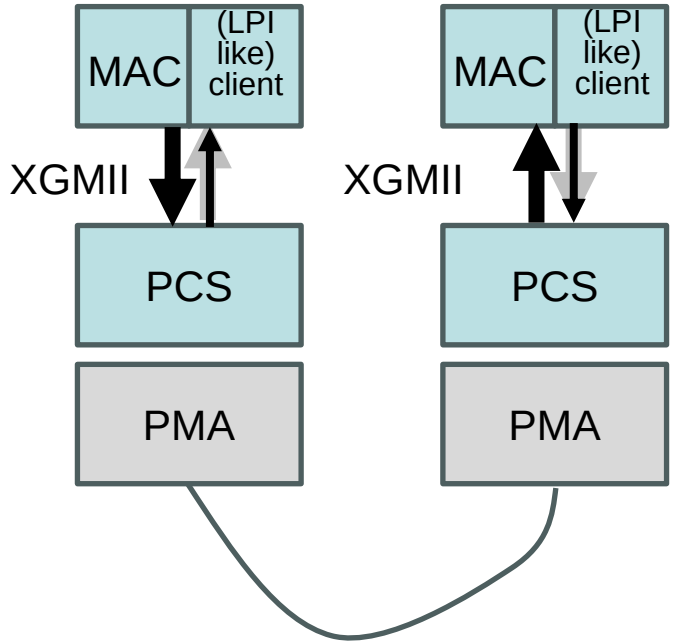
FDD or TDD (Option A)



FDX/EEE



FDD or TDD (Option B)



In https://www.ieee802.org/3/ISAAC/public/091423/Lo_01_0923.pdf it is stated that it is preferable to put any EEE/LPI related buffering in the PHY (between PCS and PMA). However, that seems to be an implementation choice. Logically, it is the MAC that holds back data in case of LPI (and this presentation therefore associates the respective buffers to the MAC).

Relevant layer 1 and 2 buffering for different PHY types

		MAC (camera)	PCS (camera)	PMA (camera)	PMA (ECU)	PCS (ECU)	MAC (ECU side)
FDX/ EEE (802.3ch)	DS	Normal MAC buffers (esp. pause), wake time buffers for min 9 us @ high rate	FEC	None	None	FEC, echo canceller	Smaller MAC buffers (application congestion)
	US	Smaller MAC buffers (application congestion)	FEC, echo canceller	None	None	FEC	Normal MAC buffers (esp. pause), wake time buffers for min 9 us @ high rate
TDD (ASA-MLE)	DS	Normal MAC buffers (esp. pause)	FEC, wait time buffers for <1 us @ high rate	None	None	FEC	Smaller MAC buffers (application congestion)
	US	Smaller MAC buffers (application congestion)	FEC	None	None	FEC, wait time buffers for <27 us @ low rate	Normal MAC buffers (esp. pause)
FDD	DS	Normal MAC buffers (esp. pause)	FEC	None	None	FEC, echo canceller likely	Smaller MAC buffers (application congestion)
	US	Smaller MAC buffers (application congestion)	None likely	None	None	None likely	Normal MAC buffers (esp. pause)

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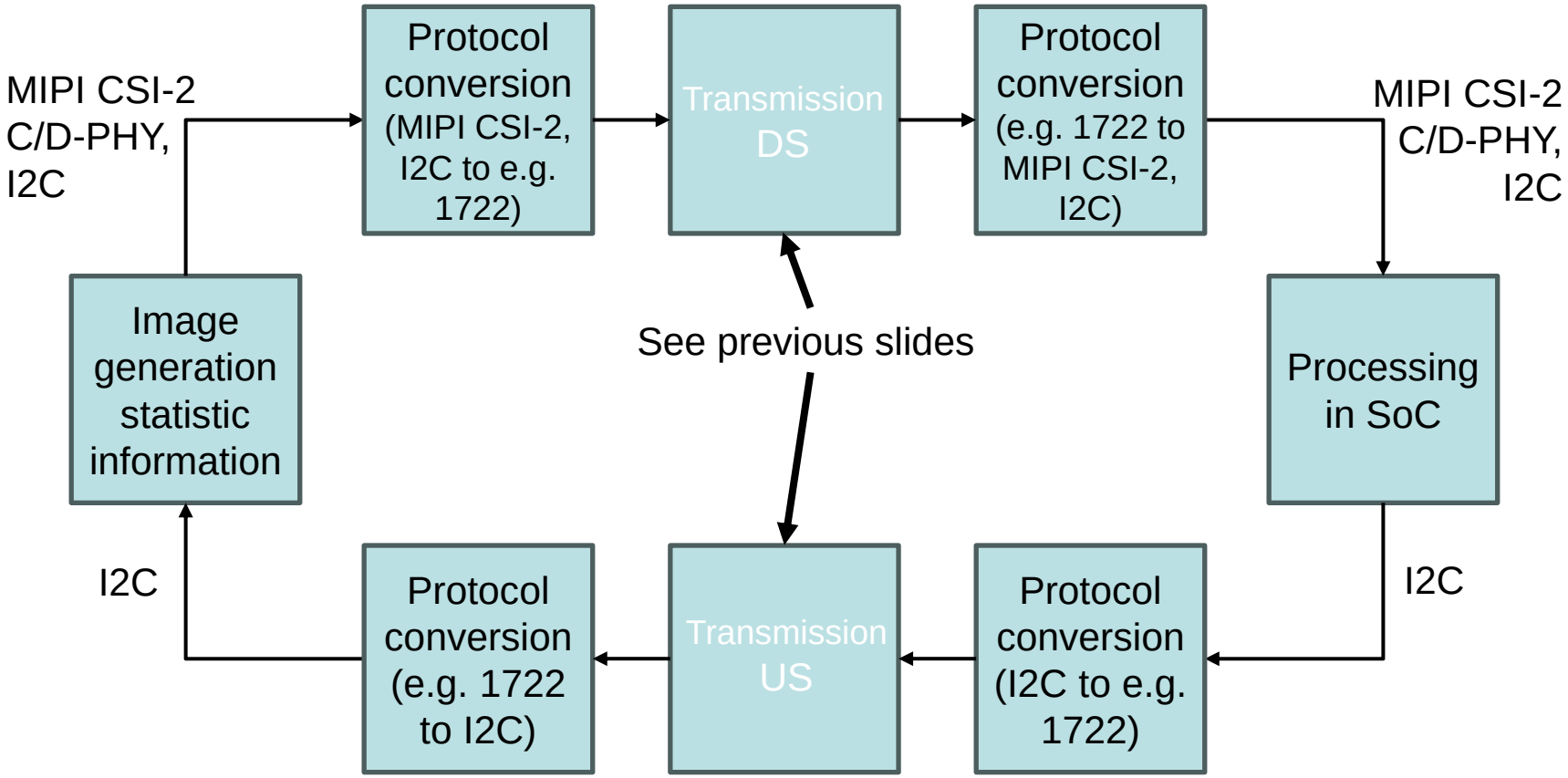
Buffers needed in typical camera communication

In the camera to SoC communication system, buffers are needed four times for protocol conversion. Video buffers (including the virtual channels) for require significant capacity.



Overview

Buffer Related to…	TDD (ASA-MLE)	FDD (anticipated)	FDX/EEE (802..3ch)
MIPI CSI-2 bridging and video	Large in comparison	Large in comparison	Large in comparison
DS MAC (esp. pause, appl. congestion)*)	Medium size buffers	Medium size buffers	Medium size buffers + added buffers for EEE
US MAC (esp. pause, appl. congestion)*)	Medium size buffers	Medium size buffers	Medium size buffers + added buffers for EEE
DS PHY	Small buffers in comparison (despite wait times)	Small buffers	Small buffers
US PHY	Small buffers in comparison (despite wait times)	Negligible	Small buffers

*) Layer 2 may have additional buffers in case of MACsec, PTP, etc.

Summary and conclusion

- This presentation looks at buffer requirements in typical automotive camera systems, including the duplexing schemes for the physical layer.
- A typical bridge chip inside the camera module (whether integrated with the imager or not) may be optimized for the specific rates and use cases. However, it will still include MAC and application related buffers.
- Main buffers result from the application requirements, especially virtual channels.
- MAC needs buffer for mitigating the effects of congestion/MAC layer pause as well as EEE (plus buffers for MACsec and other layer 2 protocols). This is a medium effort.
- The main items for buffering inside the PHY are FEC and echo cancellation. For TDD, the PHY does not need echo cancellation, but uses a buffer for wait times. These buffers are smaller, when compared with the MAC and application related buffers.

Thank You!