45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the reserved row for 1.77 through 1.79 in Table 45-3 (as modified by IEEE Std 802.3cz-2023, IEEE Std 802.3df-2024, and IEEE Std 802.3dj-20xx) as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.77	Asymmetrical BASE-T1/V1 PMA/PMD extended ability	45.2.1.60f
1.~~77~~78 through 1.79	Reserved	
…		

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Insert new rows in Table 45-9 immediately after row for 2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1 as follows *(unchanged rows not shown):*

Table 45–9—Transmit fault description location

PMA/PMD	Description location
…	
2.5G+100MBASE-T1, 5G+100MBASE-T1, 10G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-V1, 10G+100MBASE-V1	149.4.2.2
100M+2.5GMBASE-T1, 100M+5GBASE-T1, 100M+10GBASE-T1, 100M+2.5GBASE-V1, 100M+5GMBASE-V1, 100M+10GBASE-V1	200.7.2.2
…	

45.2.1.7.5 Receive fault (1.8.10)

Insert new rows in Table 45-10 immediately after row for 2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1 as follows *(unchanged rows not shown):*

Table 45–10—Receive fault description location

PMA/PMD	Description location
…	
2.5G+100MBASE-T1, 5G+100MBASE-T1, 10G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-V1, 10G+100MBASE-V1	149.4.2.3
100M+2.5GMBASE-T1, 100M+5GBASE-T1, 100M+10GBASE-T1, 100M+2.5GBASE-V1, 100M+5GMBASE-V1, 100M+10GBASE-V1	200.7.2.3
…	

Insert 45.2.1.60f after 45.2.1.60e (as inserted by IEEE Std 802.3df-202x) as follows:

45.2.1.60f Asymmetric BASE-T1/V1 PMA/PMD extended ability register (Register 1.77)

The assignment of bits in the Asymmetrical BASE-T1/V1 PMA/PMD extended ability register is shown in Table 45–58f.

Table 45–58f—Asymmetric BASE-T1/V1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.77.15:12	Reserved	Value always 0	RO
1.77.11	10G+100MBASE-V1 ability	1 = PMA/PMD is able to perform 10G+100MBASE-V1 0 = PMA/PMD is not able to perform 10G+100MBASE-V1	RO
1.77.10	100M+10GBASE-V1 ability	1 = PMA/PMD is able to perform 100M+10GBASE-V1 0 = PMA/PMD is not able to perform 100M+10GBASE-V1	RO
1.77.9	10G+100MBASE-T1 ability	1 = PMA/PMD is able to perform 10G+100MBASE-T1 0 = PMA/PMD is not able to perform 10G+100MBASE-T1/V1	RO
1.77.8	100M+10GBASE-T1 ability	1 = PMA/PMD is able to perform 100M+10GBASE-T1 0 = PMA/PMD is not able to perform 100M+10GBASE-T1	RO
1.77.7	5G+100MBASE-V1 ability	1 = PMA/PMD is able to perform 5G+100MBASE-V1 0 = PMA/PMD is not able to perform 5G+100MBASE-V1	RO
1.77.6	100M+5GBASE-V1 ability	1 = PMA/PMD is able to perform 100M+5GBASE-V1 0 = PMA/PMD is not able to perform 100M+5GBASE-V1	RO
1.77.5	5G+100MBASE-T1 ability	1 = PMA/PMD is able to perform 5G+100MBASE-T1 0 = PMA/PMD is not able to perform 5G+100MBASE-T1	RO
1.77.4	100M+5GBASE-T1 ability	1 = PMA/PMD is able to perform 100M+5GBASE-T1 0 = PMA/PMD is not able to perform 100M+5GBASE-T1	RO

Table 45–58f—Asymmetric BASE-T1/V1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.77.3	2.5G+100MBASE-V1 ability	1 = PMA/PMD is able to perform 2.5G+100MBASE-V1 0 = PMA/PMD is not able to perform 2.5G+100MBASE-V1	RO
1.77.2	100M+2.5GBASE-V1 ability	1 = PMA/PMD is able to perform 100M+2.5GBASE-V1 0 = PMA/PMD is not able to perform 100M+2.5GBASE-V1	RO
1.77.1	2.5G+100MBASE-T1 ability	1 = PMA/PMD is able to perform 2.5G+100MBASE-T1 0 = PMA/PMD is not able to perform 2.5G+100MBASE-T1	RO
1.77.0	100M+2.5GBASE-T1 ability	1 = PMA/PMD is able to perform 100M+2.5GBASE-T1 0 = PMA/PMD is not able to perform 100M+2.5GBASE-T1	RO

[a]R/W = Read/Write, RO = Read only

45.2.1.60f.1 10G+100MBASE-V1 (1.77.11)

When read as a one, bit 1.77.11 indicates that the PMA/PMD is able to operate as a 10G+100MBASE-V1 PMA type.

When read as a zero, bit 1.77.11 indicates that the PMA/PMD is not able to operate as a 10G+100MBASE-V1 PMA type.

45.2.1.60f.2 100M+10GBASE-T1/V1 (1.77.10)

When read as a one, bit 1.77.10 indicates that the PMA/PMD is able to operate as a 100M+10GBASE-V1 PMA type.

When read as a zero, bit 1.77.10 indicates that the PMA/PMD is not able to operate as a 100M+10GBASE-V1 PMA type.

45.2.1.60f.3 10G+100MBASE-T1 (1.77.9)

When read as a one, bit 1.77.9 indicates that the PMA/PMD is able to operate as a 10G+100MBASE-T1 PMA type.

When read as a zero, bit 1.77.9 indicates that the PMA/PMD is not able to operate as a 10G+100MBASE-T1 PMA type.

45.2.1.60f.4 100M+10GBASE-T1 (1.77.8)

When read as a one, bit 1.77.8 indicates that the PMA/PMD is able to operate as a 100M+10GBASE-T1 PMA type.

When read as a zero, bit 1.77.8 indicates that the PMA/PMD is not able to operate as a 100M+10GBASE-T1 PMA type.

45.2.1.60f.5 5G+100MBASE-V1 (1.77.7)

When read as a one, bit 1.77.7 indicates that the PMA/PMD is able to operate as a 5G+100MBASE-V1 PMA type.

When read as a zero, bit 1.77.7 indicates that the PMA/PMD is not able to operate as a 5G+100MBASE-V1 PMA type.

45.2.1.60f.6 100M+5GBASE-V1 (1.77.6)

When read as a one, bit 1.77.6 indicates that the PMA/PMD is able to operate as a 100M+5GBASE-V1 PMA type.

When read as a zero, bit 1.77.6 indicates that the PMA/PMD is not able to operate as a 100M+5GBASE-V1 PMA type.

45.2.1.60f.7 5G+100MBASE-T1 (1.77.5)

When read as a one, bit 1.77.5 indicates that the PMA/PMD is able to operate as a 5G+100MBASE-T1 PMA type.

When read as a zero, bit 1.77.5 indicates that the PMA/PMD is not able to operate as a 5G+100MBASE-T1 PMA type.

45.2.1.60f.8 100M+5GBASE-T1 (1.77.4)

When read as a one, bit 1.77.4 indicates that the PMA/PMD is able to operate as a 100M+5GBASE-T1 PMA type.

When read as a zero, bit 1.77.4 indicates that the PMA/PMD is not able to operate as a 100M+5GBASE-T1 PMA type.

45.2.1.60f.9 2.5G+100MBASE-V1 (1.77.3)

When read as a one, bit 1.77.3 indicates that the PMA/PMD is able to operate as a 2.5G+100MBASE-V1 PMA type.

When read as a zero, bit 1.77.3 indicates that the PMA/PMD is not able to operate as a 2.5G+100MBASE-V1 PMA type.

45.2.1.60f.10 100M+2.5GBASE-V1 (1.77.2)

When read as a one, bit 1.77.2 indicates that the PMA/PMD is able to operate as a 100M+2.5GBASE-V1 PMA type.

When read as a zero, bit 1.77.2 indicates that the PMA/PMD is not able to operate as a 100M+2.5GBASE-V1 PMA type.

45.2.1.60f.11 2.5G+100MBASE-T1 (1.77.1)

When read as a one, bit 1.77.1 indicates that the PMA/PMD is able to operate as a 2.5G+100MBASE-T1 PMA type.

When read as a zero, bit 1.77.1 indicates that the PMA/PMD is not able to operate as a 2.5G+100MBASE-T1 PMA type.

45.2.1.60f.12 100M+2.5GBASE-T1 (1.77.0)

When read as a one, bit 1.77.0 indicates that the PMA/PMD is able to operate as a 100M+2.5GBASE-T1 PMA type.

When read as a zero, bit 1.77.0 indicates that the PMA/PMD is not able to operate as a 100M+2.5GBASE-T1 PMA type.

45.2.1.214 BASE-T1 PMA/PMD control register (Register 1.2100)

Replace the rows for bits 1.2100.13:4 and 1.2100.3:0 in Table 45–178 (as modified by IEEE Std 802.3cy-2023 and IEEE Std 802.3da-202x) as follows (unchanged rows not shown):

Table 45–178—BASE-T1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.2100.13:5	Reserved	Value always 0	RO
1.2100.4:0	Type Selection	4 3 2 1 0 1 1 1 x x= Reserved 1 1 0 1 1 = 10G+100MBASE-V1 1 1 0 1 0 = 100M+10GBASE-V1 1 1 0 0 1 = 10G+100MBASE-T1 1 1 0 0 0 = 100M+10GBASE-T1 1 0 1 1 1 = 5G+100MBASE-V1 1 0 1 1 0 = 100M+5GBASE-V1 1 0 1 0 1 = 5G+100MBASE-T1 1 0 1 0 0 = 100M+5GBASE-T1 1 0 0 1 1 = 2.5G+100MBASE-V1 1 0 0 1 0 = 100M+2.5GBASE-V1 1 0 0 0 1 = 2.5G+100MBASE-T1 1 0 0 0 0 = 100M+2.5GBASE-T1 0 1 1 x x = Reserved 0 1 0 1 x = Reserved 0 1 0 0 1 = Reserved 0 1 0 0 0 = 10BASE-T1M 0 0 1 1 1 = 25GBASE-T1 0 0 1 1 0 = 10GBASE-T1 0 0 1 0 1 = 5GBASE-T1 0 0 1 0 0 = 2.5GBASE-T1 0 0 0 1 1 = 10BASE-T1S 0 0 0 1 0 = 10BASE-T1L 0 0 0 0 1 = 1000BASE-T1 0 0 0 0 0 = 100BASE-T1	R/W

[a]R/W = Read/Write, RO = Read only

Change the subclause title and first sentence of 45.2.1.214.2 (as modified by IEEE Std 802.3da-202x) as follows:

45.2.1.214.2 Type selection (1.2100.4:0) ~~(1.2100.3:0)~~

Bits 1.2100.4:0 ~~1.2100.3:0~~ are used to set the mode of operation when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented.