Insert new clauses and corresponding annexes as follows:

200. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1

This is a draft proposal for how a Clause could be structured based on the P802.3dm project documents, including Objectives. This provides flexibility to have different requirements for the different speeds and cabling. Subclauses can be combined later if the requirements are the same, or the requirement can be put in the first subclause in the document and the one later in the document can refer back to it.
Due to the fact that we are limited to a maximum of five levels in the specification, the high speed and low speed requirements are in separate subclauses without a subsection above the pair. This is also the case for the coax and shielded balanced copper cabling.

200.1 Overview

May be added by Editor based on project details.

200.1.1 Nomenclature

May be added by Editor based on project details.
In order to efficiently describe the three PHYs, the nomenclature MultiG is used to abbreviate 2.5G/5G/10G when referring to the set of PHYs.
Upstream(US) is used to refer to the 100M transmitter.
Downstream (DS) is used to refer to the MulitG transmitter.

The 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1 PHYs described in this clause represent 12 distinct PHY types that share the same PCS and PMA(?) (and MDI) specifications subject to frequency scaling. In order to efficiently describe the 12 PHYs, the following nomenclature is used.

When talking about the high speed path, regardless of speed or cable type, (i.e. MultiG+100MBASE-T1/V1 transmit path to 100M+MultiGBASE-T1/V1 receive path) use:

DS_TX

When talking about the low speed path, regardless of speed or cable type, (i.e. 100M+MultiGBASE-T1/V1 transmit path to MultiG+100MBASE-T1/V1 receive path) use:

US_TX

When talking about all PHYs communicating on shielded, balanced, pair of conductors, regardless of transmit speed, use:

MultiG+100M/100M+MultiGBASE-T1

When talking about all PHYs communicating on coaxial cable, regardless of transmit speed, use:

MultiG+100M/100M+MultiGBASE-V1

When talking about all PHYs, regardless of transmit speed or cable type, use:

MultiG+100M/100M+MultiGBASE-T1/V1

Additionally, for parameters that scale with the PHY's data rate, the parameter *S* is used for scaling, see Table 200–1. The value of S specified in Clause 200, Table 200–1, shall be used for all references to Clause 149 subclauses.

Table 200–1—Scaling parameter

PHY type	*S*
10G+100MBASE-T1/V1	1
5G+100MBASE-T1/V1	1
2.5G+100MBASE-T1/V1	0.5

200.1.2 PHY/PMD types

I have included a table here to show the different PHYs to be defined and what all the characters that I am using in the names mean. These are subject to approval.
x+y x is the transmit speed, y is the receive speed
T1 - single shielded balanced pair of conductors (SBP)
V1 - single coaxial cable (Coax)

Table 200–2—PHY/PMD type definitions

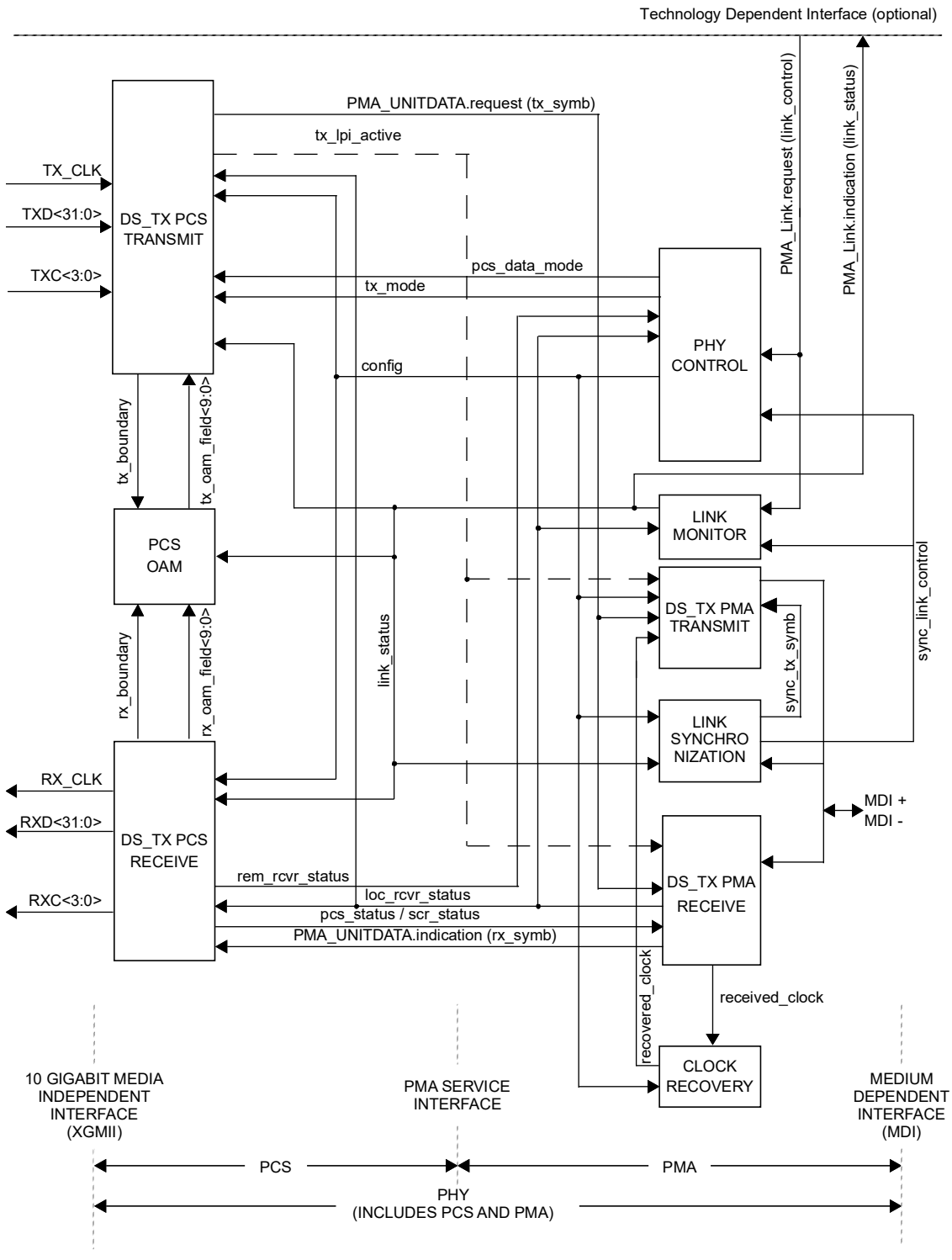
PHY name	Transmit speed	Receive speed	Cable Type
100M+2.5GBASE-T1	100M	2.5G	SBP
2.5G+100MBASE-T1	2.5G	100M	SBP
100M+5GBASE-T1	100M	5G	SBP
5G+100MBASE-T1	5G	100M	SBP
100M+10GBASE-T1	100M	10G	SBP
10G+100MBASE-T1	10G	100M	SBP
100M+2.5GBASE-V1	100M	2.5G	Coax
2.5G+100MBASE-V1	2.5G	100M	Coax
100M+5GBASE-V1	100M	5G	Coax
5G+100MBASE-V1	5G	100M	Coax
100M+10GBASE-V1	100M	10G	Coax
10G+100MBASE-V1	10G	100M	Coax

200.1.3 Relationship of MultiG+100M/100M+MultiGBASE-T1/V1 to other standards

May be added by Editor based on project details.

200.1.4 Operation of MultiG+100M/100M+MultiGBASE-T1/V1

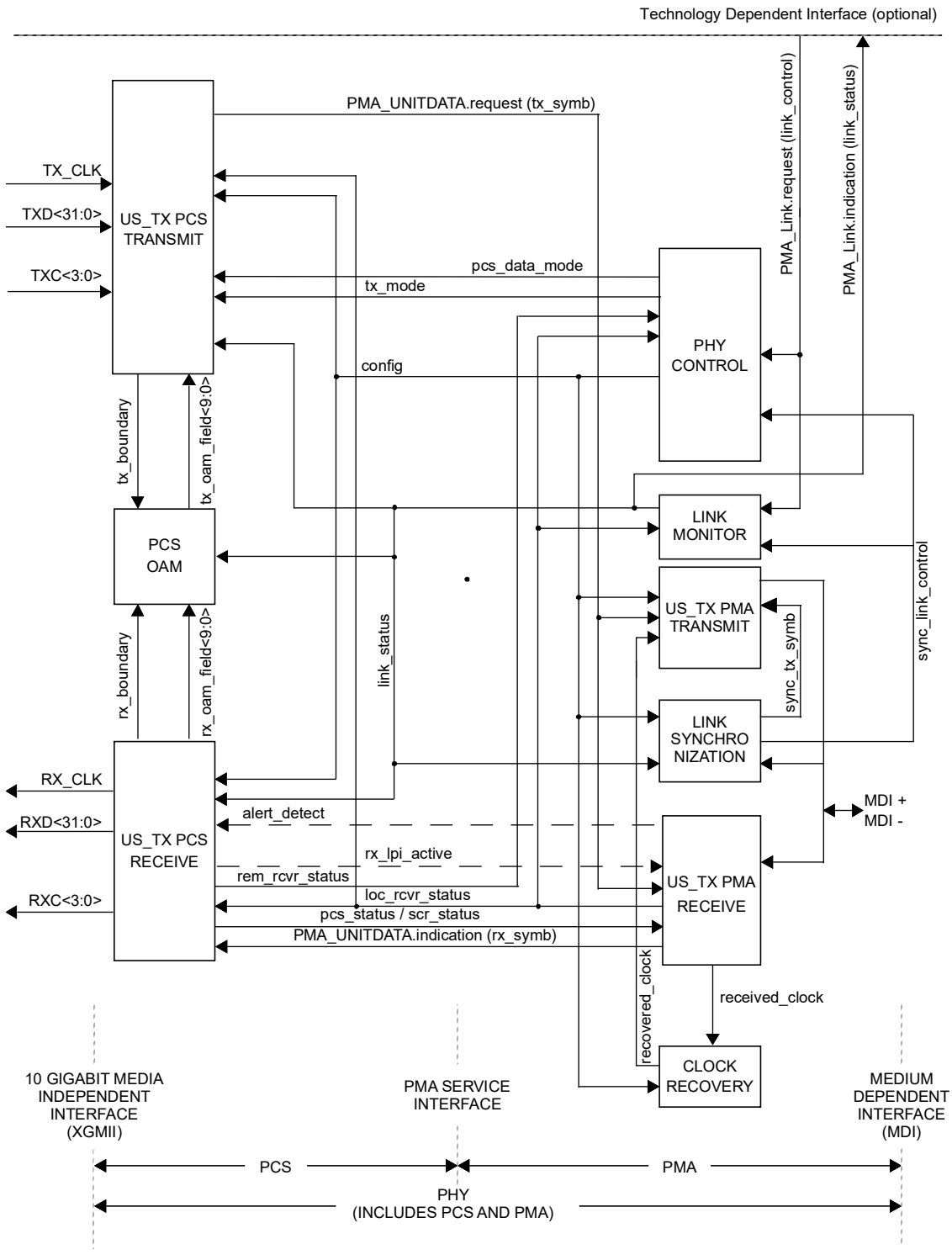
Summary provided by contribution later in project



NOTE 1—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

NOTE 2—Signals and functions shown with dashed lines are optional.

Figure 200–1—DS_TX functional block diagram



NOTE 1—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

NOTE 2—Signals and functions shown with dashed lines are optional.

Figure 200–2—US_TX functional block diagram

200.1.4.1 Physical Coding Sublayer (PCS), high speed path

For the high speed path, the DS_TX PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, to the 2.5G+100MBASE-T1/V1, 5G+100MBASE-T1/V1, or 10G+100MBASE-T1/V1 Physical Medium Attachment (PMA) sublayer. In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the high data rate direction, the PCS functions as specified in 149.3.

200.1.4.2 Physical Coding Sublayer (PCS), low speed path

For the low speed path, in normal mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block.

These 65-bit blocks are then aggregated into groups of 4 blocks. The contents of each group are contained in a vector tx_group4x65B. Next, 10 OAM bits and 6 Reserved bits are appended to form a 276-bit block. Each of these 276-bit blocks is formed into an RS-FEC input frame, then encoded by the RS-FEC ($50,46,2^6$). The RS-FEC output superframe consists of 300 bits. The duration of the frame is 2560 ns. Finally, these bits are exclusive OR'd with a 33-bit self-synchronizing scrambler to create the 100M+MultiGBASE-T1/V1 payload. The low data rate direction PCS transmit functions are described in 200.3.2.2.

The tx_group4x65B <259:0> is defined as:

$$\text{tx\_group4x65B} \langle 65 \times i + j \rangle = \text{tx\_coded}_i \langle j \rangle$$

where i = 0 to 3, j = 0 to 64, and tx_coded_i<64:0> is the i^{th} 64B/65B block where tx_coded_0<64:0> is the first block transmitted.

In the training mode (see 200.4.5.2), the DS_TX PCS transmits and receives PAM2 training frames, while the US_TX transmits and receives DME training frames, to synchronize to the PHY frame (and advertises capabilities such as EEE and OAM).

Details of the PCS functions and state diagrams are covered in 200.5. The interface to the PMA is an abstract message-passing interface specified in 200.7.

200.1.4.3 Physical Medium Attachment (PMA) sublayer, MultiG+100M/100M+MultiGBASE-T1/V1

The PMA couples messages from the PCS service interface onto a single balanced pair of conductors (T1) or a single coaxial cable (V1) via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions.

The PMA provides asymmetric data rate communications with 5625 x S MBd high speed and 117.1875 MBd low speed. See Table 200–1 for the definition of S. The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled following the completion of Auto-Negotiation or PHY Link Synchronization and provides the startup functions required for successful MultiG+100MBASE-T1 operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link channel and communicates this status to other functional blocks. A failure of the receive channel causes the data mode operation to stop and Auto-Negotiation or Link Synchronization to restart.

PMA functions and state diagrams are specified in 200.6 and 200.7. The electrical parameters of the PMA, i.e., test modes and electrical specifications for the transmitter and receiver, are specified in 200.9 and 200.10.

The PMA functions for the high data rate direction are as specified in 149.4 with the exceptions in this clause.

200.1.4.4 Delete

200.1.4.5 EEE Capability

May want to include and indicate there is no EEE Capability if it is decided this is not needed/required/desired.

200.1.4.6 Link Synchronization

The Link Synchronization function is used when Auto-Negotiation is disabled or not implemented to detect the presence of the link partner, time and control link failure, and act as the data source for the PHY control state diagram. Link Synchronization operates in a half-duplex fashion. Link Synchronization is defined in 200.8.3.

200.1.5 Signaling, high speed path

DS_TX signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over a single balanced pair of conductors (T1) or a single coaxial cable (V1). The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM2 symbols in the 2.5 Gb/s and 5 Gb/s transmit path, and PAM4 symbols in the 10 Gb/s transmit path.
c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions.
f) Block framing and other control signals.
g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
h) Ability to automatically detect and correct for incorrect polarity in the connection for the single balanced pair of conductors (T1).
i) Optionally, ability to support refresh, quiet, and alert signaling during LPI operation.

The PHY may operate in three basic modes: the normal data mode, the training mode, or an optional LPI mode.

In normal mode, the PCS generates a continuous stream of PAM4 symbols that are transmitted via the PMA at one of four voltage levels for 10Gb/s and PAM2 symbols that are transmitted via the PMA at one of two

voltage levels for 2.5Gb/s and 5Gb/s. In training mode, the PCS is directed to generate only PAM2 symbols for transmission by the PMA.

200.1.6 Signaling, low speed path

US_TX signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over single balanced pair of conductors (T1) or single coaxial cable (V1). The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to DME symbols in the high speed transmit path.
c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions.
f) Block framing and other control signals.
g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
h) Ability to automatically detect and correct for incorrect polarity in the connection for the single balanced pair of conductors (T1).

The PHY may operate in two basic modes: the normal data mode or the training mode.

In low speed direction, the PCS generates a continuous stream of DME symbols that are transmitted via the PMA in both training mode and normal mode. (See Figure <REF>)

200.1.7 Interfaces

All MultiG+100M/100M+MultiGBASE-T1/V1 PHY implementations are compatible at the MDI and at the XGMII, if implemented. Implementation of the XGMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not. The MDI for single balanced pair of conductors (T1) and single coaxial cable (V1), are different.

200.1.8 Conventions in this clause

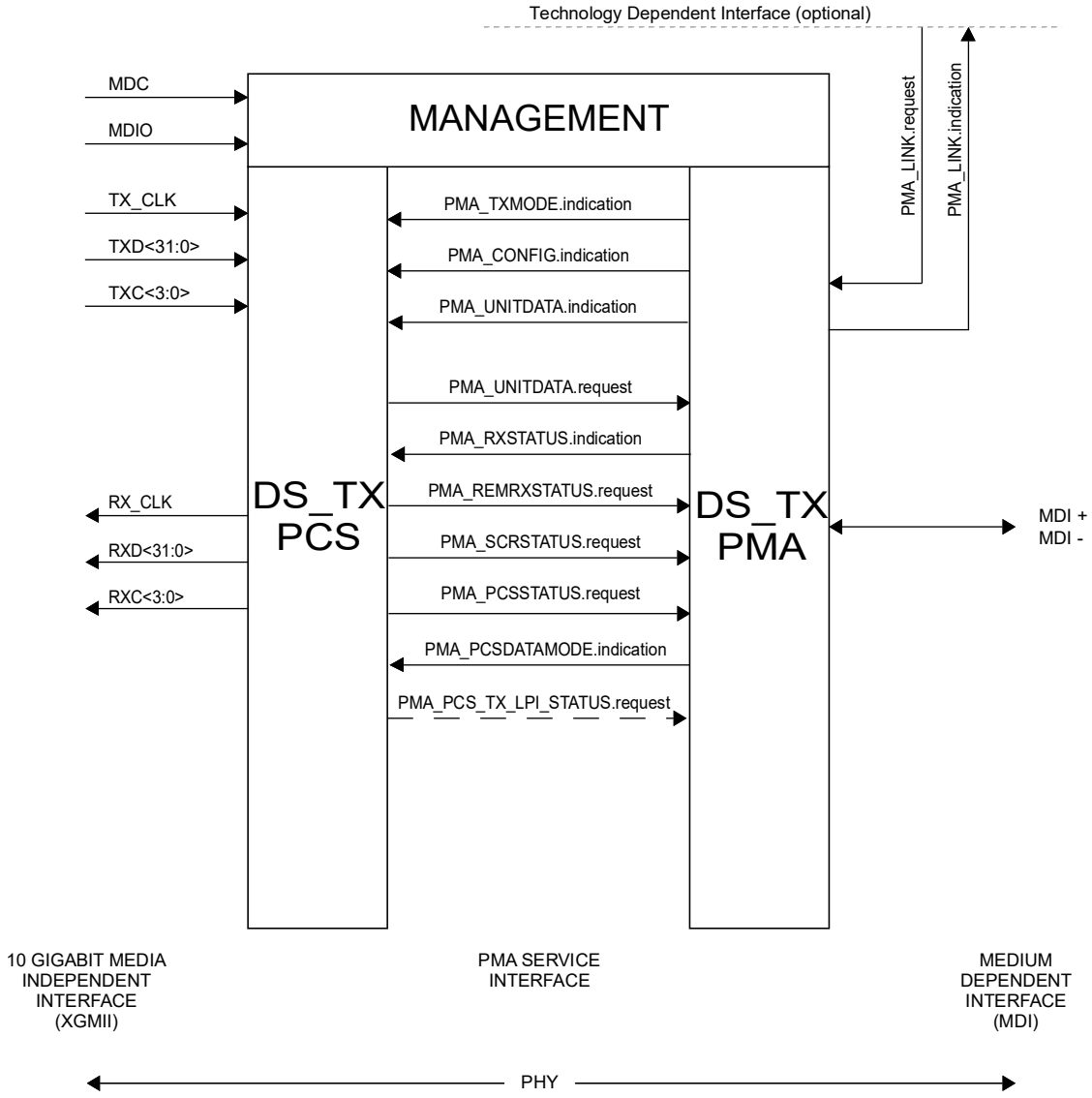
The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5, along with the extensions described in 145.2.5.2. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

Default initializations, unless specified, are left to the implementer.

200.2 High data rate service primitives and interfaces

Service primitives and interfaces in the high speed direction are as described in TBD.



NOTE—Service interface primitives shown with dashed lines are optional.

Figure 200–3—DS_TX service interfaces

200.3 Low data rate service primitives and interfaces

Service primitives and interfaces in the low speed direction transfer data and control information across the following four service interfaces:

a) 10 Gigabit Media Independent Interface (XGMII)
a) Technology Dependent Interface
a) PMA service interface
a) Medium Dependent Interface (MDI)

The XGMII is specified in Clause 46; the Technology Dependent Interface is specified in 98.4. The PMA service interface is defined in <REF> and the MDI is defined in <REF>.

200.3.1 Technology Dependent Interface

The low speed direction uses the following service primitives to exchange status indications and control signals across the Technology Dependent Interface, required in PHYs that implement Auto-Negotiation, as specified in 98.4:

PMA_LINK.request(link_control)
PMA_LINK.indication(link_status)

200.3.1.1 PMA_LINK.request

PMA_LINK.request in the low speed direction is as described in 149.2.1.1.

200.3.1.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 98.4.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation functions about the status of the underlying link.

200.3.1.2.1 Semantics of the primitive

PMA_LINK.indication(link_status)

The link_status parameter can take on one of two values: FAIL or OK.

FAIL	No valid link established.
OK	The Link Monitor function indicates that a valid US_TX link is established. Reliable reception of signals transmitted from the remote PHY is possible.

200.3.1.2.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 200–TBD.

200.3.1.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 98.4.1.

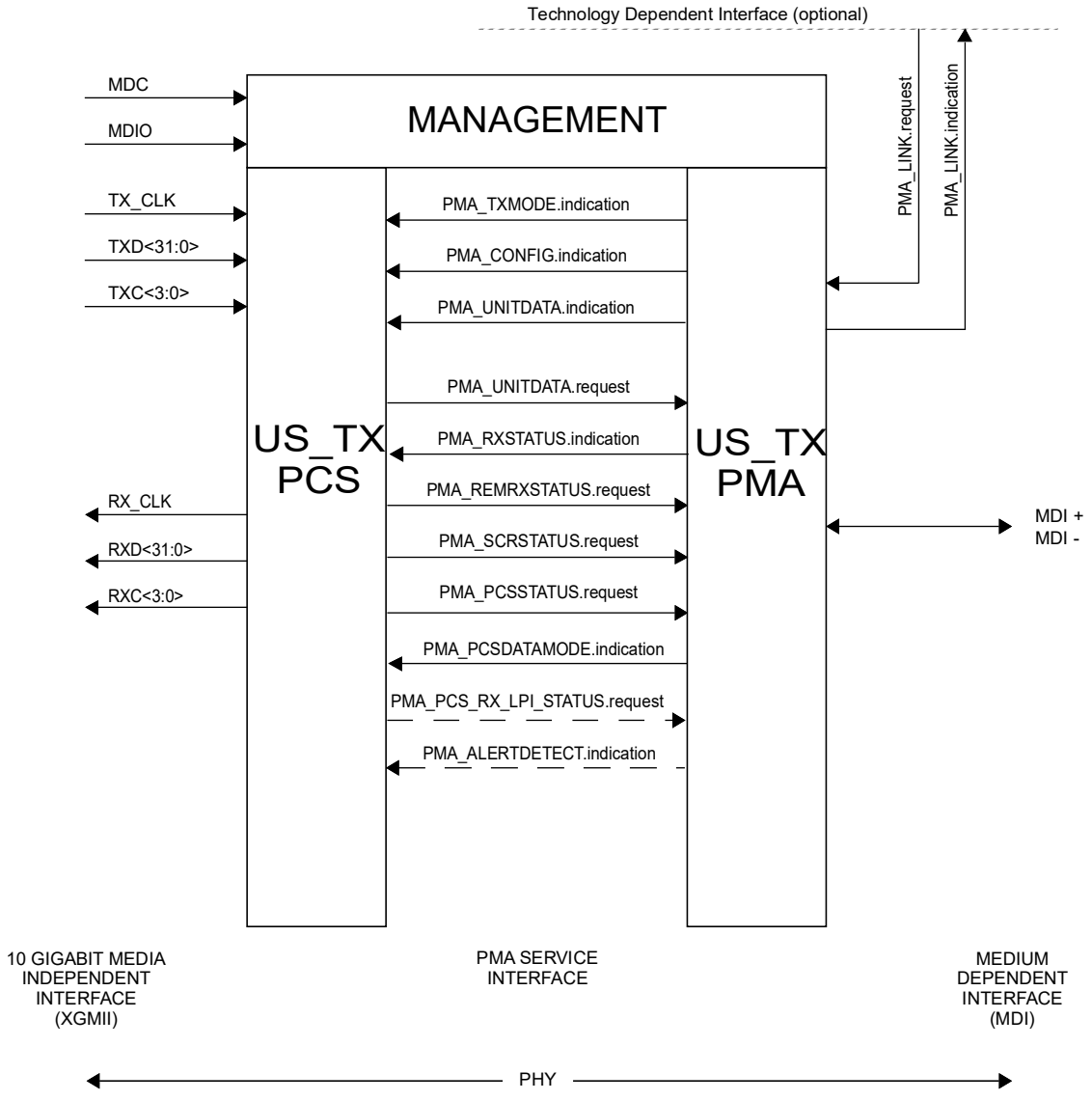
200.3.2 PMA service interface

The low speed path uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication(tx_mode)
PMA_CONFIG.indication(config)
PMA_UNITDATA.request(tx_symb)
PMA_UNITDATA.indication(rx_symb)
PMA_SCRSTATUS.request(scr_status)
PMA_PCSSTATUS.request(pcs_status)

PMA_RXSTATUS.indication(loc_rcvr_status)
PMA_REMRXSTATUS.request(rem_rcvr_status)
PMA_PCSDATAMODE.indication (pcs_data_mode)

The use of these primitives is illustrated in Figure 200–4. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 200–4.



NOTE—Service interface primitives shown with dashed lines are optional.

Figure 200–4—US_TX service interfaces

200.3.2.1 PMA_TXMODE.indication

The low speed path transmitter normally sends over the MDI symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

200.3.2.1.1 Semantics of the primitive

PMA_TXMODE.indication(tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following values of the form:

SEND_N	This value is continuously asserted during transmission of sequences of symbols representing an XGMII data stream in the data mode.
SEND_T	This value is continuously asserted in case transmission of sequences of symbols representing the training mode is to take place.
SEND_Z	This value is continuously asserted in case transmission of zeros is required.

200.3.2.2 PMA_CONFIG.indication

As specified for MultiGBASE-T1 PHYs in 149.2.2.2.

200.3.2.3 PMA_UNITDATA.request

PMA_UNITDATA.request(tx_symb)

During low data rate transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb the value of the symbols to be sent over the MDI. The tx_symb may take on one of the following values:

DME	in normal operation.
0	when zeros are to be transmitted in the following case: when PMA_TXMODE.indication is SEND_Z during PMA training.

200.3.2.4 PMA_UNITDATA.indication

The low speed path PMA generates PMA_UNITDATA.indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the low data rate PMA_UNITDATA.indication primitive is 117.1875 MHz; as governed by the recovered clock.

200.3.2.5 PMA_SCRSTATUS.request

200.3.2.6 PMA_PCSSTATUS.request

200.3.2.7 PMA_RXSTATUS.indication

200.3.2.8 PMA_REMRXSTATUS.request

200.3.2.9 PMA_PCSDATAMODE.indication

200.4 Physical Coding Sublayer (PCS) functions, high speed path

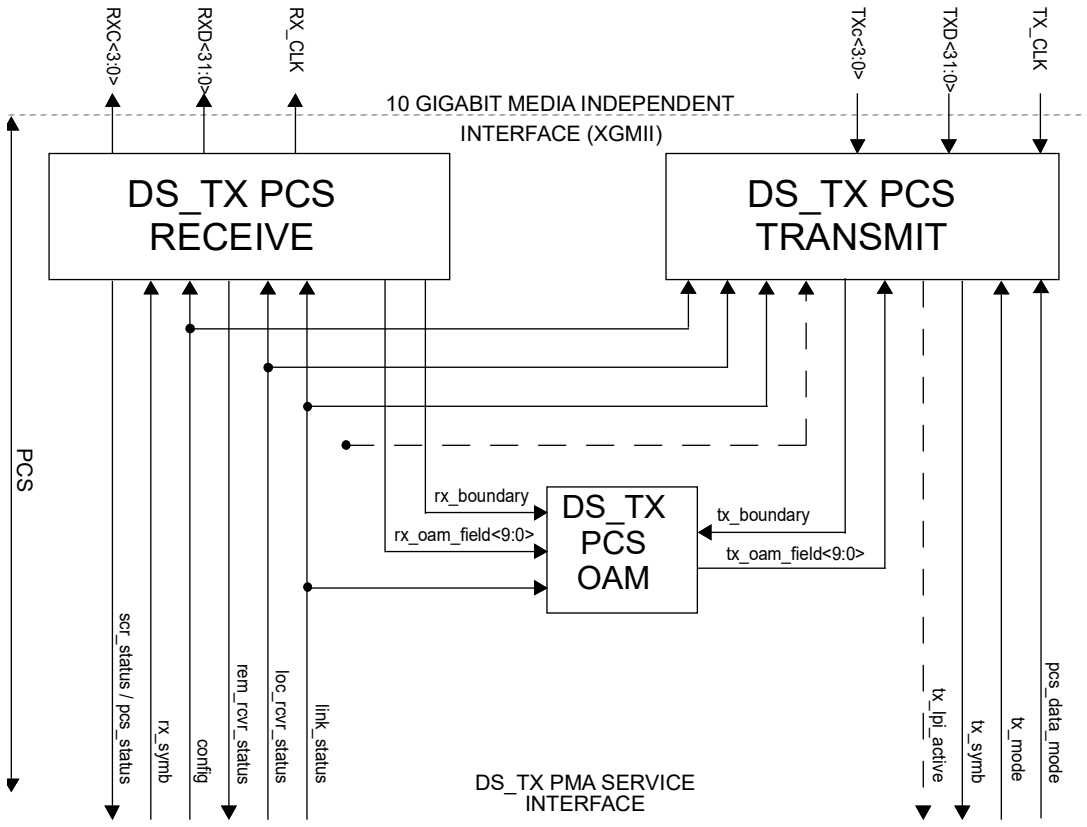
The PCS functions for DS_TX are as specified for MultiGBASE-T1 PHYs in 149.3 with the exception that 2.5Gb/s and 5Gb/s use PAM2 instead of PAM4 in data mode.

200.4.1 PCS service interface (XGMII)

200.4.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 200–5, shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 200–5.



NOTE—tx_lpi_active is only required for the EEE capability.

Figure 200–5—DS_TX PCS reference diagram

200.4.2.1 PCS Reset function

As specified for MultiGBASE-T1 PHYs in 149.3.2.1.

200.4.2.2 PCS Transmit function

There will need to be some changes, as the text and Figure 149-5 only mentionsPAM4 which only applies to 10G.

The PCS transmit function for DS_TX is as specified for MultiGBASE-T1 PHYs in 149.3.2.2 with the exception that 2.5Gb/s and 5Gb/s use PAM2 instead of PAM4 in data mode.

200.4.2.2.1 Use of blocks

Mentions LPI.

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.1.

200.4.2.2.2 65B RS-FEC transmission code

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.2.

200.4.2.2.3 Notation conventions

There will need to be some changes, as Figure 149-6 and 149-7 specify Gray Mapping and PAM4 Mapping which only apply to 10G.

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.3 with the exception that 2.5Gb/s and 5Gb/s use PAM2 instead of PAM4 in data mode.

200.4.2.2.4 Block structure

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.4.

200.4.2.2.5 Control codes

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.5.

200.4.2.2.6 Ordered sets

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.6.

200.4.2.2.7 Idle (/I/)

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.7.

200.4.2.2.8 LPI (/LI/)

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.8.

200.4.2.2.9 Start (/S/)

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.9.

200.4.2.2.10 Terminate (/T/)

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.10.

200.4.2.2.11 Ordered set (/O/)

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.11.

200.4.2.2.12 Error (/E/)

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.12.

200.4.2.2.13 Transmit process

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.13.

200.4.2.2.14 RS-FEC framing and RS-FEC encoder

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.14.

200.4.2.2.15 Reed-Solomon encoder

As specified for MultiGBASE-T1 PHYs in 149.3.2.2.17.

200.4.2.2.16 PCS scrambler

The PCS Transmit function employs side-stream scrambling as defined in 149.3.4.

For 10Gb/s with PAM4 encoding the PCS scrambler is as specified for MultiGBASE-T1 PHYs in 149.3.2.2.18.

For 2.5Gb/s and 5Gb/s with PAM2 encoding, the bits of the interleaved RS-FEC superframe are scrambled using an additive scrambler. The scrambling sequence $DS_n[0]$ is equal to $Scr_n[0]$ defined in 149.3.4. The $DS_n[0]$ is applied as additive scrambler sequence to incoming data bits D_n to generate a single scrambled data A_n as shown in Equation (149-4).

200.4.2.2.17 PAM encoding

Do we need to reference 149.3.2.2.19 for Gray mapping for the PAM4?

The 10G PCS transmit process shall encode each output symbol to one of four PAM4 levels as specified in this subclause.

0 maps to –1,
1 maps to –1/3,
2 maps to +1/3, and
3 maps to +1.

The 5G and 2.5G PCS transmit process shall encode each output symbol to one of two PAM2 levels as specified in this subclause.

0 maps to +1, and
1 maps to –1.

200.4.2.2.18 EEE capability

Only need if supporting EEE

200.4.2.3 PCS Receive function

As specified for MultiGBASE-T1 PHYs in 149.3.2.3.

200.4.2.3.1 Frame and block synchronization

As specified for MultiGBASE-T1 PHYs in 149.3.2.3.1 with the exception that 2.5Gb/s and 5Gb/s use PAM2 instead of PAM4 in data mode.

200.4.2.3.2 PCS descrambler

As specified for MultiGBASE-T1 PHYs in 149.3.2.3.2.

200.4.2.3.3 Invalid blocks

As specified for MultiGBASE-T1 PHYs in 149.3.2.3.3.

200.4.3 Test-pattern generators

As specified for MultiGBASE-T1 PHYs in 149.3.3.

200.4.4 Side-stream scrambler polynomials

The scrambler polynomials are as specified in Equation (149-5) and Equation (149-6) in 149.3.4. The polynomial in Equation (149-5) is always used for the low data rate direction and the polynomial in Equation (149-6) is always used for the high data rate direction.

200.4.5 PMA training frame

This may be able to be a PAM2 signal that is the same for both low speed and high speed. If it is, this subclause would refer to 200.5.5.

200.4.5.1 Generation of symbol Tn

As specified for MultiGBASE-T1 PHYs in 149.3.5.1.

200.4.5.2 PMA training mode descrambler polynomials

As specified for MultiGBASE-T1 PHYs in 149.3.5.2.

200.4.6 LPI signaling

Only need if supporting EEE

200.4.7 Detailed functions and state diagrams

As specified for MultiGBASE-T1 PHYs in 149.3.7.

200.4.7.1 State diagram conventions

As specified for MultiGBASE-T1 PHYs in 149.3.7.1.

200.4.7.2 State diagram parameters

As specified for MultiGBASE-T1 PHYs in 149.3.7.2.

200.4.7.2.1 Constants

Some constants may be excluded if LPI is not supported.

As specified for MultiGBASE-T1 PHYs in 149.3.7.2.1.

200.4.7.2.2 Variables

Some variables may be excluded if LPI is not supported.

As specified for MultiGBASE-T1 PHYs in 149.3.7.2.2.

Do we need to add 200.4.7.2.3 for Timers, 200.4.7.2.4 for Functions, 200.4.7.2.5 for Counters and 200.4.7.2.6 for Messages?

200.4.8 PCS management

As specified for MultiGBASE-T1 PHYs in 149.3.8.

200.4.9 MultiG+100MBASE-T1/V1 operations, administration, and maintenance (OAM)

As specified for MultiGBASE-T1 PHYs in 149.3.9.

200.5 Physical Coding Sublayer (PCS) functions, low speed path

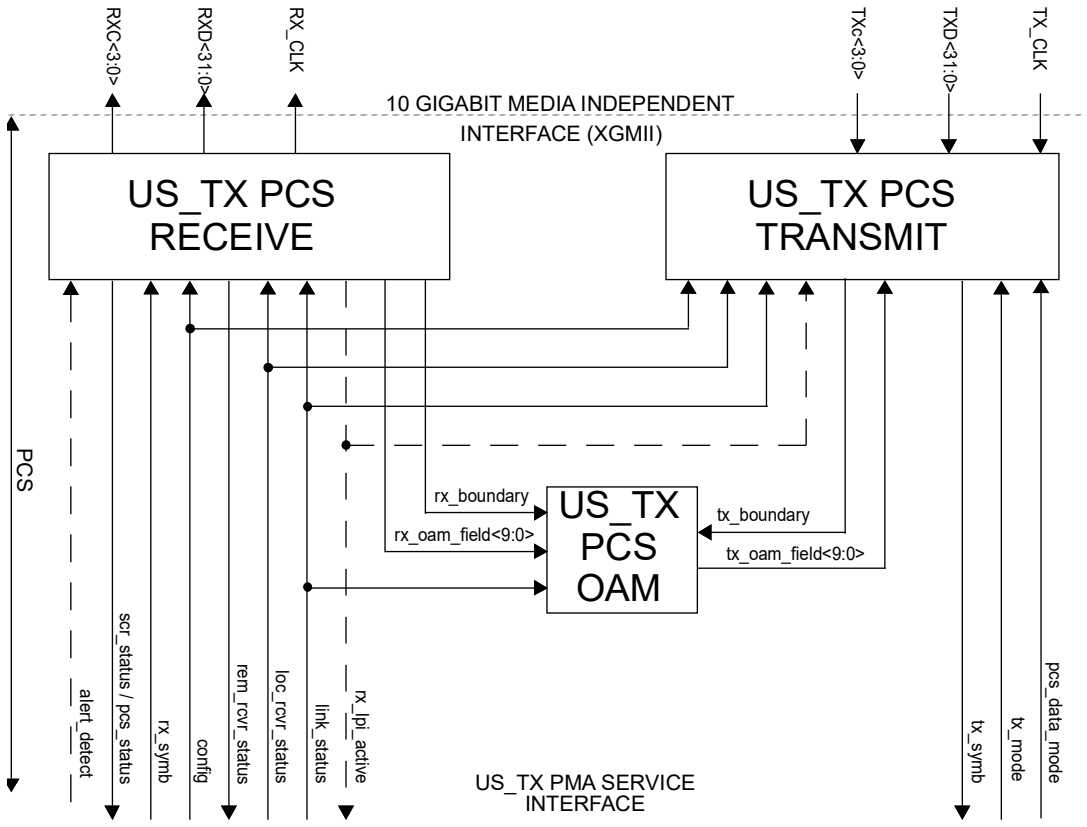
200.5.1 PCS service interface (MII)

The US_TX PCS service interface allows the 100M+MultiGBASE-T1/V1 PCS to transfer information to and from a PCS client. The PCS service interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46. The XGMII is running at 1/100th the rate of 10G, 1/50th the rate of 5G, and 1/25th the rate of 2.5G.

200.5.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 200–6, shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 200–6.



NOTE—rx_lpi_active is only required for the EEE capability.

Figure 200–6—PCS reference diagram

200.5.2.1 PCS Reset function

The low data rate PCS reset function shall be as specified in 149.3.2.1.

200.5.2.2 PCS Transmit function

The PCS transmit function shall comply with the PCS 64B/65B Transmit state diagram in Figure 149-16 and Figure 149-17, and to the PCS Transmit bit ordering in Figure 200–7.

Dashed rectangles in Figure 149-16 and Figure 149-17 are not part of the low speed PCS.

When communicating with the XGMII, the MultiGBASE-T1 PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

After mapping the eight XGMII transfers to 64B/65B blocks, the subsequent functions of the PCS Transmit process take four 65B blocks and append a 10-bit OAM field followed by 6 reserved bits set to all 1s to each

group. This forms the input to RS-FEC which adds 24 parity bits. The resulting 300 bits are then scrambled. These bits are then sent one bit at a time as a symbol. Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a symbol that is transferred to the PMA via the PMA_UNITDATA.request primitive. The symbol period, T, is 1000 / 117.1875 ns.

The operation of the PCS Transmit function is controlled by the PMA_TXMODE.indication message received from the PMA PHY Control function.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit shall generate a sequence (Tn) defined in TBD to the PMA via the PMA_UNITDATA.request primitive.

During training mode an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes requests for remote transmitter settings. (See TBD.)

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the normal mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control. During transmission, the four blocks of 65B encoded bits are appended with a 10-bit OAM field followed by six 1s to form the RS-FEC input frame. During data encoding, PCS Transmit utilizes Reed-Solomon encoders to generate and append 24 parity check bits to form 300-bit (50,46, 2^6) RS-FEC frames.

200.5.2.2.1 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into an RS-FEC frame, and vice versa, using a 65B RS-FEC coding scheme. The PMA training frame synchronization allows establishment of RS-FEC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS.

The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 149.3.2.2.2.

200.5.2.2.2 65B RS-FEC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 200–7 for transmit and Figure 200–8 for receive. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 149.3.2.2.4 for information on how blocks containing control characters are mapped.

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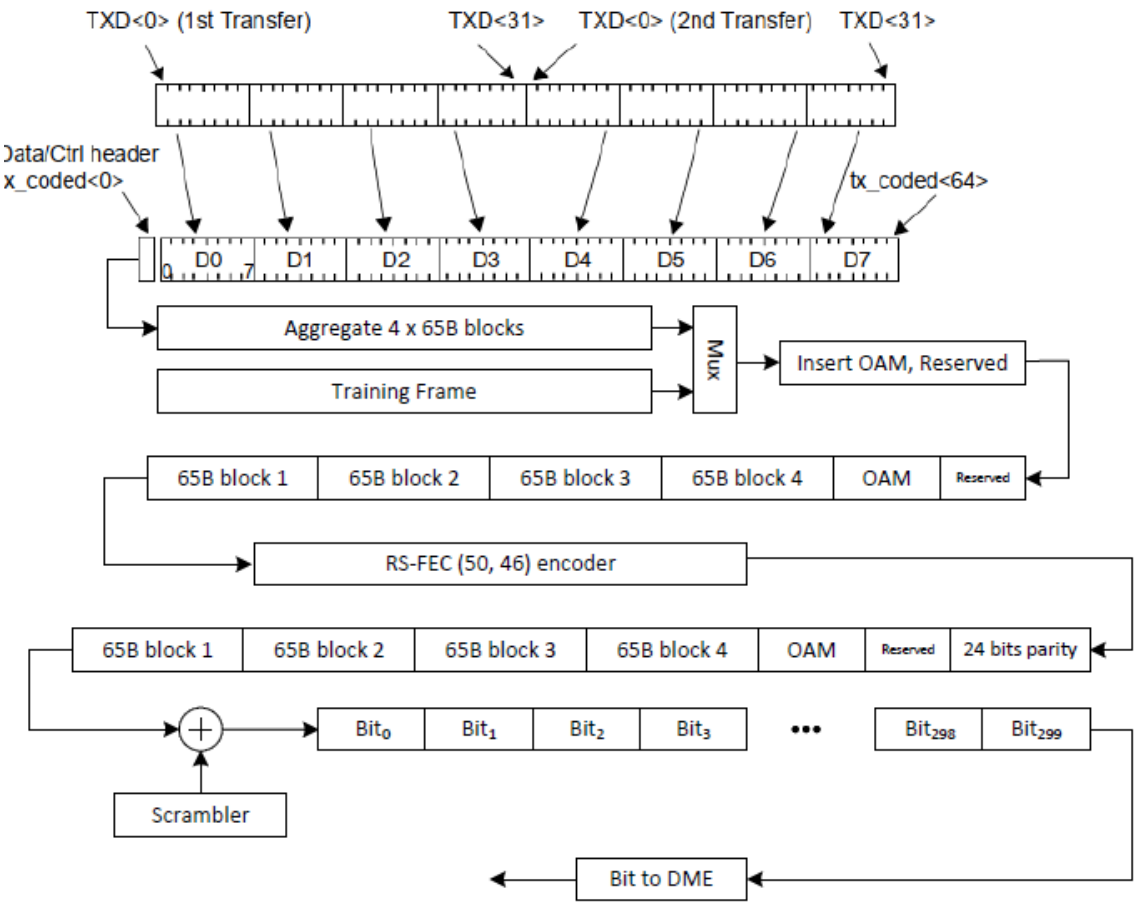

Figure 200–7—PCS Transmit bit ordering for data mode and training mode

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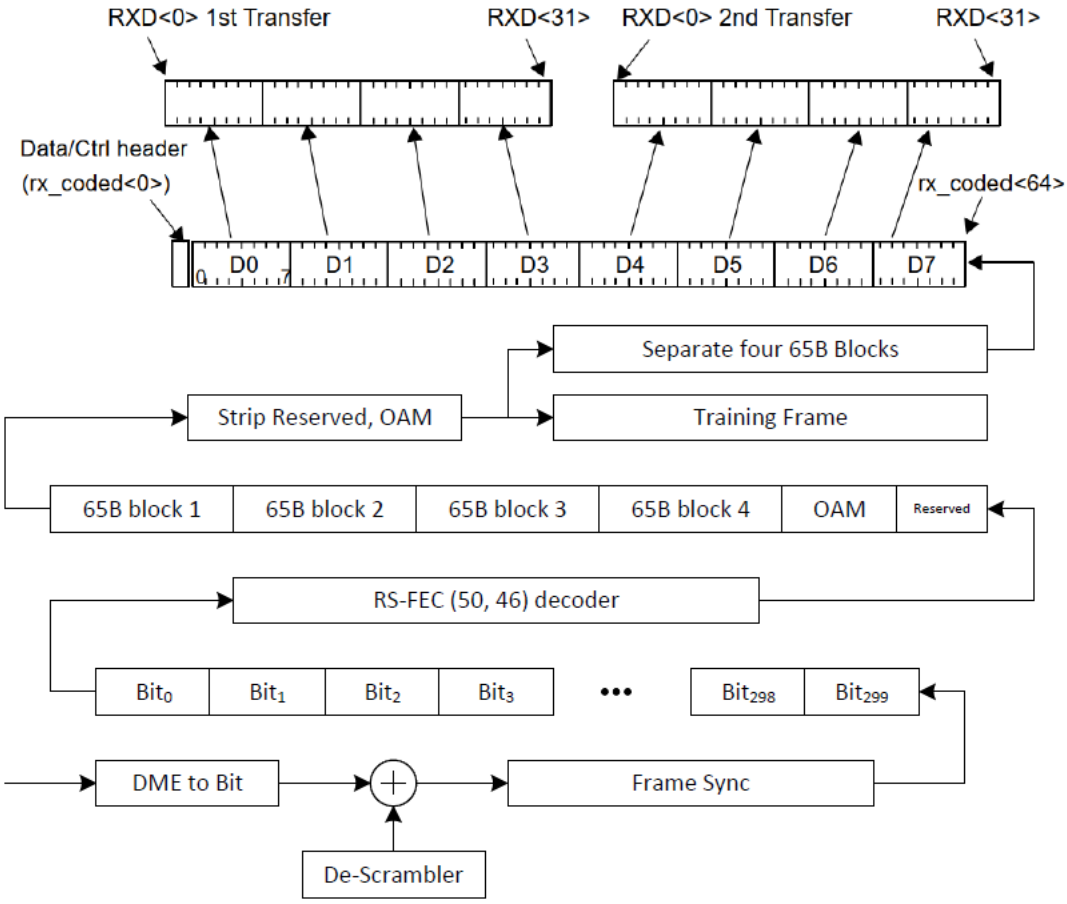

Figure 200–8—PCS Receive bit ordering for data mode and training mode

200.5.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes eight data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7. Control characters other than /O/, /S/, and /T/ are labeled C0 to C7. The control character for ordered set is labeled as O_0 or O_4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S_0 or S_4 for the same reason. The control character for terminate is labeled as T_0 to T_7.

For 100M+MultiGBASE-T1/V1, two XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfer(s).

Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled tx_coded<31:0> and rx_coded<31:0> where tx_coded<0> and rx_coded<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

200.5.2.2.4 Block structure

The low data rate block structure shall be as specified in 149.3.2.2.4

200.5.2.2.5 Control codes

The same set of control characters are supported by the XGMII and the US_TX PCS. The representations of the control characters are the control codes. The XGMII encodes a control character into an octet (an eight-bit value). The US_TX PCS encodes the start and terminate control characters implicitly by the block type field. The US_TX PCS encodes the ordered set control codes using a combination of the block type field and a four-bit O code for each ordered set. The US_TX PCS encodes each of the other control characters into a seven-bit C code.

The control characters and their mappings to US_TX control codes and XGMII control codes are specified in Table 149–2. All XGMII control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

200.5.2.2.6 Ordered sets

The low data rate ordered sets shall be as specified in 149.3.2.2.6.

200.5.2.2.7 Idle (/I/)

The low data rate ordered sets shall be as specified in 149.3.2.2.7.

200.5.2.2.8 Start (/S/)

The low data rate ordered sets shall be as specified in 149.3.2.2.9.

200.5.2.2.9 Terminate (/T/)

The low data rate ordered sets shall be as specified in 149.3.2.2.10.

200.5.2.2.10 Ordered set (/O/)

The low data rate ordered sets shall be as specified in 149.3.2.2.11.

200.5.2.2.11 Error (/E/)

The low data rate ordered sets shall be as specified in 149.3.2.2.12.

200.5.2.2.12 Transmit process

The transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. Eight XGMII data transfers are encoded into an RS-FEC frame. It takes 300 PMA_UNITDATA transfers to send an RS-FEC frame of data. Therefore, for 100M+MultiGBASE-T1/V1, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly 2:75, then the transmit process

does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 149-16 and Figure 149-17). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the transcoder and scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload

200.5.2.2.13 RS-FEC framing and RS-FEC encoder

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 200–7 for transmit and Figure 200–8 for receive. These figures illustrate the processing of a multiplicity of blocks containing 32 data octets. See 200.4.2.2.4 for information on how blocks containing control characters are mapped.

200.5.2.2.14 Reed-Solomon encoder

The group of 300 bits are encoded using a Reed-Solomon encoder operating over the Galois Field GF (2^6) where the symbol size is six bits. The encoder processes forty-six 6-bit RS-FEC message symbols to generate four 6-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of fifty 6-bit RS-FEC symbols. For the purposes of this clause, the particular Reed-Solomon code is denoted as RS-FEC(50,46,2^6).

The code is based on the generating polynomial given by Equation (200–1).

$$g(x) = \prod_{j=0}^{3} (x - \alpha^j) = g_4x^4 + g_3x^3 + g_2x^2 + g_1x + g_0 \quad (200–1)$$

In Equation (200–1), α, is a primitive element of the finite field defined by the primitive polynomial 0x43 = $x^6 + x + 1$.

Equation (200–2) defines the message polynomial $m(x)$ whose coefficients are the message symbols m_{45} to m_0.

$$m(x) = m_{45}x^{49} + m_{44}x^{48} + \ldots + m_1x^5 + m_0x^4 \quad (200–2)$$

Each message symbol m_i is the bit vector ($m_{i,5}$, $m_{i,4}$, ... $m_{i,1}$,$m_{i,0}$), which is identified with the element of the finite field. $m_{i,0}$ is the first bit transmitted. The message symbols are composed of the bits in tx_RSmessage<275:0> where
$m_{i,j}$ = tx_RSmessage <(45 – i) × 6 + j>, for i = 0 to 45, and j = 0 to 5.

tx_RSmessage<49:0> prior to RS-FEC (50,46) encoder is formed as follows:

tx_RSmessage<259:0> = tx_group4x65B<259:0>.
tx_RSmessage<269:260> = OAM_field<9:0>.
tx_RSmessage<279:270> = 111111.

The first symbol input to the encoder is m_{45}.

Equation (200–3) defines the parity polynomial $p(x)$ whose coefficients are the parity symbols p_3 to p_0.

$$p(x) = p_3x^3 + p_2x^2 + p_1x + p_0 \quad (200–3)$$

Each parity symbol p_i is the bit vector $(p_{i,5}, p_{i,4}, \ldots p_{i,1}, p_{i,0})$, which is identified with the element of the finite field. $p_{i,0}$ is the first bit transmitted.

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This can be computed using the shift register implementation illustrated in Figure 200–9. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0, is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of x, $c_{49} = m_{45}$ is transmitted first and the coefficient of the lowest power of x, $c_0 = p_0$ is transmitted last. The first bit transmitted from each symbol is bit 0.

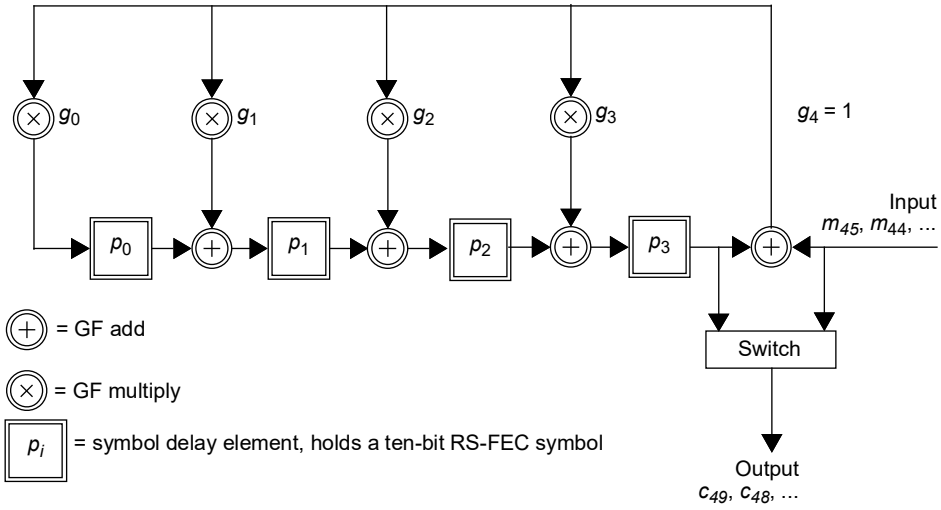

Figure 200–9—Reed-Solomon encoder functional model

The coefficients of the generator polynomial for the code are presented in Table 200–3.

Table 200–3—Coefficients of the generator polynomial g_i (decimal)

i	RS-FEC(50, 46)
0	3
1	59
2	54
3	15
4	1

200.5.2.2.15 PCS scrambler

The bits of the interleaved RS-FEC superframe are scrambled using an additive scrambler. For each bit, D_n, a scrambler bit is generated from the side-stream scrambler. The scrambler bit, DS_n, is equal to $Scr_n[0]$ of $G_M(x)$ defined in 149.3.4.

DS_n is applied as additive scrambler sequences to incoming data bits D_n to generate the scrambled data bit A_n as shown in Equation (200–4).

$$A_n = D_n \oplus DS_n \quad (200–4)$$

200.5.2.2.16 Differential Manchester encoding (DME)

The scrambled data bit, A_n, is encoded using Differential Manchester Encoding (DME).

The following rules apply to encode a bit to DME:

— A “clock transition” shall always be generated at the start of each bit.
— A “data transition” in the middle of a nominal bit period shall be generated if the bit to be transmitted is a logical '1'. Otherwise, no transition shall be generated until the next bit.

See Figure 200–10 and Table 200–4.

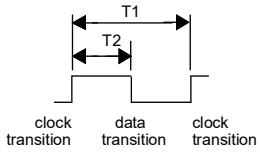

Figure 200–10—DME encoding scheme

Table 200–4—DME timings

Parameter name	Description	Minimum value	Nominal value	Maximum value	Unit of measure
T1	Clock transition to clock transition	$8.5\overline{3}$–100 ppm	$8.5\overline{3}$	$8.5\overline{3}$+100 ppm	ns
T2	Clock transition to data transition (data = 1)	4.05	$4.2\overline{6}$	4.48	ns

NOTE - I used the 117.1875 MBd rate in the text from May. For the T2 timing, I used the ~+/- 5% (38, 40, 42 ns) for the T2 (T3 in da) that was in the da draft. Designers should discuss desired accuracy, which might need to be better for crystal less operation.

200.5.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 149-18, and the PCS Receive bit ordering in Figure 200–8 including compliance with the associated state variables as specified in 149.3.7.2.2.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received DME symbols are demapped and descrambling is performed.

Following descrambling, the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. The RS-FEC decoded frame is then separated into ten OAM bits and six Reserved bits and four 64B/65B blocks. This process generates the 64B/65B block vector rx_coded<64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 149-18). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received DME training framing and signals the reliable acquisition of the descrambler state by setting the scr_status parameter of the PMA_SCRSTATUS.request primitive to OK.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If forty consecutive RS-FEC frame errors are detected, the block_lock flag is de-asserted. The block_lock flag is re-asserted upon detection of a valid RS-FEC frame. When block_lock is asserted and hi_rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication (loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training frame includes an alignment pattern every 300 symbols, which can be used to find the RS-Frame boundary. The side stream descrambler employs the generator polynomial per Equation (149–5). When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.

200.5.2.3.1 Frame and block synchronization

When operating in the data mode, the receiving PCS shall form a DME stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from rx_DME_0 to rx_DME_299 (see Figure 200–5). It obtains block lock to the PHY frames during training using synchronization bits provided in the training frames.

200.5.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process for generation of RXD<31:0> to the XGMII. The side stream descrambler employs the generator polynomial per Equation (149-5).

200.5.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exist:

a) The block type field contains a reserved value.

a) Any control character contains a value not in Table 149–2.

a) Any O code contains a value not in Table 149–2.

a) The block contains information from the payload of an invalid RS-FEC frame.

The PCS Receive function shall check the integrity of the RS-FEC parity bits defined in 200.5.2.2.14. If the check fails, the RS-FEC frame is invalid.

The R_BLOCK_TYPE of an invalid block is set to E.

200.5.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, the channel, and remote receiver. When the transmit PCS is operating in test-pattern mode it shall transmit continuously by setting the data input to the scrambler to zero.

When the receiver PCS is operating in test-pattern mode it shall receive continuously as illustrated in Figure 200–5. The output of the received descrambled values should be zero. Any nonzero values correspond to receiver bit errors. The output of the RS-FEC decoder should also be zero; however, there is the possibility that the RS-FEC decoder corrected some errors. This mode is further described as test mode 7 in TBD.

200.5.4 Side-stream scrambler polynomials

The side stream scrambler is as specified for $g_M(x)$ as specified in 149.3.4.

200.5.5 PMA training frame

During PMA training, the PHY operates as shown in Figure 200–7 and Figure 200–5 except the training frame is muxed/de-muxed in lieu of the four 64/65 blocks. The four 64B/65B blocks in the FEC frame are loaded with the internal training frame, consisting of three consecutive blocks of all zeros and the fourth block being a special control block. The structure of the special control block is as shown in Figure 200–11..

C/D								
1	Block	D0	D1	D2	D3	D4	D5	D6
1	0x5A	Reserved	Reserved	Reserved	Message	PHY Capability Bits		

Figure 200–11—Training frame 64B/65B control block

The message and PHY capability fields are as specified in 149.4.2.4.4.

The four training frame 64B/65B blocks are then concatenated with the sixteen OAM/Reserved bits and the 24 FEC parity bits, as shown in Figure 200–12. Note that the OAM (if present) should be inactive during training.

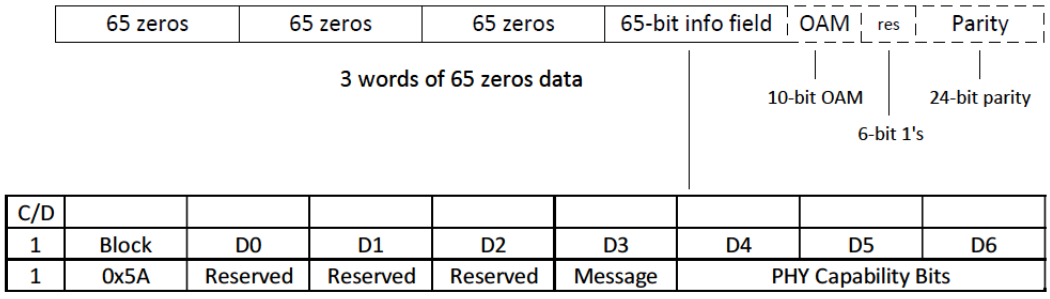

Figure 200–12—Training frame

200.5.6 Detailed functions and state diagrams

As specified for MultiGBASE-T1 PHYs in 149.3.7, except items enclosed in the dotted lines are not present.

200.5.6.1 State diagram parameters

As specified for MultiGBASE-T1 PHYs in 149.3.7.2.

200.5.6.1.1 Constants

As specified for MultiGBASE-T1 PHYs in 149.3.7.2.1.

200.5.6.1.2 Variables

As specified for MultiGBASE-T1 PHYs in 149.3.7.2.2.

200.5.7 PCS management

200.5.8 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

200.5.8.1 Status

pcs_status:

Indicates whether the PCS is in a fully operational state. It is only TRUE if pcs_data_mode is TRUE, block_lock is TRUE, and hi_rfer is FALSE. This status is reflected in MDIO bit 3.2324.10. A latch low view of this status is reflected in MDIO bit 3.2323.2 and the inverse of this status is reflected in MDIO bit 3.2323.7.

block_lock:

Indicates the state of the block_lock variable. This status is reflected in MDIO bit 3.2324.8. A latching low version of this status is reflected in MDIO bit 3.2324.6.

hi_rfer:

Indicates the state of the hi_rfer variable. This status is reflected in MDIO bit 3.2324.9. A latching high version of this status is reflected in MDIO bit 3.2324.7.

200.5.8.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

RFER_count:

6-bit counter that counts each time the RFER_BAD_RF of the RFER monitor state diagram (see Figure 149–15) is entered. This counter is reflected in MDIO register bits 3.2324.5:0. The counter is reset when register 3.2324 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

200.5.9 100M+MultiGBASE-T1/V1 operations, administration, and maintenance (OAM)

As specified for MultiGBASE-T1 PHYs in 149.3.9.

200.6 Physical Medium Attachment (PMA) sublayer, high speed path

The high speed PMA functions are as specified in 149.4, with the following exception:

1) The 2.5Gb/s signaling uses PAM2 instead of PAM4.
2) The 5Gb/s signaling uses PAM2 instead of PAM4.

200.7 Physical Medium Attachment (PMA) sublayer, low speed path

The low speed PMA Transmit function comprises a transmitter to generate a DME signal on the MDI interface.

200.7.1 PMA functional specifications

200.7.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure <REF>, shows how the operating functions relate to the messages of the PMA service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure <REF>.

200.7.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power for the device containing the PMA has not reached the operating state.

b) The receipt of a request for reset from the management entity.

PMA Reset sets pma_reset = ON while any of the above reset conditions hold TRUE. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The 100M+MultiGBASE-T1/V1 PMA takes no longer than TBD(100) ms to enter the PCS_DATA state after exiting from reset or low power mode (see Figure 149-32).

200.7.2.2 PMA Transmit

The PMA Transmit function comprises a transmitter to generate a DME modulated signal on the single balanced pair of conductors (T1) or Coaxial cable (V1). When the PHY Control state diagram (Figure 149-32) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by tx_symb onto the MDI. During Link Synchronization, when sync_link_control = DISABLE and Auto-Negotiation is either not enabled or is not implemented, the sync_tx_symb output by the PHY Link Synchronization function shall be used in place of tx_symb as the data source for PMA Transmit. The signals generated by PMA Transmit shall comply with the electrical specifications given in 149.5.2.

When the PMA_CONFIG.indication parameter config is MASTER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 149.5.2.3. The MASTER-SLAVE relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 149.4.2.8 while meeting the jitter requirements of TBD.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

When the PMA_transmit_disable variable is set to TRUE, this function shall turn off the transmitter so that the average launch power of the transmitter is less than –53 dBm.

200.7.2.3 PMA Receive function

The low speed PMA Receive function comprises a receiver for the DME signal on the MDI. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI, and to present these sequences to the PCS Receive function. The PMA translates the signals received at the MDI into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 2 x after RS-FEC decoding, over a channel meeting the requirements of 200.12 for balanced pair cabling and of 200.13 for coaxial cabling.

The low speed direction PMA Receiver function uses the parameters pcs_status and scr_status, along with other applicable receiver status, and generates the loc_rcvr_status variable accordingly The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other value (see the PHY Control state diagram in Figure 149-32). The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for pair polarity swaps.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the

link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.193.7.

200.7.2.4 PHY Control function

The Message and PHY Capability Bits in 200.5.5 are as described in 149.4.2.4.4 and 149.4.2.4.5.

All reserved fields shall be set to 0.

The PMA MDIO function mappings are as described in 149.4.2.4.9.

200.8 Common PMA Function

This clause describes items that apply to both the fast and slow directions.

200.8.1 Startup Sequence

The startup sequence shall comply with the state diagram description given in Figure 200–13. If the Auto-Negotiation function is not implemented, or disabled (mr_autoneg_en = FALSE), PMA_CONFIG is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup. The Auto-Negotiation function is optional for MultiG+100M/100M+MultiGBASE-T1/V1 PHYs. If the Auto-Negotiation function is implemented and enabled, Auto-Negotiation is the source of control (via link_control) and MASTER/SLAVE configuration; however, if Auto-Negotiation is either not enabled or is not implemented, the Link Synchronization function is the source of control (via sync_link_control) and MASTER/SLAVE configuration.

In the TRAINING state, PAM 2 transmission is used and PHY capabilities are exchanged with Infofields as specified in 149.4.2.4.5.

At any time following the TRAINING state, if the local receiver status (indicated by loc_rcvr_status) transitions to NOT_OK, PHY Control returns to the SILENT state and attempts a retrain.

The startup timing shall comply with Table 200–5 for LEADER and Table 200–6 for FOLLOWER.

Table 200–5—Startup timing maximums for LEADER

Timing interval	Maximum time (ms)
From entry to SILENT state until en_slave_tx = 1 is transmitted	TBD
From entry of SILENT state until entry to COUNTDOWN state	TBD
Entry to COUNTDOWN until entry of TX_SWITCH	TBD
Entry to exit of PCS TEST	TBD
Total (Entry to SILENT to exit of PCS TEST)	97

Table 200–6—Startup timing maximums for FOLLOWER

Timing interval	Maximum time (ms)
Entry to exit of SILENT state	TBD
Entry of SILENT state to exit of TRAINING state	TBD
Entry to COUNTDOWN until entry of TX_SWITCH	TBD
Entry to exit of PCS TEST	TBD
Total (Entry to SILENT to exit of PCS TEST)	97

200.8.2 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel causes the PMA to set link_status to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the Auto-Negotiation (if enabled) or Link Synchronization (if Auto-Negotiation is not enabled) process.

The Link Monitor function shall comply with the state diagram of Figure 149-33.

Upon power on, reset, or release from power down, the Auto-Negotiation function sets link_control = DISABLE, or PHY Link Synchronization algorithms set sync_link_control = DISABLE. During this period, link_status = FAIL is asserted. When the Auto-Negotiation function establishes the presence of a remote MultiG+100M/100M+MultiGBASE-T1/V1 PHY, link_control is set to ENABLE, or when the PHY Link Synchronization finishes the synchronization function, sync_link_control is set to ENABLE, and the Link Monitor state diagram begins monitoring the PCS and receiver lock status. As soon as reliable transmission is achieved, the variable link_status = OK is asserted, upon which further PHY operations can take place.

200.8.2.1 State variables

200.8.2.1.1 State diagram variables

The variables defined in 149.4.4.1 apply to this clause. The following additional variables are defined below.

phy_role

This variable indicates which side of the asymmetrical line the device is on.

Values:

DS_TX: MultiG+100MBASE-T1/V1 PHY.

US_TX: 100M+MultiGBASE-T1/V1 PHY.

200.8.2.1.2 Timers

The variables defined in 149.4.4.2 apply to this clause.

200.8.2.1.3 State diagrams

The PHY Control state diagram is shown in Figure 200–13, the Link Monitor state diagram is shown in Figure 149–33, and the EEE Refresh monitor state diagram for the fast data path is shown in Figure 149–34.

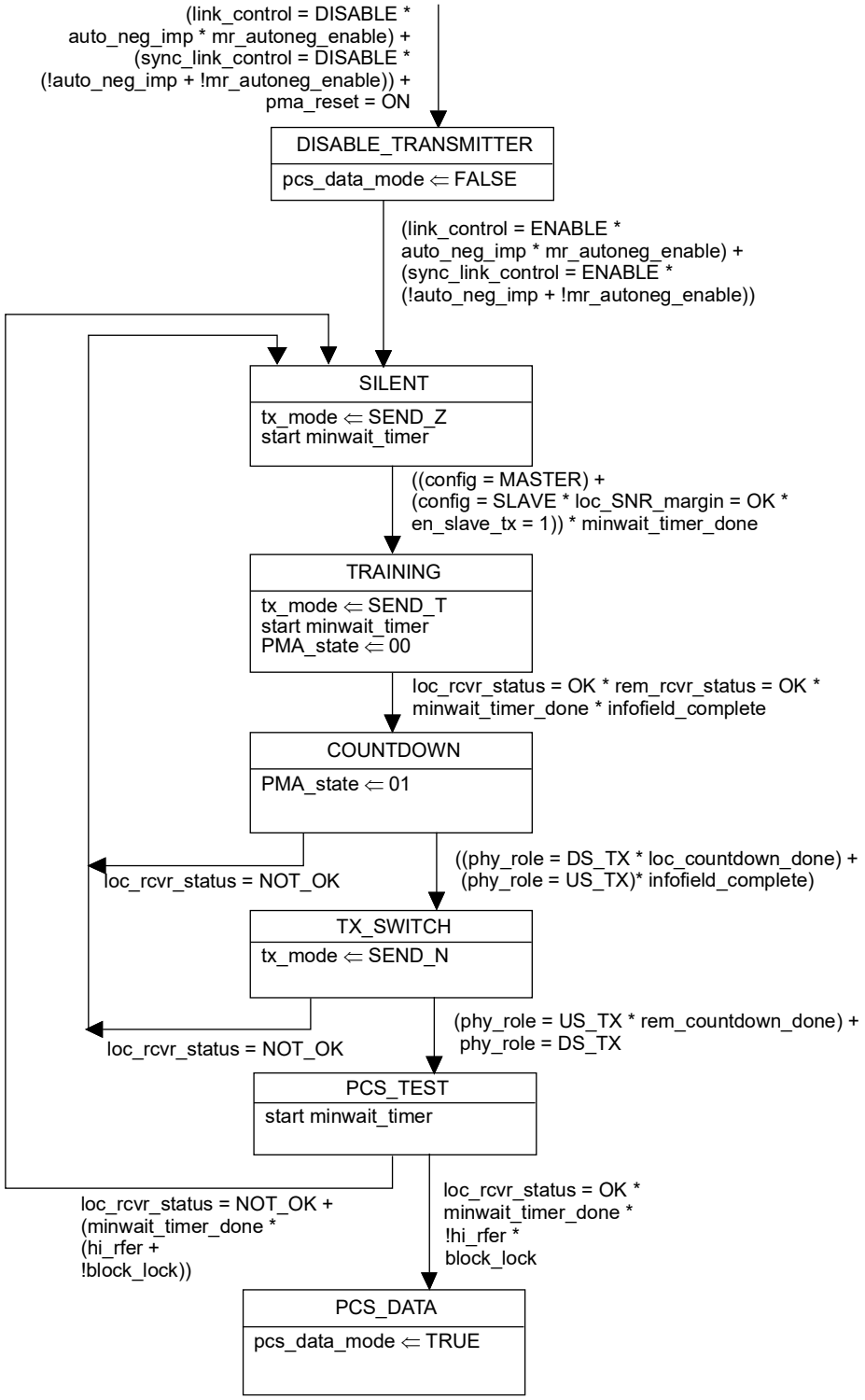

Figure 200–13—PHY Control state diagram

200.8.3 PHY Link Synchronization

If the optional Clause 98 Auto-Negotiation function is disabled or not implemented, then the Link Synchronization function shall establish the start of PHY PMA training as defined in 200.7.2.4.

When operating, the Link Synchronization function is the data source for the PMA Transmit function (see 200.7.2.2), and uses a signal, SEND_S. This signal is used by the MASTER and SLAVE to discover the link partner and synchronize the start of PMA training. The structure of the Link Synchronization signaling is shown in Figure 200–14.

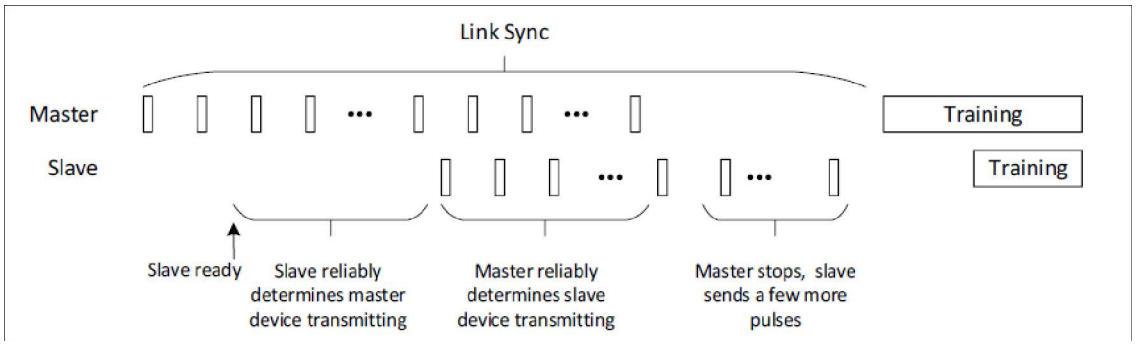

Figure 200–14—Link Synchronization signaling structure

The PHY Link Synchronization state diagram in Figure 200–15 shall be used to synchronize PHYs prior to the MultiG+100M/100M+MultiGBASE-T1/V1 link training. If the Clause 98 Auto-Negotiation function is enabled, then the Auto-Negotiation function shall be used as the mechanism for PHY synchronization and the PHY Link Synchronization state diagram in Figure 200–15 remains in the SYNC_DISABLE state.

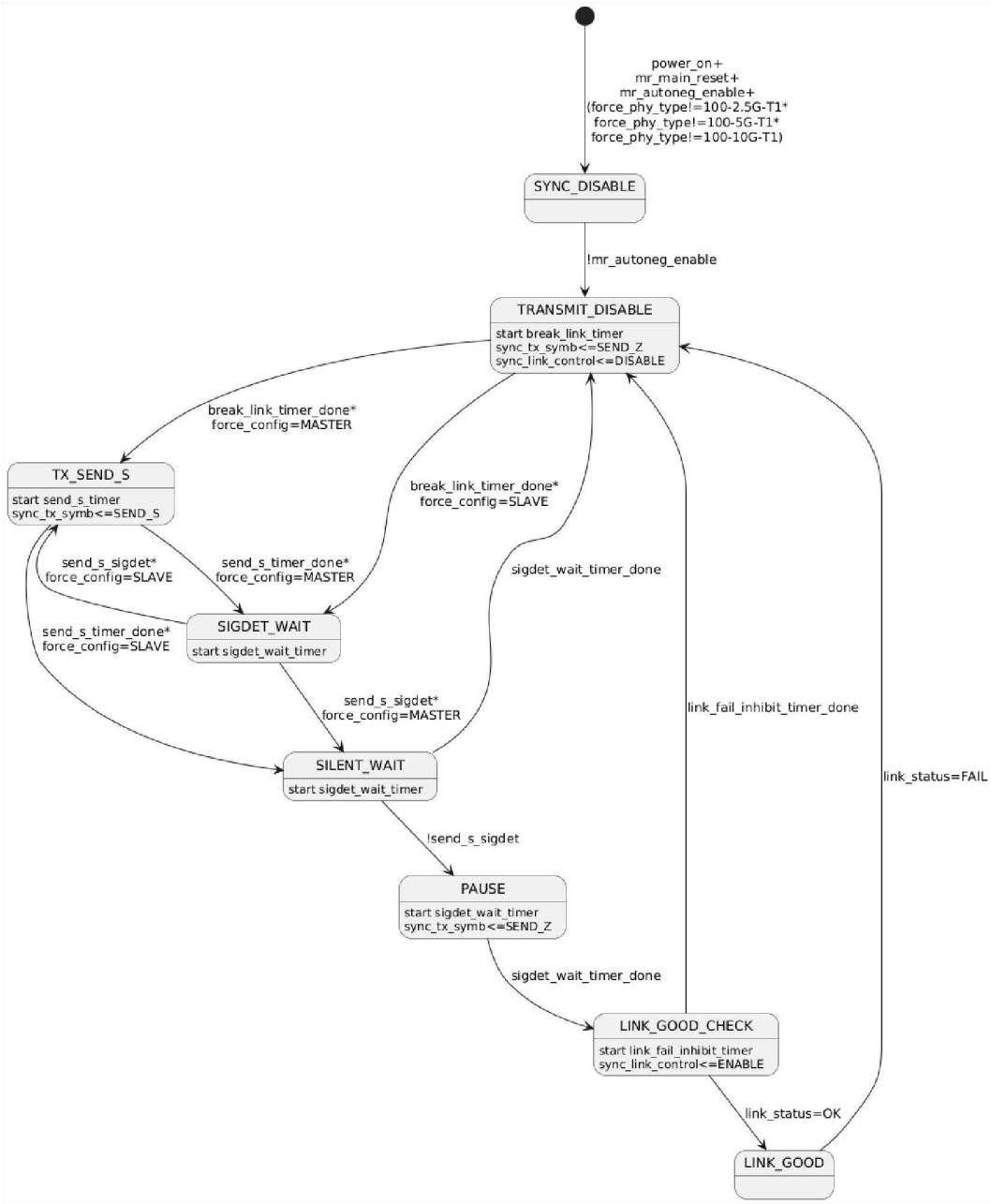

Figure 200–15—Link Synchronization state diagram

The SEND_S signal shall be a periodic signal with 192 DME symbol (1.6384 us) interval. Each period consist of signal pulse with 4 DME symbol (34.133ns) duration, and the rest of the signal period is quiet. Both MASTER and SLAVE shall transmit their pulse with a fixed interval between pulses. When both MASTER and SLAVE are transmitting, the SLAVE shall synchronize its transmit pulse to start any time between 76 to 117 DME symbols after the start of the previous MASTER pulse. The time structure of the SENS_S signals is shown in Figure 200–16.

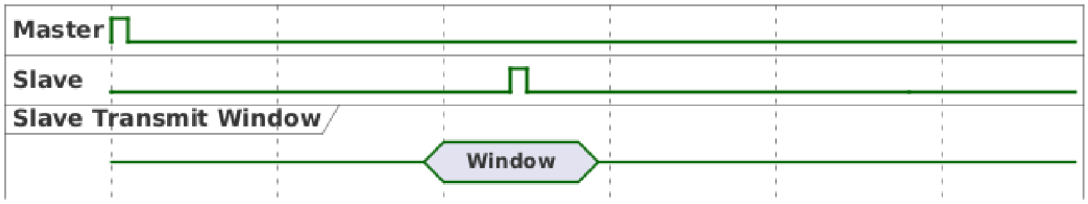

Figure 200–16—Time period for SEND_S

The pulse in the low data rate direction shall have a 4 bits fixed pattern 1001, transmitted as DME symbols using the normal DME symbol rate. Note that the DME signal polarity can vary for each pulse.

The modulation of the high data rate pulse is TBD.

200.8.4 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RFER indicated in 200.7.2.4 is achieved. The received clock signal is expected to be stable and ready for use when training has been completed. The received clock signal is supplied to the PMA Transmit function by received_clock.

200.8.5 MDI, T1

The MDI signals are as specified in 149.4.3, with the following exceptions:

1) The 100Mb/s signaling uses DME instead of PAM4.
2) The 2.5Gb/s signaling uses PAM2 instead of PAM4.
3) The 5Gb/s signaling uses PAM2 instead of PAM4.

200.8.6 MDI, V1

The MDI signals are as specified in 149.4.3, with the following exceptions:

1) The signals are single ended instead of differential.
2) The 100Mb/s signaling uses DME instead of PAM4.
3) The 2.5Gb/s signaling uses PAM2 instead of PAM4.
4) The 5Gb/s signaling uses PAM2 instead of PAM4.

200.8.7 State variables

The 100M+MultiGBASE-T1/V1 state variables are as specified in 149.4.4.

200.8.8 State diagrams

The 100M+MultiGBASE-T1/V1 state diagrams are as specified in 149.4.4.

200.9 Physical Medium Dependent (PMD) sublayer, T1

This subclause defines the electrical characteristics of the PMD and specifies PMD-to-MDI interface tests, for differential balanced pair (T1).

200.9.1 Test modes

The MultiG+100M/100M+MultiGBASE-T1 test modes, including the test fixtures, are as specified in 149.5.1.

Editorial Note: The test mode transmit signals may belong in the PMA Clauses (200.6 and 200.7)

200.9.2 Transmitter electrical specifications

The MultiG+100M/100M+MultiGBASE-T1 transmitter electrical specifications are as specified in 149.5.2, with the exceptions listed in this subclause.

200.9.2.1 Maximum output droop

As specified for MultiGBASE-T1 PHYs in 149.5.2.1.

200.9.2.2 Transmitter linearity

With the transmitter in test mode 4 and using the transmitter test fixture 1 shown in Figure 149–35, the test defined in 120D.3.1.2 shall be performed. The ideal PAM4 level of 1/3 should be used for effective symbol levels of ES1 and ES2. The transmitter SNDR distortion, as specified in 120D.3.1.6, shall exceed 36 dB in 10G+100MBASE-T1 modes.

With the transmitter in test mode 4 and using the transmitter test fixture 1 shown in Figure 149–35, the test defined in 120D.3.1.2 shall be performed. The ideal PAM2 level of TBD should be used for effective symbol levels of ES1 and ES2. The transmitter SNDR distortion, as specified in 120D.3.1.6, shall exceed 32 dB in 5G+100MBASE-T1, and 30 dB in 2.5G+100MBASE-T1 modes.

200.9.2.3 Transmitter timing jitter

The allowable jitter varies with the PHY's data rate. The parameter *J* is used for scaling of the jitter, see Table 200–7.

Table 200–7—Jitter Scaling parameter

PHY type	*J*
10G+100MBASE-T1/V1	1
5G+100MBASE-T1/V1	1.5
2.5G+100MBASE-T1/V1	3

The transmitter timing jitter is measured by capturing the TX_TCLK_175 waveform in both MASTER and SLAVE configurations while in test mode 1 using the transmitter test fixture 2 shown in Figure 149–36. When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the MASTER TX_TCLK_175 jitter relative to an unjittered reference shall be less than *J* ps. The peak-to-peak value of the MASTER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 10**J* ps. See Table 200–7 for the definition of *J*.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the SLAVE TX_TCLK_175 jitter relative to an unjittered reference shall be less than 2**J* ps. The peak-to-peak value of the SLAVE TX_TCLK_175 jitter relative to an unjittered reference shall be less than 20**J* ps.

TX_TCLK_175 jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the capturing device shall be at least 200 MHz (this is equivalent to phase noise integration of the clock over a bandwidth of at least 100 MHz from the carrier frequency). The unjittered reference is a constant clock frequency extracted from each record of captured TX_TCLK_175. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

200.9.2.4 Transmitter power spectral density (PSD) and power level

In test mode 5 (normal operation), the transmit power for the MultiG+100MBASE-T1 PHYs shall be as specified in Table 200–8 and the power spectral density of the transmitter, measured into a 100 Ω load using test fixture 4 shown in Figure 149–38 shall be between the upper and lower masks specified in Equation (200–5) and Equation (200–6). The upper and lower masks for each data rate, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s, are shown in Figure 200–17. See Table 200–1 for the definition of *S*.

.

Table 200–8—Transmit Power - T1

Transmit Rate	Min (dBm	Max (dBm)
10G	-1	2
5G	-1	2
2.5G	-4	-1
100M	-3	0

$$\text{UpperPSD}(f) = \left\{ \begin{array}{ll} P_O & 0 \le f < 600 \times S \\ P_O + 1 - \dfrac{f}{600 \times S} & 600 \times S \le f < 3000 \times S \\ P_O + 8 - \dfrac{f}{250 \times S} & 3000 \times S \le f \le 5500 \times S \end{array} \right\} \text{dBm/HZ} \qquad (200\text{–}5)$$

$$\text{LowerPSD}(f) = \left\{ \begin{array}{ll} P_O & 0 \le f < 600 \times S \\ P_O + 1 - \dfrac{f}{600 \times S} & 600 \times S \le f < 3000 \times S \\ P_O + 8 - \dfrac{f}{250 \times S} & 3000 \times S \le f \le 5500 \times S \end{array} \right\} \text{dBm/HZ} \quad (200\text{–}6)$$

where

P_O is equal to -90 dBm/Hz
f is the frequency in MHz

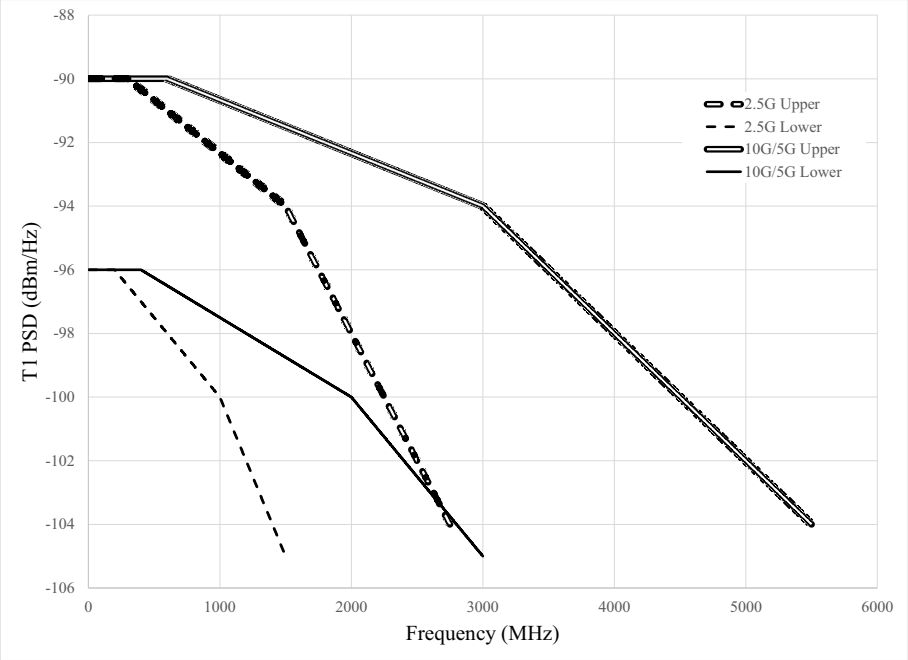

Figure 200–17—T1 MultiGTransmitter Power Spectral Density, upper and lower masks

In test mode 5, the transmit power for the 100M+MultiGBASE-T1 PHY shall be as specified in Table 200–8 and the power spectral density of the transmitter, measured into a 100 Ω load using test fixture 4 shown in Figure 149–38 shall be between the upper and lower masks specified in Equation (200–7) and Equation (200–8). The upper and lower masks are shown in Figure 200–18.

$$\text{UpperPSD}(f) = \left\{ \begin{array}{cc} P_O & 3 \le f < 150 \\ P_O + 15 - \frac{f}{10} & 150 \le f < 260 \\ P_O - 11 & 260 \le f \le 400 \end{array} \right\} \text{dBm/HZ} \quad (200\text{–}7)$$

$$\text{LowerPSD}(f) = \left\{ \begin{array}{cc} P_O - 6 - \frac{90-f}{3} & 45 \le f < 90 \\ P_O - 6 - \frac{f-90}{4} & 90 \le f \le 150 \end{array} \right\} \text{dBm/HZ} \quad (200\text{–}8)$$

where

P_O is equal to –79 dBM/Hz
f is the frequency in MHz

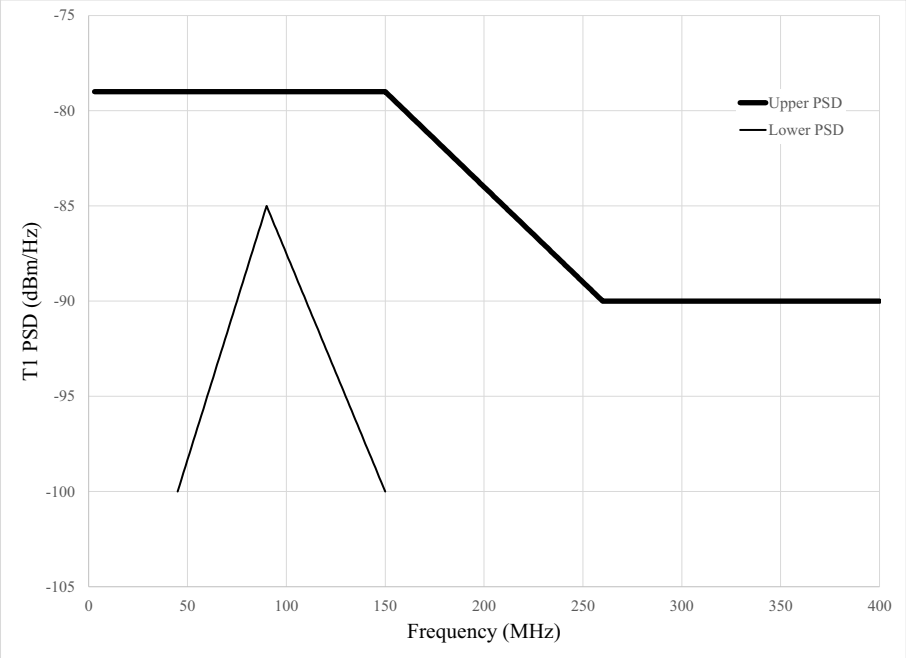

Figure 200–18—T1 100M Transmitter Power Spectral Density, upper and lower masks

200.9.2.5 Transmitter peak differential output

When transmitting at a data rate of 10G and measured with 100 Ω termination, the transmit differential signal at the MDI shall be less than 1.3 V peak-to-peak. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

When transmitting at a data rate of 5G and measured with 100 Ω termination, the transmit differential signal at the MDI shall be less than 1.0 V peak-to-peak. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

When transmitting at a data rate of 2.5G and measured with 100 Ω termination, the transmit differential signal at the MDI shall be less than 0.7 V peak-to-peak. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

When transmitting at a data rate of 100M and measured with 100 Ω termination, the transmit differential signal at the MDI shall be less than TBD V peak-to-peak. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

200.9.2.6 Transmitter clock frequency

As specified for MultiGBASE-T1 PHYs in 149.5.2.6.

200.9.3 Receiver electrical specifications

The MultiG+100M/100M+MultiGBASE-T1 receiver electrical specifications are as specified in 149.5.3, with the exception listed in this sub-clause.

The cabling used is according to 200.12, instead of 149.7.

200.9.3.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 200.9.2 and have passed through a link specified in 200.12 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link reset completion. This specification can be verified by a frame error ratio less than 7.8×10^{-9} for 800 octet frames with minimum IPG or greater than 220-octet IPG.

200.9.3.2 Alien crosstalk noise rejection

As specified for MultiGBASE-T1 PHYs in 149.5.3.2 with the noise levels specified in Table 200–9.

Table 200–9—Alien crosstalk noise source

PHY type	Noise bandwidth (MHz)	Added noise at MDI (dBm/Hz)
10GBASE-T1	3500	–148
5GBASE-T1	3500	–144
2.5GBASE-T1	1750	–140

200.9.4 MDI

Communication through the MDI is summarized in 149.4.3.1 and 149.4.3.2, with the exceptions listed in 200.8.5 for T1 links.

200.10 Physical Medium Dependent (PMD) sublayer, V1

This subclause defines the electrical characteristics of the PMD and specifies PMD-to-MDI interface tests, for coaxial cables (V1).

200.10.1 Test modes

The test modes described in 149.5.1 shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER.
Editorial Note: The test mode transmit signals may belong in the PMA Clauses 200.6 and 200.7.

200.10.1.1 Test fixtures

The following fixtures, or their equivalents, as shown in Figure 200–19, Figure 200–20, Figure 200–21, and Figure 200–22, in stated respective tests, are defined for measuring the transmitter specifications for data communication only.

.

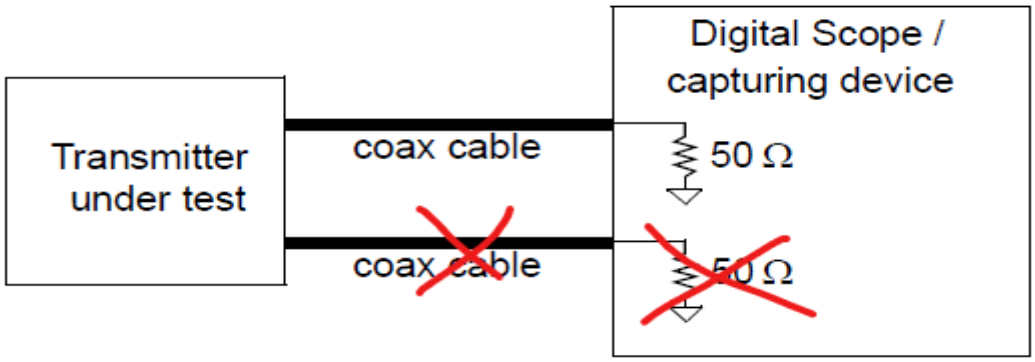

Figure 200–19—Transmitter test fixture 1 for transmitter droop measurement and

.

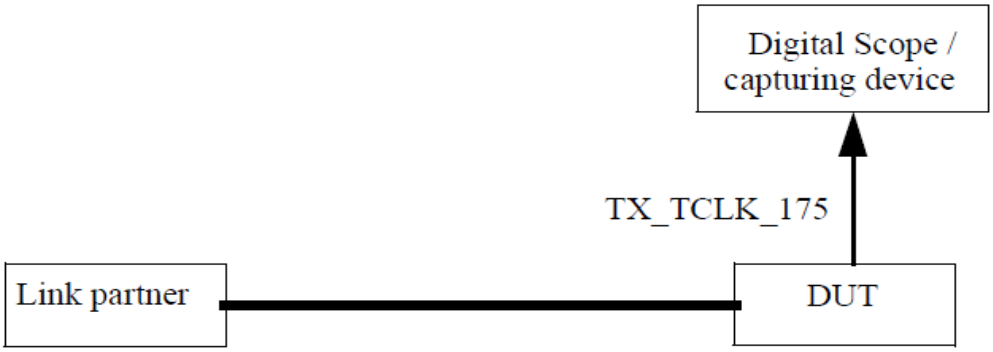

Figure 200–20—Transmitter test fixture 2 for MASTER and SLAVE clock jitter measurement

.

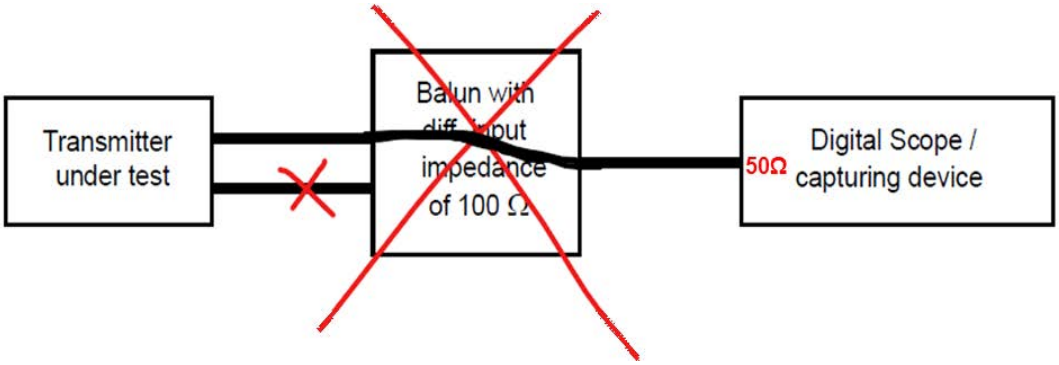

Figure 200–21—Transmitter test fixture 3 for MDI jitter measurement

.

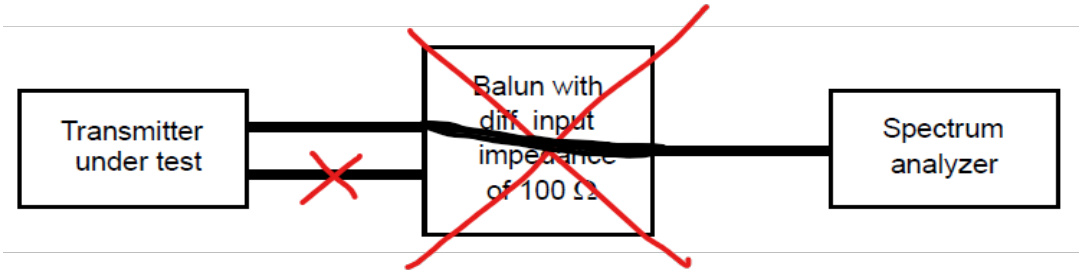

Figure 200–22—Transmitter test fixture 4 for power spectral density measurement and

200.10.2 Transmitter electrical specifications

The PMA provides the Transmit function specified in 200.7.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be AC-coupled, i.e., it shall present a high DC common-mode impedance at the MDI. There may be various methods for AC-coupling in actual implementations.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 50 Ω resistive differential load connected to each transmitter output. Transmitter electrical tests are specified with a load tolerance of ± 0.1%.

200.10.2.1 Maximum output droop

With the transmitter in test mode 6 and using the transmitter test fixture 1 shown in Figure 200–19, the magnitude of both the positive and negative droop shall be less than 15%, measured with respect to an initial value at 4 ns after the zero crossing and a final value at 16 ns after the zero crossing (12 ns period).

200.10.2.2 Transmitter linearity

The transmitter linearity shall meet the requirement in 200.9.2.2.

200.10.2.3 Transmitter timing jitter

The transmitter timing jitter shall meet the requirement in 200.9.2.3.

200.10.2.4 Transmitter power spectral density (PSD) and power level

In test mode 5 (normal operation), the transmit power for the MultiG+100MBASE-V1 PHYs shall be as specified in Table 200–10 and the power spectral density of the transmitter, measured into a 100 Ω load using test fixture 4 shown in Figure 149–38 shall be between the upper and lower masks specified in Equation (200–5) and Equation (200–6)

where

P_O is equal to -93 dBm/Hz

The upper and lower masks for each data rate, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s, are shown in Figure 200–23. See Table 200–1 for the definition of *S*.

.

Table 200–10—Transmit Power - V1

Transmit Rate	Min (dBm	Max (dBm)
10G	-4	-1
5G	-4	-1
2.5G	-7	-4
100M	-6	-3

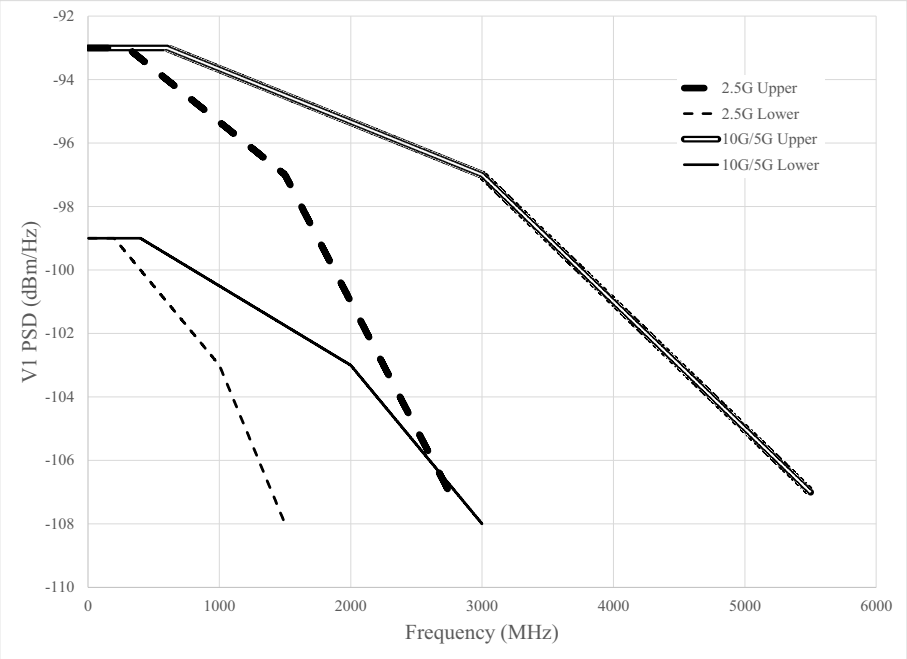

Figure 200–23—V1 MultiGTransmitter Power Spectral Density, upper and lower masks

In test mode 5, the transmit power for the 100M+MultiGBASE-V1 PHY shall be as specified in Table 200–8 and the power spectral density of the transmitter, measured into a 100 Ω load using test fixture 4 shown in Figure 149–38 shall be between the upper and lower masks specified in Equation (200–7) and Equation (200–8).

where

P_O is equal to –82 dBM/Hz
f is the frequency in MHz

The upper and lower masks are shown in Figure 200–24

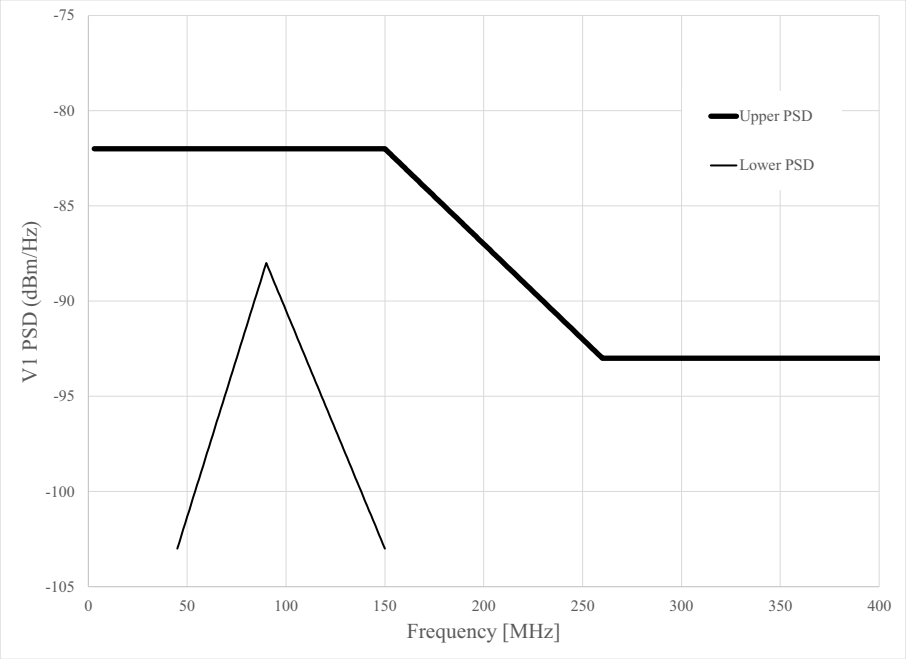

Figure 200–24—V1 100M Transmitter Power Spectral Density, upper and lower masks

200.10.2.5 Transmitter peak output

When transmitting at a data rate of 10G and measured with 50 Ω termination, the transmit differential signal at the MDI shall be less than 0.65 V peak-to-peak. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

When transmitting at a data rate of 5G and measured with 50 Ω termination, the transmit differential signal at the MDI shall be less than 0.5 V peak-to-peak. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

When transmitting at a data rate of 2.5G and measured with 50 Ω termination, the transmit differential signal at the MDI shall be less than 0.35 V peak-to-peak. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

When transmitting at a data rate of 100M and measured with 50 Ω termination, the transmit differential signal at the MDI shall be less than TBD V peak-to-peak. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

200.10.2.6 Transmitter clock frequency

As specified for MultiGBASE-T1 PHYs in 149.5.2.6.

200.10.3 Receiver electrical specifications

The PMA provides the Receive function specified in TBD in accordance with the electrical specifications of this clause using cabling that is within the limits specified in 200.13.

200.10.3.1 Receiver input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 200.7.2 and have passed through a link specified in 200.13 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link reset completion. This specification can be verified by a frame error ratio less than 7.8×10^{-9} for 800 octet frames with minimum IPG or greater than 220-octet IPG.

200.10.3.2 External noise rejection

External noise rejection is TBD.

200.10.4 MDI

Communication through the MDI is summarized in 149.4.3.1 and 149.4.3.2, with the exceptions listed in 200.8.6 for V1 links.

200.11 Management interface

200.12 Link segment characteristics, -T1

2.5G+100MBASE-T1, 5G+100MBASE-T1, and 10G+100MBASE-T1 are designed to operate over a single shielded balanced pair of conductors that meet the requirements specified in this sub clause. The single shielded balanced pair of conductors supports an effective data rate of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s in one direction and simultaneously 100 Mb/s in the other direction. The term link segment used in this clause refers to a single balanced pair of conductors (cable or backplane). Full duplex operation at the logical interface of XGMII is supported.

200.12.1 Link transmission parameters

The transmission characteristics for the MultiG+100M/100M+MultiGBASE-T1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

200.12.1.1 Insertion loss

The insertion loss of each MultiG+100MBASE-T1 link segment shall meet the values determined using Equation (200–9).

$$Insertion\ loss(f) \leq -0.0015 + 0.001325f + 0.3645\sqrt{f} + \frac{1.1785}{\sqrt{f}} (\text{dB}) \qquad (200\text{–}9)$$

where

f is the frequency in MHz; $3 \leq f \leq F_{max}$

Fmax is given by Equation (200–10).

$$F_{max} = \begin{cases} 2\text{Gb/s} & \text{for 2.5 Gb/s} \\ 4\text{Gb/s} & \text{for 5 Gb/s and 10 Gb/s} \end{cases} \quad (200–10)$$

The Insertion loss is illustrated in Figure 200–25.

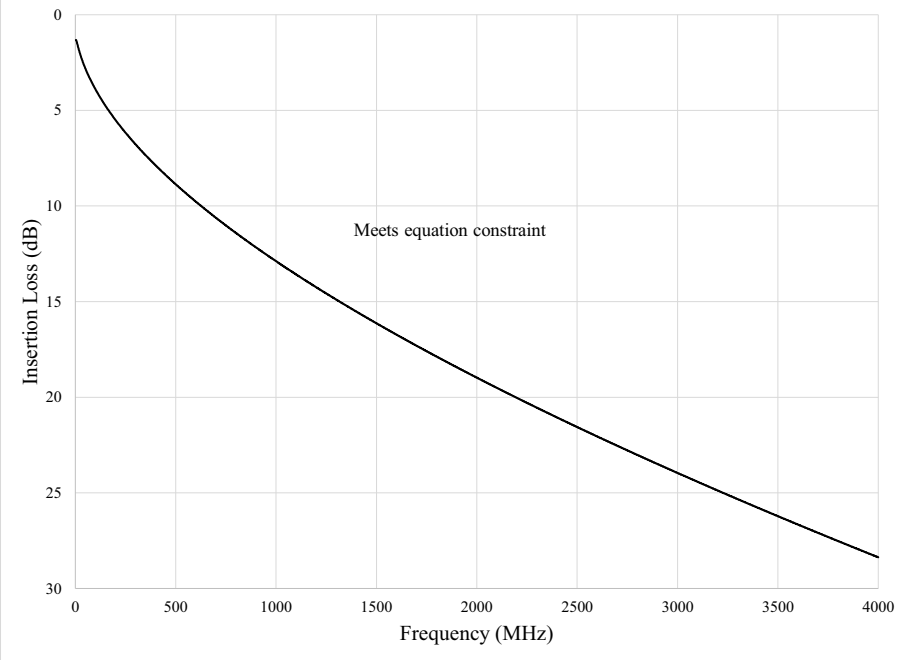

Figure 200–25—Insertion loss using Equation (200–9) for T1 and V1

200.12.1.2 Differential characteristic impedance

The nominal differential characteristic impedance of the link segment is 100 Ω.

200.12.1.3 Return loss

The return loss of each MultiG+100M/100M+MultiGBASE-T1 link segment shall meet the values determined using Equation (200–11).

(200–11)

where

f is the frequency in MHz; $1 \le f \le 4000$

$$Return\ Loss(f) \geq \begin{cases} 18 & 1 \leq f < 400 \\ 16.5 - 11.5\log_{10}\left(\frac{f}{550}\right) & 400 \leq f < 3000 \\ 8 & 3000 \leq f < 4000 \end{cases} (\text{dB})$$

The Return loss is illustrated in Figure 200–26.

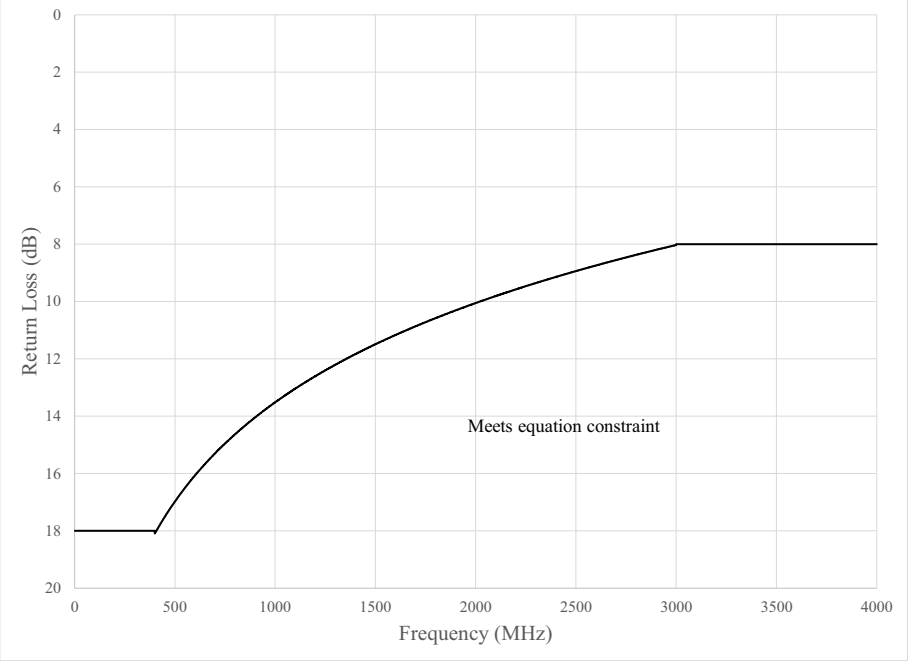

Figure 200–26—IReturn loss using Equation (200–11) for T1 and V1

200.12.1.4 Coupling attenuation

The coupling attenuation of each MultiG+100M/100M+MultiGBASE-T1 link shall be as specified in 149.7.1.4.

200.12.1.5 Screening attenuation

The screening attenuation of each MultiG+100M/100M+MultiGBASE-T1 link shall be as specified in 149.7.1.5.

200.12.1.6 Maximum link delay

The maximum link delay of each MultiG+100M/100M+MultiGBASE-T1 link shall be TBD.

200.12.2 Coupling parameters between link segments

The coupling parameters between link segments shall be as specified in 149.7.2.

200.12.2.1 Power sum alien near-end crosstalk (PSANEXT)

The PSANEXT shall be as specified in 149.7.2.1.

200.12.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

The PSAACRF shall be as specified in 149.7.2.2.

200.13 Link segment characteristics, -V1

2.5G+100MBASE-V1, 5G+100MBASE-V1, and 10G+100MBASE-V1 are designed to operate over a single coaxial cable that meet the requirements specified in this subclause. The single coaxial cable supports an effective data rate of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s in one direction and 100Mb/s in the other direction. The term link segment used in this clause refers to a coaxial cable. Full duplex operation at the logical interface of XGMII is supported.

200.13.1 Link transmission parameters

The transmission characteristics for the MultiG+100MBASE-V1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

200.13.1.1 Insertion loss

The insertion loss of each MultiG+100M/100M+MultiGBASE-V1 link segment shall meet the values determined using Equation (200–9).

200.13.1.2 Single ended characteristic impedance

The nominal characteristic impedance of the link segment is 50 Ω.

200.13.1.3 Return loss

The return loss of each MultiG+100M/100M+MultiGBASE-V1 is link segment shall meet the values determined using Equation (200–11).

200.13.1.4 Coupling attenuation

The coupling attenuation is not defined for coaxial cables.

200.13.1.5 Screening attenuation

Where coaxial cabling is used, the minimum screening attenuation for a link segment is TBD dB for all frequencies between 30 MHz and Fmax MHz. Screening attenuation is tested as specified in IEC 62153-4-7 using triaxial tube-in-tube method. Additional screening attenuation test methodologies are defined in Annex 149A.

200.13.1.6 Maximum link delay

The maximum link delay of each MultiG+100M/100M+MultiGBASE-V1 link shall be TBD.

200.13.2 Coupling parameters between link segments

200.13.2.1 Power sum alien near-end crosstalk (PSANEXT)

The power sum ANEXT loss between a disturbed link segment and the disturbing link segment shall meet the values determined using Equation (TBD).

PSANEXT loss(f)>TBD (dB) (TBD)

where

f is the frequency in MHz; $1 \leq f \leq 4000$

The PSANEXT loss is illustrated in Figure TBD.

200.13.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

The power sum AACRF loss between a disturbed link segment and the disturbing link segment shall meet the values determined using Equation (TBD).

PSANEXT loss(f)>TBD (dB) (TBD)

where

f is the frequency in MHz; $1 \leq f \leq 4000$

The PSANEXT loss is illustrated in Figure TBD.

200.14 MDI specification, T1

200.14.1 MDI connectors

The MDI connectors are as specified in 149.8.1.

200.14.2 MDI electrical specification

200.14.2.1 MDI return loss

The differential impedance at the MDI for each transmit/receiver channel shall be such that any reflection due to signals incident upon the MDI from the cabling relative to the incident signal are per the relationship shown in Equation (200–12). For balanced cabling, a nominal differential characteristic is impedance of 100 Ω is used, and for coaxial cabling a nominal characteristic impedance of 50 Ω is used.

$$MDI\_Return\_Loss(f) \leq \begin{cases} 18 + 20\log_{10}\left(\frac{f}{50}\right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13\log_{10}\left(\frac{f}{400}\right) & 400 \leq f < Fmax \end{cases} \text{(dB)} \qquad \text{(200–12)}$$

where

f is the frequency in MHz; $1 \leq f \leq F_{max}$

Fmax is given by Equation (200–10).

For MultiG+100M/100M+MultiGBASE-T1 the maximum applicable frequency, *Fmax*, for the MDI return loss is 4000 MHz.
Note: Fmax should scale with baud rate once the transmit signals are established.

The MDI return loss for 10G+100MBASE-T1 and 100M+10GBASE-T1 is illustrated in Figure 200–27.

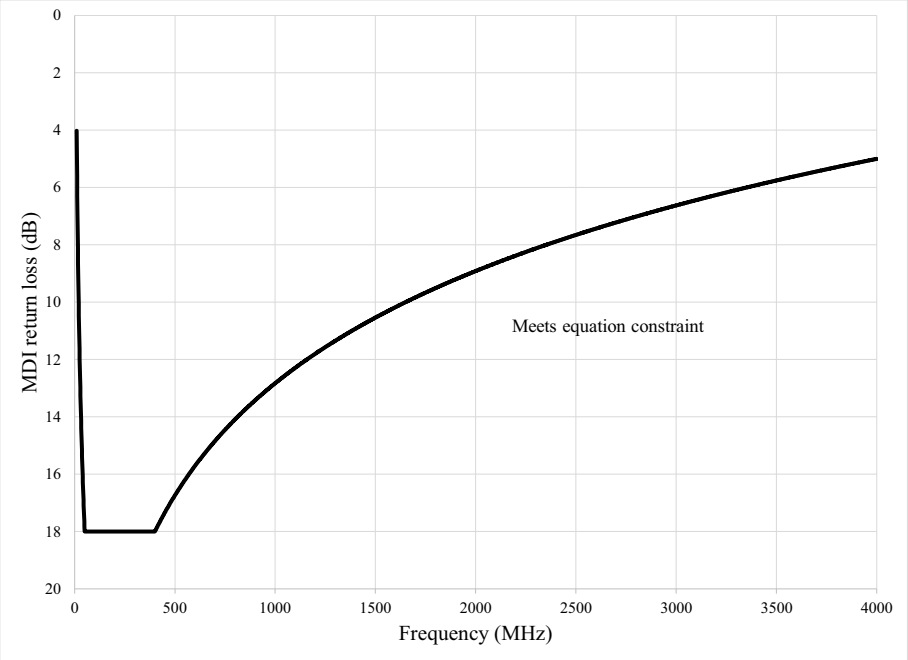

Figure 200–27—MDI return loss using Equation (200–12)

200.14.3 MDI fault tolerance

The MDI fault tolerance shall comply with 96.8.3.

200.15 MDI specification, V1

200.15.1 MDI connectors

Where coaxial cabling is used, the mechanical interface to the coaxial cabling is a single pin connector with a shield. Further specification of the mechanical interface is beyond the scope of this standard.

200.15.2 MDI electrical specification

200.15.2.1 MDI return loss

The MDI return loss for coax cables is as specified in 200.14.2.1.

200.15.3 MDI fault tolerance

The MDI fault tolerance shall comply with 96.8.3.

200.16 Environmental specifications

The environmental specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.

200.16.1 General safety

The general safety specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.1.

200.16.2 Network safety

The network safety specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.2.

200.16.2.1 Environmental safety

The environmental safety specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.2.1.

200.16.3 Electromagnetic compatibility

The electromagnetic compatibility safety specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.2.2.

200.17 Delay constraints

The delay constraints for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.10 with the exceptions and extensions in this sub-clause.

The delay limits for 100Mb/s low speed direction are TBD.

200.18 Protocol implementation conformance statement (PICS) proforma for Clause 200, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1[4]

200.18.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 200, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

[4]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

200.18.2 Identification

200.18.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

200.18.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3xx-202x, Clause 200, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3xx-202x.)	

Date of Statement	

200.18.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] No [ ]
					Yes [ ]

200.18.4 PICS proforma tables for Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1,

10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1

200.18.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ]
					Yes [ ] No [ ]
					Yes [ ] No [ ] N/A [ ]

200.18.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] N/A [ ]
					Yes [ ] No [ ] N/A [ ]