200. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100M+2.5GMBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GMBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1

200.1 Overview

May be added by Editor based on project details.

200.1.1 Nomenclature

May be added by Editor based on project details. In order to efficiently describe the three PHYs, the nomenclature MultiG is used to abbreviate 2.5G/5G/10G when referring to the set of PHYs.

200.1.2 PHY/PMD types

200.1.3 Relationship of MultiG+100M/100M+MultiGBASE-T1/V1 to other standards

May be added by Editor based on project details.

200.1.4 Operation of MultiG+100M/100M+MultiGBASE-T1/V1

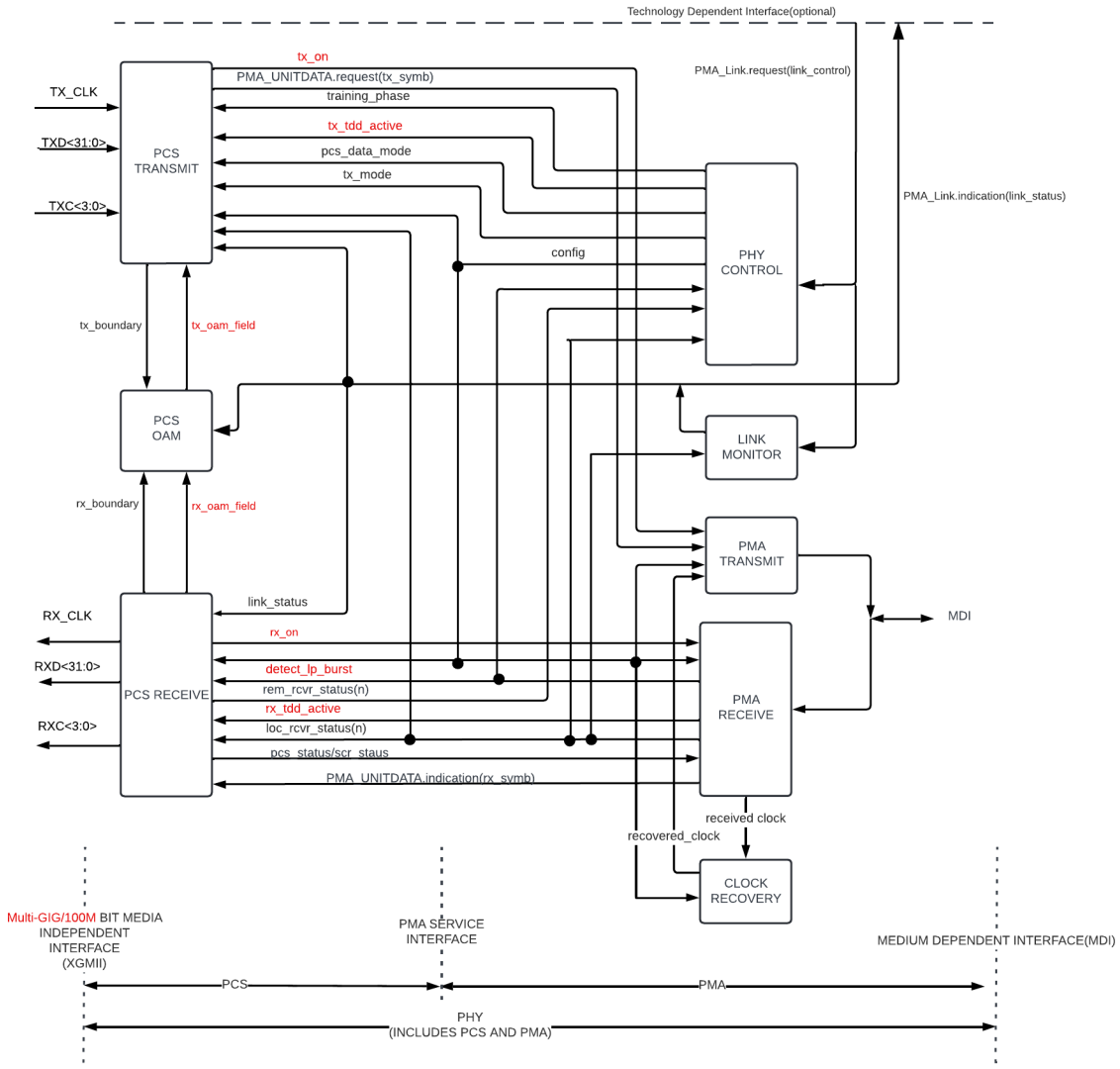


Figure 200-2 --- Functional block diagram

200.1.4.1 Physical Coding Sublayer (PCS), MultiG+100MBASE-T1/V1

200.1.4.2 Physical Coding Sublayer (PCS), 100M+MultiGBASE-T1/V1

200.1.4.3 Physical Medium Attachment (PMA) sublayer, MultiG+100MBASE-T1/V1

200.1.4.4 Physical Medium Attachment (PMA) sublayer, 100M+MultiGBASE-T1/V1

~~200.1.4.5 EEE Capability~~

May want to include and indicate there is no EEE Capability if it is decided this is not needed/required/desired.

~~200.1.4.6 Link Synchronization~~

200.1.5 Signaling, MultiG+100MBASE-T1/V1

200.1.6 Signaling, 100M+MultiGBASE-T1/V1

200.1.7 Interfaces

200.1.8 Conventions in this clause

200.2 MULTIG+100MBASE-T1/V1 service primitives and interfaces

200.2.1 Technology Dependent Interface

200.2.1.1 PMA_LINK.request

200.2.1.1.1 Semantics of the primitive

200.2.1.1.2 When generated

200.2.1.1.3 Effect of receipt

200.2.1.2 PMA_LINK.indication

200.2.1.2.1 Semantics of the primitive

200.2.1.2.2 When generated

200.2.1.2.3 Effect of receipt

200.2.2 PMA service interface

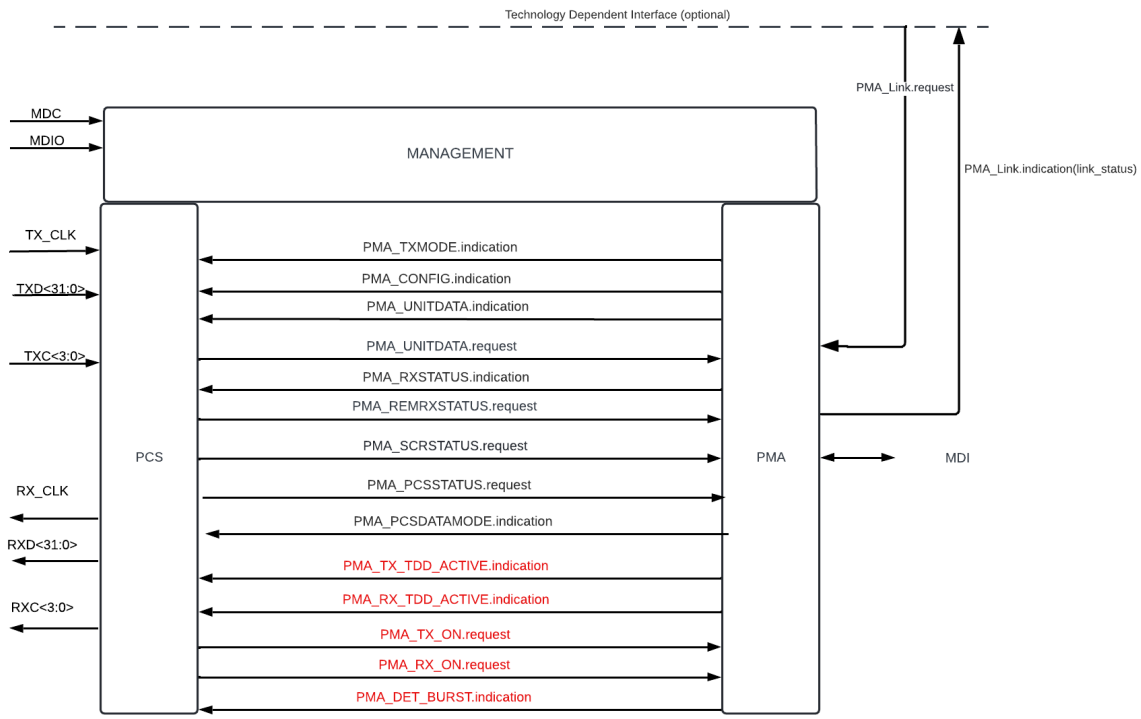


Figure 200-3 MultiG+100M/100M+MultiGBASE-T1/V1 service interface

200.2.2.1 PMA_TXMODE.indication

The transmitter in a MultiGBASE+100M/100M+MultiGBASE-T1/V1 link normally sends over the MDI symbols that represent XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

200.2.2.1.1 Semantics of the primitive

PMA_TXMODE.indication(tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following values of the form:

SEND_N: This value is continuously asserted during transmission of sequences of symbols representing a (XGMII?) data stream in the data mode.

SEND_TS: This value is continuously asserted in case transmission of sequences of symbols representing the TDD symmetric training mode is to take place. MASTER and SLAVE send 3Gsps baud rate with PAM2 TDD training frames.

SEND_TA: This value is continuously asserted in case transmission of sequences of symbols representing the TDD asymmetric training mode is to take place. Master send 3Gsps baud rate with PAM2 TDD training frames. SLAVE send target baud rate of 3Gsps or 6Gsps with PAM2 TDD training frames

SEND_TA_EXT: This value is continuously asserted in case transmission of sequences of symbols representing the TDD asymmetric extended training mode is to take place for SLAVE baud rate of 6Gsps and PAM2/PAM4 modulation. MASTER baud rate is 3Gsps and PAM2 Modulation.

SEND_Z: This value is continuously asserted in case transmission of zero symbols is required

200.2.2.1.2 When generated

As specified for MultiGBASE-T1 PHYs in 149.2.2.1.2

200.2.2.1.3 Effect of receipt

As specified for MultiGBASE-T1 PHYs in 149.2.2.1.3

200.2.2.2 PMA_CONFIG.indication

Each PHY in a MultiG+100M/100M+MultiGBASE-T1/V1 link is capable of operating either as a MASTER PHY (100M+multiGBASE-T1/V1) or as a SLAVE PHY(multiG+100MBASE-T1/V1). PMA_CONFIG MASTER-SLAVE configuration is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup. (MultiG+100MBASE-T1/V1 as MASTER and 100M+multiGBASE-T1/V1 as SLAVE case could be added if the task force decides)

200.2.2.2.1 Semantics of the primitive

PMA_CONFIG.indication(config)

PMA_CONFIG.indication specifies to the PCS and PMA Transmit via the parameter config whether the PHY operates as a MASTER PHY or as a SLAVE PHY. The parameter config can take on one of the following two values of the form

MASTER This value is continuously asserted when the PHY operates as a MASTER PHY.

SLAVE This value is continuously asserted when the PHY operates as a SLAVE PHY.

200.2.2.2.2 When generated

As specified for MultiGBASE-T1 PHYs in 149.2.2.2.2

200.2.2.2.3 Effect of receipt

As specified for MultiGBASE-T1 PHYs in 149.2.2.2.3

200.2.2.3 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 149.3.2.2 (TBD)

200.2.2.3.1 Semantics of the primitive (TBD, Need review)

PMA_UNITDATA request(tx_symb)

During transmission, the PMA_UNITDATA request simultaneously conveys to the PMA via the parameter tx symb the value of the symbols to be sent over the MDI. The tx_symb may take on one of the following (-1, -1/3, +1/3, +1) in normal operation for 10Gbps mode's data payload or extended training's training payload. It may take one of the following {-1,+1} in normal operation for all refresh header and 2.5Gbps and 5Gbps modes' data payload

when zeros are to be transmitted in the following two cases:

1) when PMA_TXMODE indication is SEND Z during PMA training, and

2) pcs_tx_mode is QUIET.

200.2.2.3.2 When generated

The PCS generates PMA_UNITDATA request(tx_symb) synchronously with every transmit clock cycle

200.2.2.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols processed to conform to 149.5.2.(TBD)

200.2.2.4 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx symb parameter from the PMA to the PCS.

200.2.2.4.1 Semantics of the primitive

PMA_UNITDATA indication (rx_symb)

During reception the PMA UNITDATA indication conveys to the PCS via the parameter rx_symb the value of symbols detected on the MDI during each cycle of the recovered clock.

200.2.2.4.2 When generated (need review)

The PMA generates PMA UNITDATA indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the PMA_UNITDATA indication primitive is 3 GHz for 100M+2.5GBASE-T1/V1 and MultiG+100MBASE-T1/V1, 6 GHz for 100M+5GBASE-T1/V1, and 6 GHz for 100M+10GBASE-T1/V1; as governed by the recovered clock.

200.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

200.2.2.5 PMA_SCRSTATUS.request

As specified for MultiGBASE-T1 PHYs in 149.2.2.5

200.2.2.5.1 Semantics of the primitive

As specified for MultiGBASE-T1 PHYs in 149.2.2.5.1

200.2.2.5.2 When generated

As specified for MultiGBASE-T1 PHYs in 149.2.2.5.2

200.2.2.5.3 Effect of receipt

As specified for MultiGBASE-T1 PHYs in 149.2.2.5.3

200.2.2.6 PMA_PCSSTATUS.request

As specified for MultiGBASE-T1 PHYs in 149.2.2.6

200.2.2.6.1 Semantics of the primitive

As specified for MultiGBASE-T1 PHYs in 149.2.2.6.1

200.2.2.6.2 When generated

As specified for MultiGBASE-T1 PHYs in 149.2.2.6.2

200.2.2.6.3 Effect of receipt

As specified for MultiGBASE-T1 PHYs in 149.2.2.6.3

200.2.2.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_(*n*)_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not, during each training phase *n* or data mode. Note that loc_rcvr_(*n*)_status is used by the PCS Receive decoding functions. The criteria for setting the parameter loc_rcvr_(n)_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver

and detecting errors during reception of symbol stream. Loc_rcvr_status could be reset to NOT_OK, when the 100M+MultiGBASE-T1/V1 PHY started Asymmetric training or extended Asymmetric training (TBD)

200.2.2.7.1 Semantics of the primitive

As specified for MultiGBASE-T1 PHYs in 149.2.2.7.1

200.2.2.7.2 When generated

As specified for MultiGBASE-T1 PHYs in 149.2.2.7.2

200.2.2.7.3 Effect of receipt

As specified for MultiGBASE-T1 PHYs in 149.2.2.7.3

200.2.2.8 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter rem_rcvr_status is set to the value received in the loc_rcvr_status bit in the InfoField from the remote PHY. The rem_rcvr_status is set to NOT_OK if the PCS has not decoded a valid InfoField from the remote PHY. Rem_rcvr_staus could be reset to NOT_OK, when the MultiG+100M-T1/V1 PHY started Asymmetric training or extended Asymmetric training. (TBD)

200.2.2.8.1 Semantics of the primitive

As specified for MultiGBASE-T1 PHYs in 149.2.2.8.1

200.2.2.8.2 When generated

As specified for MultiGBASE-T1 PHYs in 149.2.2.8.2

200.2.2.8.3 Effect of receipt

As specified for MultiGBASE-T1 PHYs in 149.2.2.8.3

200.2.2.9 PMA_PCSDATAMODE.indication

As specified for MultiGBASE-T1 PHYs in 149.2.2.9

200.2.2.9.1 Semantics of the primitive

As specified for MultiGBASE-T1 PHYs in 149.2.2.9.1

200.2.2.9.2 When generated

As specified for MultiGBASE-T1 PHYs in 149.2.2.9.2

200.2.2.9.3 Effect of receipt

As specified for MultiGBASE-T1 PHYs in 149.2.2.9.3

200.2.2.10 ~~PMA_PCS_RX_LPI_STATUS.request If EEE is supported.~~
PMA_TX_TDD_ACTIVE.indication(tx_tdd_active) (TBD)

This primitive is generated by PMA PHY Control to indicate it exits the SILENT0 state. The parameter tx_tdd_active conveys to the PCS Transmit function that the PCS shall start to send PMA training or data frames at the proper time.

200.2.2.10.1 Semantics of the primitive

PMA_TX_TDD_ACTIVE.indication(tx_tdd_active)

PMA_TX_TDD_ACTIVE.indication specifies to PCS Transmit via the parameter tx_tdd_active that the PCS shall start TDD cycles.

200.2.2.10.2 When generated

The MASTER and SLAVE shall set this bit to TRUE when the PHY control state enters the TRAINING state.

200.2.2.10.3 Effect of receipt

The MASTER(100M+MultiGBASE-T1/V1) PHY PCS shall start the transmission right away. The SLAVE(MultiG+100MBASE-T1/V1) PHY PCS shall start the transmission with certain delay after the last bit of the MASTER burst appearing on the SLAVE MDI input. (TBD)

200.2.2.11 ~~PMA_PCS_TX_LPI_STATUS.request If EEE is supported.~~

PMA_RX_TDD_ACTIVE.indication(rx_tdd_active) (TBD)

This primitive is generated by PMA Receive to indicate it has achieved loc_SNR_Margin=OK. The parameter rx_tdd_active conveys to the PCS Receive function that the PCS shall perform frame synchronization or RS-FEC data decoding.

200.2.2.11.1 Semantics of the primitive

PMA_RX_TDD_ACTIVE.indication(rx_tdd_active)

PMA_RX_TDD_ACTIVE.indication specifies to PCS Receive via the parameter rx_tdd_active that the PCS shall start receive TDD cycles.

200.2.2.11.2 When generated

The MASTER and SLAVE shall set this bit to TRUE when the loc_SNR_margin is OK

200.2.2.11.3 Effect of receipt

In training mode, PCS receiving should start frame synchronization and infofield decoding. In data mode, PCS receiving should decode RS-FEC frames

200.2.2.12 ~~PMA_ALERTDETECT.indication If EEE is supported.~~ PMA_TX_ON.request(tx_on) (TBD)

This primitive is generated by PCS Transmit to indicate to PMA Transmit the burst transmission has started

200.2.2.12.1 Semantics of the primitive

PMA_TX_ON.request(tx_on)

PMA_TX_ON.request specifies to PMA Transmit via the parameter tx_on that the PCS has started its transmission of training or data mode frames. Set to FALSE when the PCS stops its transmission.

200.2.2.12.2 When generated

PCS None Zero transmission is started(TBD)

200.2.2.12.3 Effect of receipt

PMA turn on Transmitter(TBD)

200.2.2.13 PMA_RX_ON.request(rx_on) (TBD)

This primitive is generated by PCS Receive to indicate it is ready to receive training or data frames. The parameter rx_on conveys to the PMA Receive function that the PCS Receive is ready

200.2.2.13.1 Semantics of the primitive

PMA_RX_ON.request(rx_on)

PMA_RX_ON.request specifies to PMA Receive via the parameter rx_on that the PCS is ready to receive training or data mode frames. Set to FALSE when the PCS stops receiving frames.

200.2.2.13.2 When generated

PCS Receive is ready to receive training payload or data mode FEC frames

200.2.2.13.3 Effect of receipt

PMA Receive shall send rx_symb to PCS Receive.

200.2.2.14 PMA_DET_LP_BURST.indication(detect_lp_burst) (TBD)

This primitive is generated by PMA Receive to indicate it has detected a burst from Link Partner. The parameter detect_lp_burst conveys to the PCS Receive function and PHY control.

200.2.2.13.1 Semantics of the primitive

PMA_DET_LP_BURST.indication(detect_lp_burst)

PMA_DET_LP_BURST.indication specifies to PCS Receive and PHY Control via the parameter detect_lp_burst that the TDD burst has been detected. Set to FALSE when the PMA detected the burst has ended (PMA could use timer timeout to terminate this detection signal) (TBD).

200.2.2.13.2 When generated

TBD

200.2.2.13.3 Effect of receipt

Used by TDD monitor and PHYC control state diagram.(TBD)

200.3 100M+MultiGBASE-T1/V1 service primitives and interfaces, low speed channel

As specified for MultiG+100MBASE-T1/V1 PHYs in 200.2

Note: the entire 200.3 could be removed, as 200.2 covers both MultiG+100M/100M+MultiGBASE-T1/V1 PHYs.

~~**200.3.1 Technology Dependent Interface**~~

~~**200.3.1.1 PMA_LINK.request**~~

~~**200.3.1.2 PMA_LINK.indication**~~

~~**200.3.2 PMA service interface**~~

~~**200.3.2.1 PMA_TXMODE.indication**~~

~~**200.3.2.2 PMA_CONFIG.indication**~~

~~**200.3.2.3 PMA_UNITDATA.request**~~

~~**200.3.2.4 PMA_UNITDATA.indication**~~

~~**200.3.2.5 PMA_SCRSTATUS.request**~~

~~**200.3.2.6 PMA_PCSSTATUS.request**~~

~~**200.3.2.7 PMA_RXSTATUS.indication**~~

~~**200.3.2.8 PMA_REMRXSTATUS.request**~~

~~**200.3.2.9 PMA_PCSDATAMODE.indication**~~

~~**200.3.2.10 PMA_PCS_RX_LPI_STATUS.request If EEE is supported.**~~

~~**200.3.2.11 PMA_PCS_TX_LPI_STATUS.request If EEE is supported.**~~

~~**200.3.2.12 PMA_ALERTDETECT.indication If EEE is supported.**~~

200.4 Physical Coding Sublayer (PCS) functions, MultiG+100MBASE-T1/V1

200.4.1 PCS service interface (XGMII)

200.4.2 PCS functions

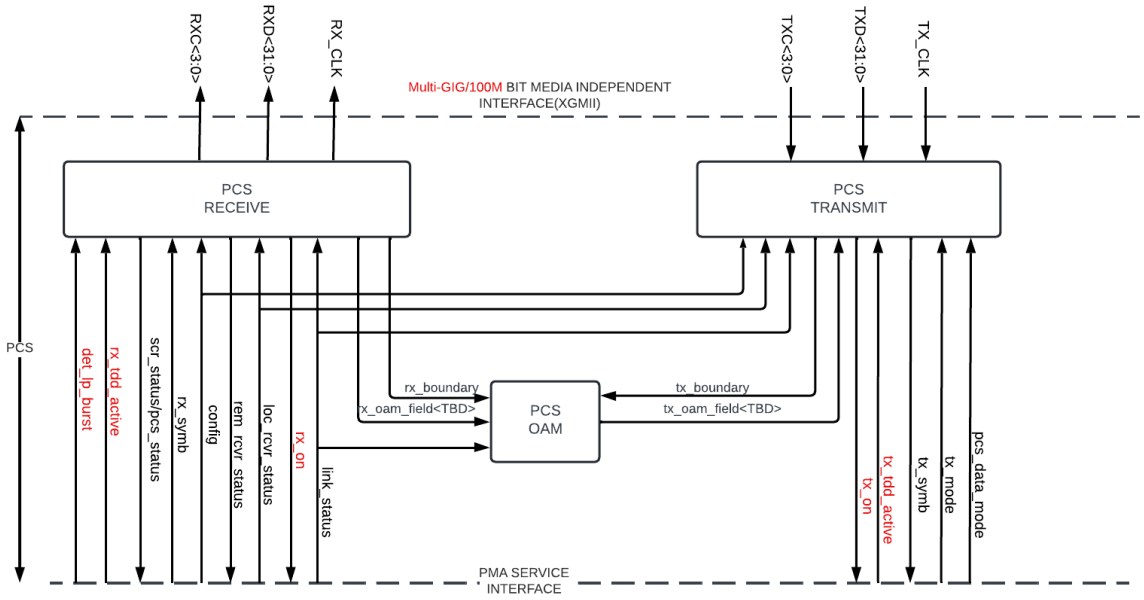


Figure 200-4 PCS reference diagram

200.4.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of following conditions occur:

A. Power on (see 200.4.7.2.2)

B. The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset=TRUE while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

The control and management interface shall be restored to operation within (TBD) ms from the setting of bit 4.2322.15 (TBD)

200.4.2.2 PCS Transmit function

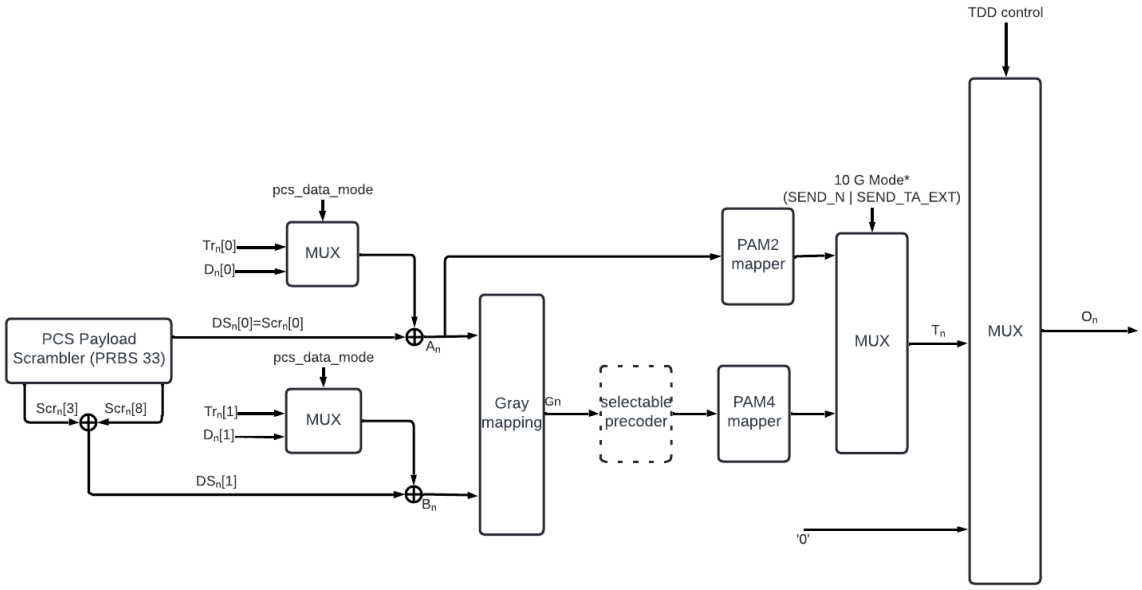


Figure 200-5 PCS Transmit Function block diagram

The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 200-16, and to the PCS Transmit bit ordering in Figure 200-6-1 or Figure 200-6-2.

Dashed rectangles in Figure 200-6-2 and Figure 200-7-1 are used to indicate data path of PAM2 or PAM4 signals. Only one of them shall be chosen for a particular operational speed mode. Dashed rectangles in Figure 200-16 should be removed from final standard as it is related to EEE operation.

When communicating with the XGMII, the MultiG +100MBASE-TI/V1 or 100M+MultiGBASE-T1/V1 PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals.

Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

For 100M+MultiGBASE-T1/V1 PHY (MASTER), after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the PCS Transmit process take 1 group of 15 65B blocks and append a 17-bit OAM field to it, shown in Figure 200-6-1. This forms the input to an (130,124) RS-FEC which adds 48 parity bits. The resulting 1040 bits are then scrambled. These bits are then mapped, one at a time, into a PAM2 symbol. Transmit data-units are sent to the PMA service interface via the PMA UNITDATA.request primitive.

For MultiG+100MBASE-T1/V1 PHY(SLAVE), after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the PCS Transmit process take L groups of 15 65B blocks and append a 1-bit OAM field to each group. This forms the input to an L-interleaved (130,122) RS-FEC superframe which adds L × 64 parity bits, shown in Figure 200-6-2. 25 such superframes are formed for one data payload. L=1 for 2.5Gbps and L=2 for 5Gbps. For 2.5Gbps and 5Gbps PAM2 transmission, the resulting L × 1040 x 25 bits are then scrambled. These bits are then mapped, one at a time, into a PAM2 symbol. L=4 for 10Gbps PAM4 transmission. The resulting L × 1040 x 25 bits are then scrambled. These bits are then mapped, two at a time, into a PAM4 symbol. the transmit data-units are sent to the PMA service interface via the PMA UNITDATA.request primitive.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a PAM2 or PAM4 symbol that is transferred to the PMA via the PMA UNITDATA request primitive.

The operation of the PCS Transmit function is controlled by the PMA TXMODE indication message received from the PMA PHY Control function.

If a PMA_TXMODE. indication message has the value SEND_Z, PCS Transmit shall pass a vector of zeros at each symbol period to the PMA via the PMA_ UNITDATA request primitive.

If a PMA TXMODE.indication message has the value SEND_TS, SEND_TA, or SEND_TA_EXT, PCS Transmit shall generate a sequence (O_n,) defined in 200.4.5.4 to the PMA via the PMA UNITDATA.request primitive.

These code-groups are used for training mode and only transmit the values (-1, +1} in SEND_TS and SEND_TA mode. It could send {-1, -1/3, +1/3, +1} in SEND_TA_EXT mode.

During training mode an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes request for remote transmitter settings. (200.6.2.4).

If a PMA_TXMODE indication message has the value SEND N. the PCS is in the normal mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control.

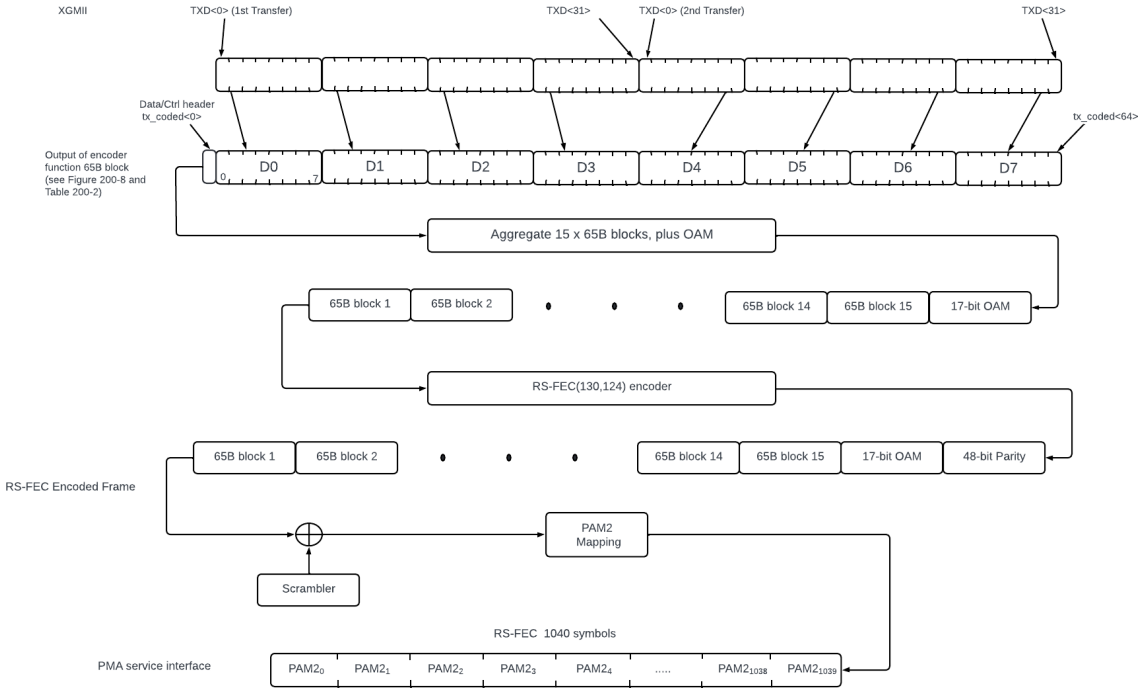
L interleaving and Superframe structure… (TBD, similar to 802.3ch format)

200.4.2.2.1 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into an RS-FEC frame, and vice versa, using a 65B RS-FEC coding scheme. The PAM2/PAM4 PMA training frame synchronization allows establishment of RS-FEC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. ~~During the LPI mode, RS-FEC frame boundaries delimit sleep, wake, refresh, quiet, and alert cycles.~~ The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 200.4.2.2.2.

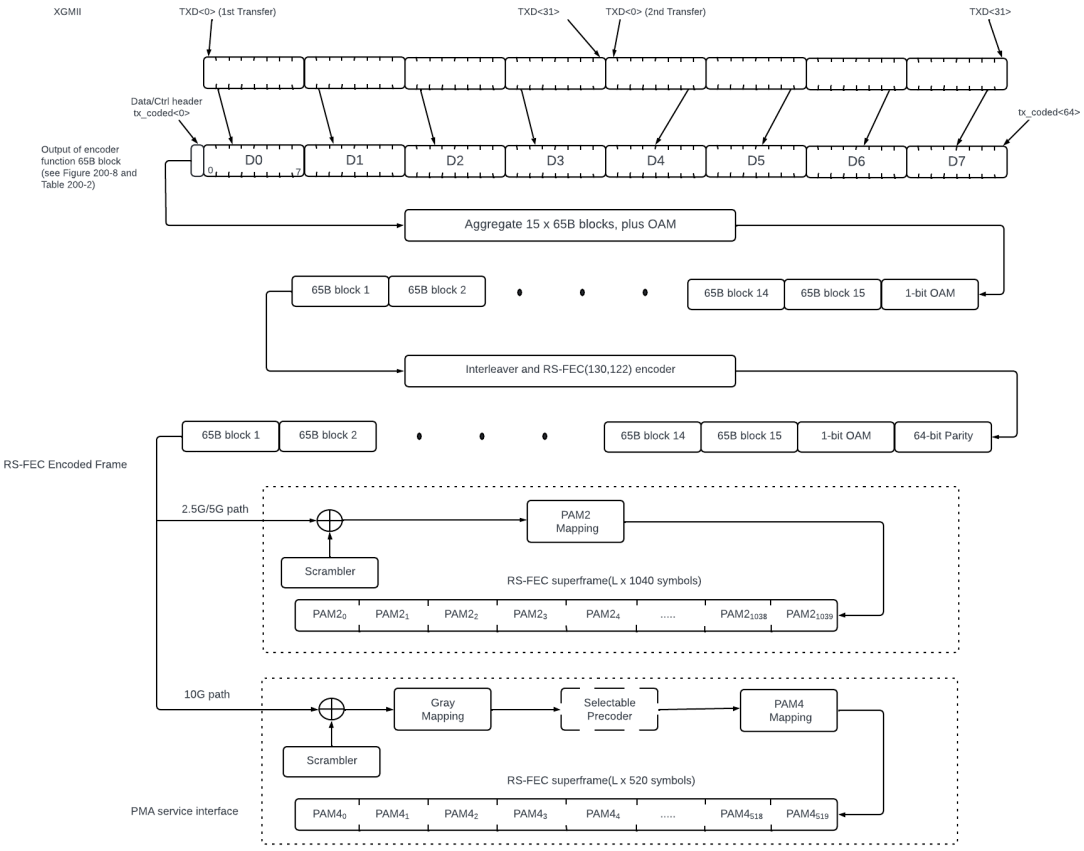
200.4.2.2.2 65B RS-FEC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.
The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 200-6-1 and Figure 200-6-2 for transmit and Figure 200-7-1 and Figure 200-7-2 for receive. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 200.4.2.2.4 for information on how blocks containing control characters are mapped.



Note 1 -- This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters

Figure 200-6-1 MASTER PCS Transmit bit ordering



Note 1 -- This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters
Note 2-- Figure shown for L=1
Note 3-- Either the PAM2 or the PAM4 path is choosen

Figure 200-6-2 SLAVE PCS Transmit bit ordering

200.4.2.2.3 Notation conventions

As specified in MultiGBASE-T1 PHYs in 149.3.2.2.3, with name change to MultiG+ 100M/100M+MultiGBASE-T1/V1

200.4.2.2.4 Block structure

As specified in MultiGBASE-T1 PHYs in 149.3.2.2.4, with name change to MultiG+ 100M/100M+MultiGBASE-T1/V1, and Figure number change to 200-8

200.4.2.2.5 Control codes

~~The same set of control characters are supported by the XGMII and the 2.5G/5G/10GBASE-T1 PCS.~~ All control characters except LPI are supported by both the XGMII and the DM's PCS, as DM does not support EEE. The representations of the control characters are the control codes. The XGMII encodes a control character into an octet (an eight-bit value). The ~~2.5G/5G/10GBASE-T1~~ PCS encodes the start and terminate control characters implicitly by the block type field. The ~~2.5G/5G/10GBASE-T1~~ PCS encodes the ordered set control codes using a combination of the block type field and a four-bit O code for each ordered set. The ~~2.5G/5G/10GBASE-T1~~ PCS encodes each of the other control characters into a seven-bit C code.

The control characters and their mappings to ~~2.5G/5G/10GBASE-T1~~ control codes and XGMII control codes are specified in Table ~~149–2~~. All XGMII control code

Table ~~149–2~~—Control codes for ~~MultiGBASE-T1~~

Control character	Notation	XGMII control code	~~2.5G/5G/10GBASE-T1~~ control code	~~2.5G/5G/10GBASE-T1~~ O code
idle	/I/	0x07	0x00	
~~LPI~~	~~/LI/~~	~~0x06~~	~~0x06~~	
start	/S/	0xFB	Encoded by block type field	
terminate	/T/	0xFD	Encoded by block type field	
error	/E/	0xFE	0x1E	
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0
reserved0		0x1C	0x2D	reserved0
reserved1		0x3C	0x33	reserved1
reserved2		0x7C	0x4B	reserved2
reserved3		0xBC	0x55	reserved3
reserved4		0xDC	0x66	reserved4
reserved5		0xF7	0x78	reserved5
Signal ordered set[1]	/Fsig/	0x5C	Encoded by block type field plus O code	0xF

[1]Reserved for INCITS T11 Fibre Channel use.

Table 200-2 Control codes for MultiG+100M/100M+MultiGBASE-T1/V1

200.4.2.2.6 Ordered sets

As specified in MultiGBASE-T1 PHYs in 149.3.2.2.6, with table name change to 200-2.

200.4.2.2.7 Idle (/I/)

As specified in MultiGBASE-T1 PHYs in 149.3.2.2.7

200.4.2.2.8 ~~LPI (/LI/)~~

As EEE is not supported, LPI related clauses will be removed.

200.4.2.2.9 Start (/S/)

As specified in MultiGBASE-T1 PHYs in 149.3.2.2.9

200.4.2.2.10 Terminate (/T/)

As specified in MultiGBASE-T1 PHYs in 149.3.2.2.10

200.4.2.2.11 Ordered set (/O/)

As specified in MultiGBASE-T1 PHYs in 149.3.2.2.11

200.4.2.2.12 Error (/E/)

The /E/ is sent whenever an /E/ is received. The /E/ allows physical sublayers such as the PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 200.4.7.2.4 for further information.

200.4.2.2.13 Transmit process

The 100M+MultiGBASE-T1/V1 PHY transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. 30 XGMII data transfers are encoded into an RS-FEC frame. It takes 1040 PMA_UNITDATA transfers to send an RS-FEC frame of data. ~~Therefore, for 100M+multiGBASE-T1/V1, transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.~~ ~~(TBD—Rate matching case?)~~

The MultiG+100MBASE-T1/V1 PHY transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. 30 XGMII data transfers are encoded into an RS-FEC frame. For 2.5Gbps and 5Gbps mode, it takes 1040 PMA_UNITDATA PAM2 transfers to send an RS-FEC frame of data. For 10Gbps mode, it takes 520 PMA_UNITDATA PAM4 transfers to send an RS-FEC frame of data. ~~Therefore, for MultiG+100MBASE-T1/V1, transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.~~ ~~(TBD—Rate matching case?)~~

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 200-16). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the transcoder and scrambler. Tx_coded<0> contains the data/ctrl header and the remainder of bits contain the block payload.

200.4.2.2.14 RS-FEC framing and RS-FEC encoder

For 100M+MultiGBASE-T1/V1 transmission, the resulting RS-FEC frame of 15 65B blocks, followed by the 17-bit OAM/Reserved field and 48 parity bits is 1040 bits. See Figure 200-6-1 and 200.4.2.2.17 for details on PCS bit ordering and RS-FEC encoding. The RS-FEC encoding takes the 992-bit vector, consisting of tx_group15x65B, and the 17-bit OAM/Reserved field, and shall generate the 6 8-bit parity symbols(48 bits total).

For MultiG+100MBASE-T1/V1 transmission, the resulting RS-FEC frame of 15 65B blocks, followed by the 1-bit OAM/Reserved field and 64 parity bits is 1040 bits. See Figure 200-6-2 and 200.4.2.2.17 for details on PCS bit ordering and RS-FEC encoding. The RS-FEC encoding takes the 976-bit vector, consisting of tx_group15x65B, and the 1-bit OAM/Reserved field, and shall generate the 8 8-bit parity symbols(64 bits total).

200.4.2.2.15 ~~Reed-Solomon encoder~~ RS-FEC superframe and round-robin interleaving

The interleaver depth L of the transmitter shall be predefined for each speed.

When the defined interleaving depth L=1, there is no interleaving, and the RS-FEC superframe is the same as the RS-FEC frame.

When the defined interleaving depth L>1, the round-robin interleaving scheme as shown in Figure 200-9 shall be applied.

100M+MultiGBASE-T1/V1 transmission only supports L=1 (no interleaving)

2.5G+ 100MBASE-T1/V1 only supports L=1, 5G+ 100MBASE-T1/V1 only supports L=2, 10G+ 100MBASE-T1/V1 only supports L=4

The MultiG+100MBASE-T1/V1 PCS Transmit shall aggregate L RS-FEC input frames into an interleaved RS-FEC input superframe. There are 976 x L bits, or 122 x L Reed-Solomon message symbols in total in the input superframe. The corresponding message symbols are $m_{122xL-1}$, $m_{122*L-2}$, …m_1,m_0. These message symbols are distributed to L RS-FEC encoders. When L>1, each RS-FEC encoder receives one out of every L message symbols from the superframe; otherwise, the RS-FEC encoder operates exactly the same as specified in 200.4.2.2.17

200.4.2.2.16 RS-FEC recombine

The L encoded RS-FEC frames are combined into an interleaved RS-FEC superframe when the PHY operates as a SLAVE PHY. The output symbols are as follows:

$m_{122 \times L-1}$, $m_{122 \times L-2}$, …, m_1, m_0, $p_{1,7}$, …, $p_{L,7}$, …, $p_{1,0}$, …, $p_{L,0}$, where $p_{i,r}$ is the r^{th} parity symbol of the i^{th} encoder.

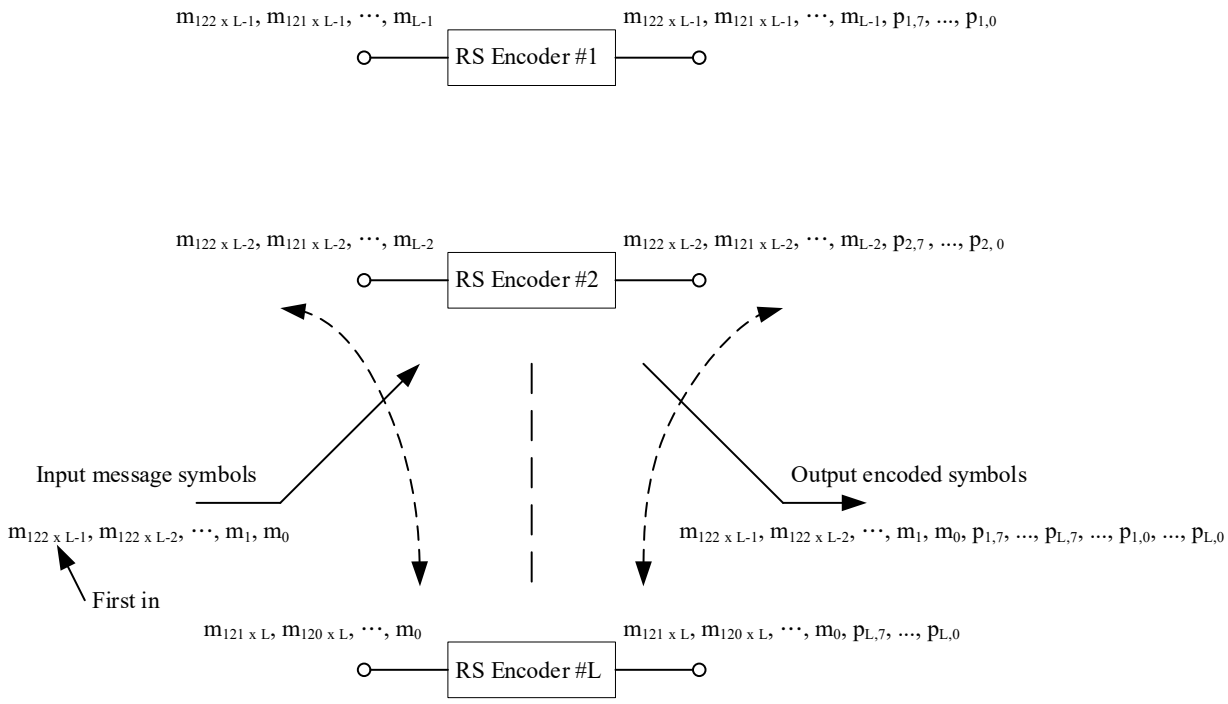


Figure 200–9—Interleaving block diagram with interleaving depth L

200.4.2.2.15~~5~~7 Reed-Solomon encoder

The PCS sublayer employs a Reed-Solomon code operating over the Galois Field GF(2^8) where the symbol size is 8 bits. The encoder processes k 8-bit RS FEC message symbols to generate (130-k) 8-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 130 8-bit RS-FEC symbols. k = 124 and k = 122 are adopted for MASTER and SLAVE, respectively. For the purposes of this clause, a particular Reed-Solomon code is denoted RS(130,k).

The code is based on the generating polynomial given by Equation (200–1).

$$g(x) = (x - \alpha^{130-k-1})(x - \alpha^{130-k-2})...(x - 1) = g_{130-k}x^{130-k} + g_{129-k-1}x^{130-k-1} + ... + g_1x + g_0 \quad (200–1)$$

In Equation (200–1), α, is a primitive element of the finite field defined by the primitive polynomial 0x285 = $x^8 + x^4 + x^3 + x^2 + 1$.

Equation (200–2) defines the message polynomial m(x) whose coefficients are the message symbols m_{k-1} to m_0.

$$m(x) = m_{k-1}x^{129} + m_{k-2}x^{128} + ... + m_1{}^{130-k+1} + m_0x^{130-k} \quad (200–2)$$

Each message symbol m_i is the bit vector ($m_{i,7}$, $m_{i,6}$, …, $m_{i,1}$, $m_{i,0}$), which is identified with the element of the finite field. $m_{i,0}$ is the first bit transmitted. The message symbols are composed of the bits in tx_RSmessage<(8 x k – 1):0>.

For Master,

$m_{i,j}$ = tx_RSmessage<(123 – i) x 8 + j>, for i = 0 to 123, and j = 0 to 7.
tx_RSmessage<991:0> prior to RS-FEC(130,124) encoder is formed as follows:
tx_RSmessage<974:0> = tx_group15x65B<974:0>.
tx_RSmessage<991:975> = OAM_field<16:0>.

For Slave,

$m_{i,j}$ = tx_RSmessage<(121 – i) x 8 + j>, for i = 0 to 121, and j = 0 to 7.
tx_RSmessage<975:0> prior to RS-FEC(130,122) encoder is formed as follows:
tx_RSmessage<974:0> = tx_group15x65B<974:0>.
tx_RSmessage<975> = OAM_field<0>.

The first symbol input to the encoder is m_{k-1}.

Equations (200–3) defines the parity polynomial $p(x)$ whose coefficients are the parity symbols $p_{130-k-1}$ to p_0.

$$p(x) = p_{130-k-1}x^{130-k-1} + p_{130-k-2}x^{130-k-2} + \ldots + p_1x^2 + p_1x + p_0 \qquad (200–3)$$

Each parity symbol p_i is the bit vector ($p_{i,7}$, $p_{i,6}$, …, $p_{i,1}$, $p_{i,0}$), which is identified with the element of the finite field. $p_{i,0}$ is the first bit transmitted.

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This can be computed using the shift register implementation illustrated in Figure 200–10. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0, is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of x, $c_{129} = m_{k-1}$ is transmitted first and the coefficient of the lowest power of x, $c_0 = p_0$ is transmitted last. The first bit transmitted from each symbol is bit 0.

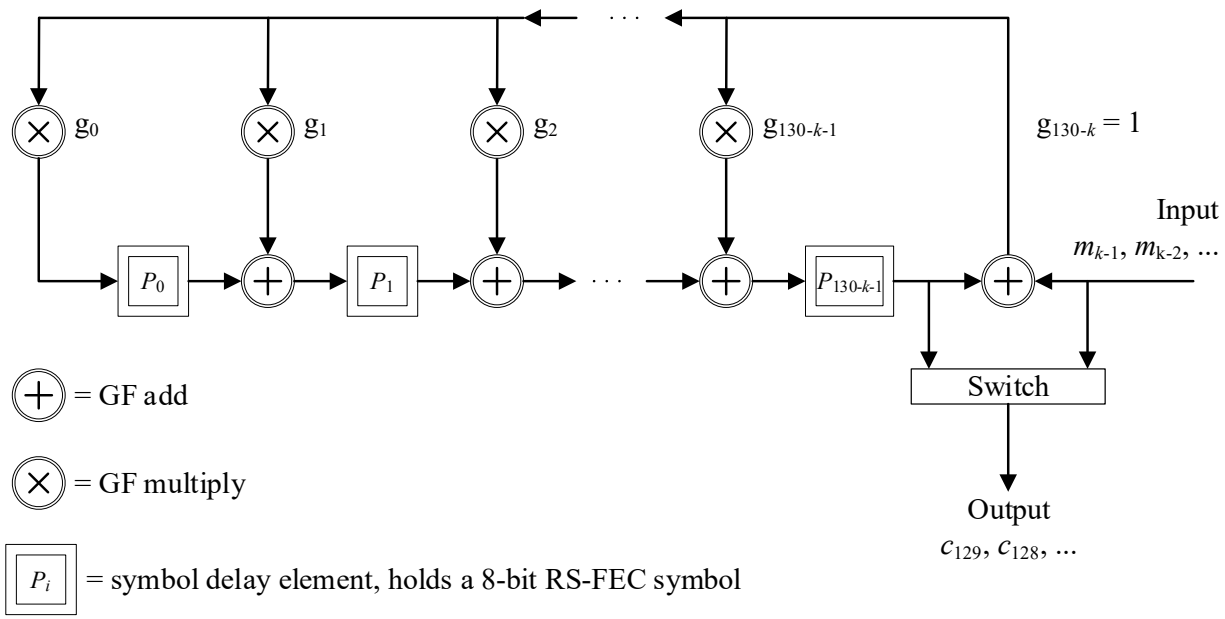


Figure 200–10—Reed-Solomon encoder functional model

The coefficients of the generator polynomial for the code are presented in Table 200–3.

Table 200–3—Coefficients of the generator polynomial g_i (decimal)

i	MASTER RS-FEC(130,124)	SLAVE RS-FEC(130,122)
0	38	24
1	227	200
2	32	173
3	218	239
4	1	54
5	63	81
6	1	11
7	—	255
8	—	1

200.4.2.2.16~~8~~ PCS scrambler

$$A_n = \begin{cases} DS_n[0] \oplus Tr_n[0] & pcs\_data\_mode = FALSE \\ DS_n[0] \oplus D_n[0] & pcs\_data\_mode = TRUE \end{cases}$$

$$B_n = \begin{cases} DS_n[1] \oplus Tr_n[1] & pcs\_data\_mode = FALSE \\ DS_n[1] \oplus D_n[1] & pcs\_data\_mode = TRUE \end{cases}$$

Equation 200-4

200.4.2.2.1~~7~~9 Gray mapping for PAM4 encoding

As specified in MultiGBASE-T1 PHYs in 149.3.2.2.19. Need specify the PHY types for transmit and receive.

200.4.2.2.20 Selectable precoder

Similar to specified in 149.3.2.2.20, with modifications (TBD)

200.4.2.2.21 PAM4 encoding

During PAM4 transmission period, the 10G+100MBASE-T1/V1 PCS transmit process shall encode each precoder output symbol to one of four PAM4 levels as specified in this subclause.

The PAM4 encoded symbols are denoted M(n), where:
n is an index indicating the symbol number.
Each consecutive precoder output symbol, P(n), is mapped to one of four PAM4 levels and assigned to the PAM4 encoder output M(n).
Mapping from the precoder output symbol P(n) to a PAM4 encoded symbol M(n) is as follows:

0 maps to –1,

1 maps to –1/3,

2 maps to +1/3, and

3 maps to +1.

200.4.2.2.22 PAM2 mapping

The 2.5G+100MBASE-T1/V1, 5G+100MBASE-T1/V1, and 100M+MultiGBASE-T1/V1 PHYs PCS transmit process send out PAM2 symbols according to following mapping:

Input bit S_n is mapped to the transmit symbol T_n as follows: if S_n=0 then T_n=+1, if S_n=1 then T_n=-1

The 10G+100MBASE-T1/V1 PHYs PCS transmit process send out PAM2 symbols during its PAM2 transmission period according to the same mapping rules.

~~The 5G PCS transmit process shall encode each output symbol to one of TBD PAM levels as specified in this subclause.~~

~~The 2.5G PCS transmit process shall encode each output symbol to one of 2 PAM2 levels as specified in this subclause.~~

~~0 maps to –1, and~~

~~1 maps to +1.~~

~~**200.4.2.2.18 EEE capability**~~

~~*Only need if supporting EEE*~~

200.4.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 200-17, and the PCS Receive bit ordering in Figure 200-7-1 and Figure 200-7-2 including compliance with the associated state variable as specified in 200.4.7.2.2

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received PAM2 or PAM4 symbols are demapped and descrambling is performed according to rules.

Following descrambling, the L-interleaved RS-FEC superframe is de-interleaved and the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. For 100M+MultiGBASE-T1/V1 PHY, the RS-FEC decoded frame is then separated into a 1-bit OAM field and 15 64B/65B blocks. In each burst, the 25 superframes can form 25-bit, 50-bit and 100-bit OAM field, for 2.5Gbps, 5Gbps, and 10Gbps mode, respectively. For MultiG+100MBASET-T1/V1 PHY, the RS-FEC decoded frame is then separated into a 17-bit OAM field and 15 64B/65B blocks.

This process generates the 64B/65B block vector rx_coded <64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 200-17). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 or PAM4 framing and signals the reliable acquisition of the descrambler state by setting the scr_status parameter of the PMA_ SCRSTATUS.request primitive to OK.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If 40 (TBD, MASTER and SLAVE difference?) consecutive RS-FEC frame errors are detected, the block lock flag is de-asserted. The block lock flag is re-asserted upon detection of a valid RS-FEC frame. When block lock is asserted and hi _rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD 31:0> and RXC <3:0> on the XGMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMARXSTATUS.indication(loc_rcvr_status).
When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA

training frames and conveys received blocks to the PCS Receive process when PHY control is in PCS_DATA state. The PCS Synchronization process sets the block lock flag to indicate whether the PCS has obtained synchronization. The PMA training frame includes a refresh header. It also includes training payload which has an Infofield, inserted in the *N_inf* th bit of the training payload(specified in clause 200.4.5.3). When the PCS Synchronization process is synchronized to this pattern, block lock is asserted.

TDD related description(TBD)

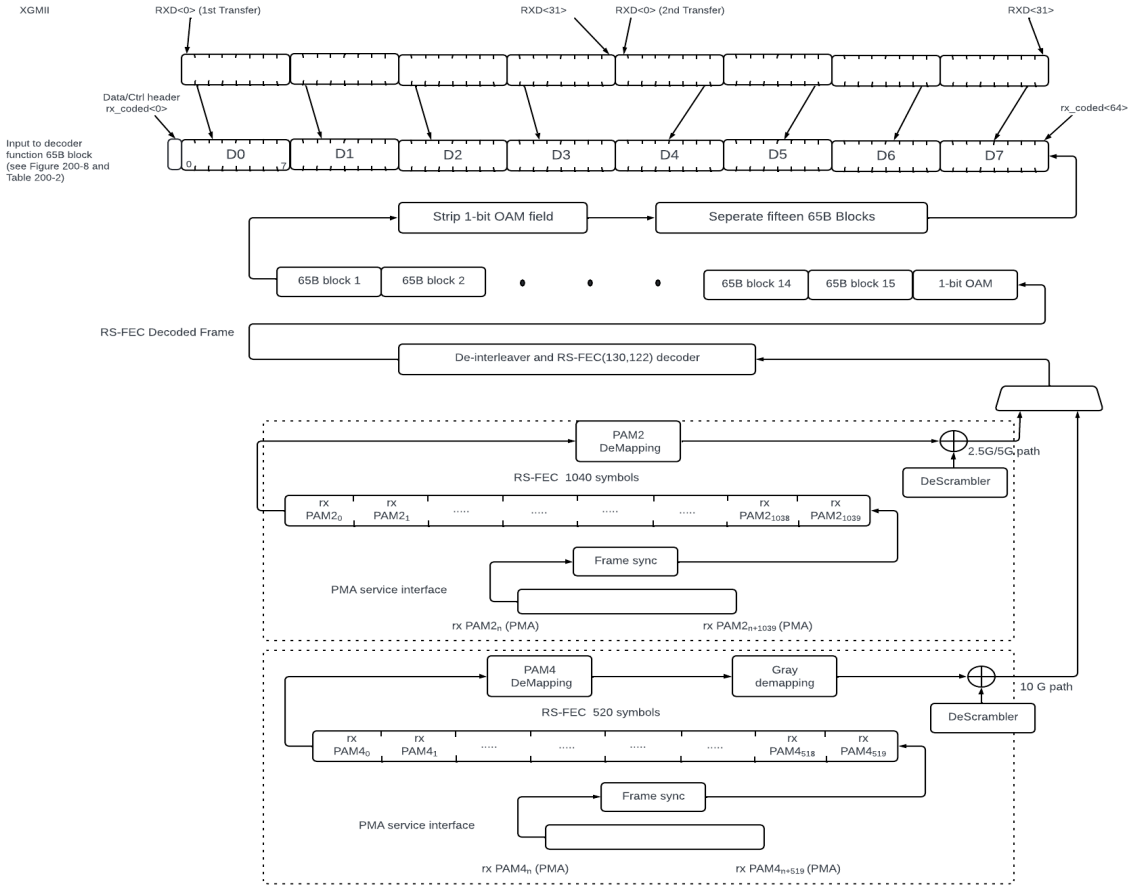
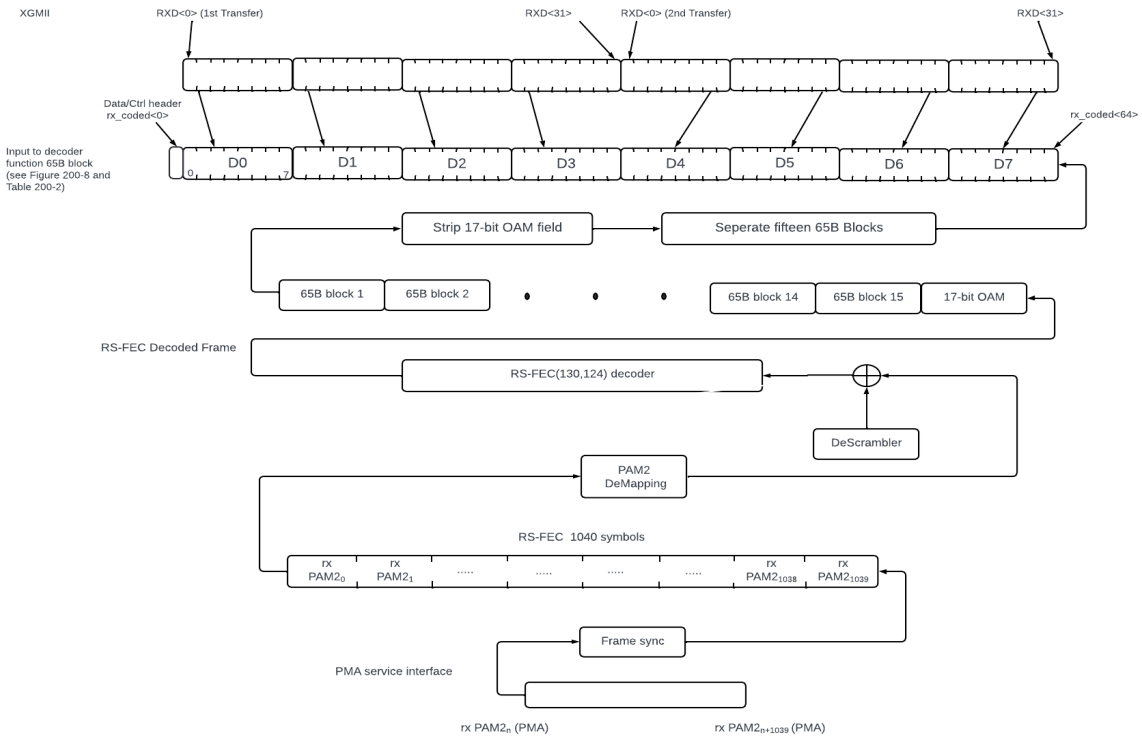


Figure 200-7-1 MASTER PCS Receive bit ordering



Note 1 -- This figure shows the mapping from the a 64B/65B block to a block containing eight data characters to the XGMII

Figure 200-7-2 SLAVE PCS Receive bit ordering

200.4.2.3.1 Frame and block synchronization

When operating in the data mode, MultiG+100MBASE-T1/V1, 100M+2.5GBASE-T1/V1, 100M+5GBASE-T1/V1 PHYs receiving PCS shall form a PAM2 stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from rx_PAM2_0 to rx_PAM2_1039 (see Figure 200-7-1 or Figure 200-7-2). The 100M+10GBASE-T1/V1 receiving PCS shall form a PAM4 stream from PMA_UNITDATA.indication primitive by concatenating requests in order from rx_PAM4_0 to rx_PAM4_519 (see Figure 200-7-1).

The receiving PCS obtains block lock to the PHY frames during training using synchronization sequence and infofield provided in the training frames.

200.4.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process for generation of RXD<31:0> to the XGMII. For side-stream descrambling, the 100M+MultiGBASE-T1/V1 PHY shall employ the receiver descrambler generator polynomial per

Equation(200-6) and the MultiG+100MBASE-T1/V1 PHY shall employ the receiver descrambler generator polynomial per Equation (200-5).

200.4.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exist:

a) The block type field contains a reserved value.
b) Any control character contains a value not in Table 200-2.
c) Any O code contains a value not in Table 200-2.
d) The block contains information from the payload of an invalid RS-FEC frame.

The PCS Receive function shall check the integrity of the RS-FEC parity bits defined in 200.4.2.2.14. If the check fails the RS-FEC frame is invalid
The R_BLOCK_ TYPE of an invalid block is set to E.

200.4.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, the channel, and remote receiver. When the transmit PCS is operating in test-pattern mode it shall transmit TDD bursts as illustrated in Figure 200-6-1 or Figure 200-6-2, with the input to the RS-FEC encoder set to zero and the initial condition of the scrambler set to any non-zero value. This has the same effect as setting the input to the scrambler to zero.

When the receiver PCS is operating in test-pattern mode it shall receive TDD bursts as illustrated in Figure 200-7-1 or Figure 200-7-2. The output of the received descrambled values should be zero. Any nonzero values correspond to receiver bit errors. The output of the RS-FEC decoder should also be zero; however, there is the possibility that the RS-FEC decoder corrected some errors. This mode is further described as test mode 7 (TBD) in 200.5.1 (TBD).

200.4.4 Side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indication message assumes the value MASTER, PCS Transmit shall employ Equation ~~(149~~–5) as transmitter side-stream scrambler generator polynomial.

$$g_M(x) = 1 + x^{13} + x^{33} \quad (149–5)$$

If the PMA_CONFIG.indication message assumes the value of SLAVE, PCS Transmit shall employ Equation ~~(149~~–6) as transmitter side-stream scrambler generator polynomial.

$$g_S(x) = 1 + x^{20} + x^{33} \quad (149–6)$$

An implementation of MASTER and SLAVE PHY side-stream scramblers by linear-feedback shift registers is shown in Figure ~~149~~–11. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

This scrambler, once started during PMA training, shall continue to run uninterrupted ~~during the transition from PAM2 to PAM4.~~ during PMA training frames and data mode frames(including refresh header and payload), and shall stop during QUIET

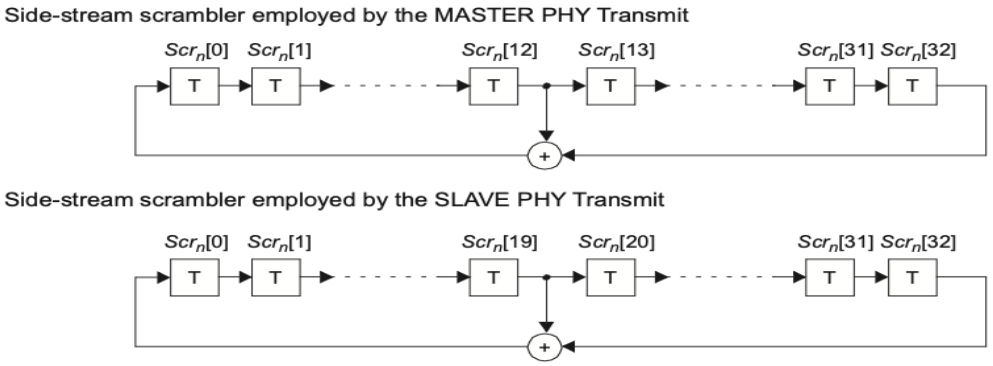


Figure ~~149~~–11—Realization of side-stream scramblers by linear feedback shift registers

200.4.5 PMA training frame

~~This may be able to be a PAM2 signal that is the same for both low speed and high speed. If it is, this subclause would refer to 2xx.4.5.~~

Each PMA training frame includes a refresh header followed by a training payload.

Refresh header (refresh_hdr) is a sequence of PAM2 symbols with length of N_r symbols. Depending on which training phase and speed mode, training payload is a sequence of either PAM2 or PAM4 symbols with length of N_p symbols.

The 33 bit side-stream scrambler(Clause 200.4.4) is used to generate both refresh header and training payload. Once started at the beginning of 1st burst, this scrambler shall continue to run uninterrupted for each symbol during refresh headers and the training payloads and shall stop during the Quiet.

The refresh header and training payload data sequence bits are all 0s, with the exception that a 96 bits infofield is started at *N_inf* th symbol of the training payload. This data sequence *S_t(n)* is scrambled by the 33 bit side-stream scrambler, and it is defined in Equation 200-9.

The infoField is used to exchange messages between link partners during the startup training.

During the 10Gbps extended training mode (Training phase 2), the training payload transmitted by 10G+100MBASE-T1/V1 PHY shall map to PAM4 symbols. In all other cases, the training payload shall map to PAM2 symbols.

Refresh_hdr's and training payload's lengths are described in the 200.4.5.1, in Table 200-4, Table 200-5 and Table 200-6.

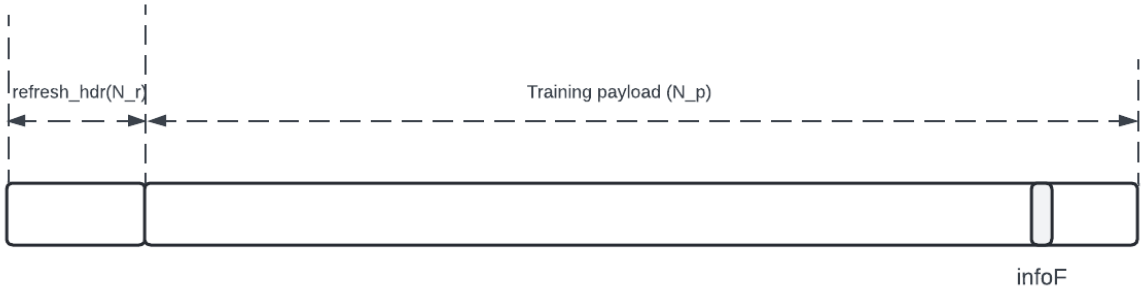


Figure 200-12 PMA Training frame

200.4.5.1 Refresh header and training payload length

tx_mode	refresh_header N_r(symb)	training_payload N_p(symb)
SEND_TS	560	13200
SEND_TA	640	1040
SEND_TA_EXT	640	1040
SEND_N	640	1040

Table 200-4 N_r and N_p value for 100M+MultiGBASE-T1/V1 (MASTER) TX

tx_mode	refresh_header N_r(symb)	training_payload N_p(symb)
SEND_TS	560	13200
SEND_TA	480	26000
SEND_TA_EXT	N/A	N/A
SEND_N	480	26000

Table 200-5 N_r and N_p value for 2.5G+100MBASE-T1/V1 (SLAVE)TX

tx_mode	refresh_header N_r (symb)	training_payload N_p(symb)
SEND_TS	560	13200
SEND_TA	960	52000
SEND_TA_EXT (10G only)	960(10G Only)	52000(10G Only)
SEND_N	960	52000

Table 200-6 N_r and N_p value for 5G/10G + 100MBASE-T1/V1 (SLAVE) TX

200.4.5.2 Refresh header and training payload data bits generation

N_b is the number of bits in the training payload. *N_inf* is the bit position where infoField starts. The first bit start at bit 0.

$$N\_b = \begin{cases} N\_p & \sim(tx\_speed=10Gbps * tx\_mode=SEND\_TA\_EXT) \\ 2 * N\_p & tx\_speed=10Gbps * tx\_mode=SEND\_TA\_EXT \end{cases}$$

Equation: 200-7

$$N\_inf = \begin{cases} N\_b - 256 & \sim(tx\_speed=10Gbps * tx\_mode=SEND\_TA\_EXT) \\ N\_b - 512 & tx\_speed=10Gbps * tx\_mode=SEND\_TA\_EXT \end{cases}$$

Equation: 200-8

$$S\_t_k = \begin{cases} 0 & 0 <= k <= N\_r + N\_inf - 1 \\ InfoField\ (k \bmod N\_r + N\_inf) & N\_r + N\_inf <= k <= N\_r + N\_inf + 95 \\ 0 & N\_r + N\_inf + 96 <= k <= N\_r + N\_b - 1 \end{cases}$$

Equation: 200-9

$$Tr_n[0] = \begin{cases} S\_t_{(n)} & \sim(tx\_speed=10Gbps * tx\_mode= SEND\_TA\_EXT) + (0<= n <= N\_r-1) \\ S\_t_{(2n-N\_r)} & tx\_speed=10Gbps * (tx\_mode= SEND\_TA\_EXT) * (N\_r <= n <= N\_r + N\_p - 1) \end{cases}$$

$$Tr_n[1] = S\_t_{(2n-N\_r+1)} \qquad tx\_speed=10Gbps * (tx\_mode= SEND\_TA\_EXT) * (N\_r <= n <= N\_r + N\_p - 1)$$

Equation: 200-10

***S_t**k* is the PMA training frame bit sequence. It has all 0s, except at the infoField position. *0 <= k <=N_r + N_b -1*

For refresh header, or PAM2 training payload, $Tr_n[0]$ is the same as S_t_n and it is used as scrambler input.

For PAM4 training payload, two bits are grouped into pairs, $Tr_n[0]$ and $Tr_n[1]$, where *n* is an index indicating the symbol number. The pair $\{Tr_n[0], Tr_n[1]\}$ will be used as scrambler input

200.4.5.2.1 Refresh Header encoding (TBD)

200.4.5.3 PMA training symbol generation

For PAM2 training frame, $Tr_n[0]$ shall be scrambled with the $DS_n[0]$ which is equal to $Scr_n[0]$ defined by clause 149.3.4. The output scrambled bit A_n shall be input to PAM2 mapper.

For PAM4 training payload, the pair of $Tr_n[0]$ and $Tr_n[1]$ shall be scrambled with two scrambler bits $DS_n[0]$ and $DS_n[1]$, defined by clause 149.3.4 and 149.3.2.2.18

The generation of scrambled bits $\{A_n,B_n\}$ can be found at Figure 200-5, with equation 200-4. The $\{A_n,B_n\}$ shall be input to the Gray mapping for PAM4 encoding specified by 149.3.2.2.19. The output G_n can be input to precoder and then to the PAM4 mapper defined by 149.3.2.2.21

$$G_n = \text{Gray mapping } (\{A_n,B_n\})$$

Equation: 200-11

$$T_{(n)} = \begin{cases} PAM2\_Mapper(A_n) & \sim(tx\_speed=10Gbps * (tx\_mode=SEND\_N + tx\_mode=SEND\_TA\_EXT)) + (0<= n <= N\_r-1) \\ PAM4\_Mapper(G_n) & tx\_speed=10Gbps * (tx\_mode=SEND\_N + tx\_mode=SEND\_TA\_EXT) * (N\_r <= n <= N\_r+N\_p-1) \end{cases}$$

Equation: 200-12

200.4.5.1~~1~~4 Generation of symbol ~~Tn~~ O_n

The transmit symbol O_n is selected by TDD control logic. For each TDD cycle (specified in Clause 200.4.6), the transmitter will send out T_n and 0, based on symbol time index *n*.

n will be continuous symbol count modulo *N_tdd.* The 33 bit scrambler shall be stopped during QUIET.

PAM2_Mapper is specified in 200.4.2.2.22

PAM4_Mapper is specified in 200.4.2.2.21

Gray mapping is specified in 200.4.2.2.19

N_tdd is the number of symbols equivalent to 9.6 us of tdd cycle time.

$$O_n = \begin{cases} T_{(n)} & 0 <= n <= N\_r + N\_p - 1 \\ 0 & N\_r + N\_p <= n <= N\_tdd-1 \end{cases}$$

Equation: 200-13

200.4.5.2~~5~~ PMA training mode descrambler polynomials

The PHY shall acquire descrambler state synchronization to the PAM2 or PAM4 training sequence and report success through scr_status. For side-stream descrambling, the MASTER PHY employs the receiver descrambler generator polynomial per Equation(200-6) and the SLAVE PHY employs the receiver descrambler generator polynomial per Equation(200-5).

~~**200.4.6 2xx.4.6 LPI signaling Only need if supporting EEE**~~

200.4.6 PCS TDD signaling

The following timing diagram shows the TDD cycle signaling and TDD frame structures. Table 200-7 assumes the 100M+MultiGBASE-T1/V1 PHY is the MASTER and MultiG+100MBASE-T1/V1 PHY is the SLAVE. If MASTER and SLAVE designation is reversed, a separate table is TBD.

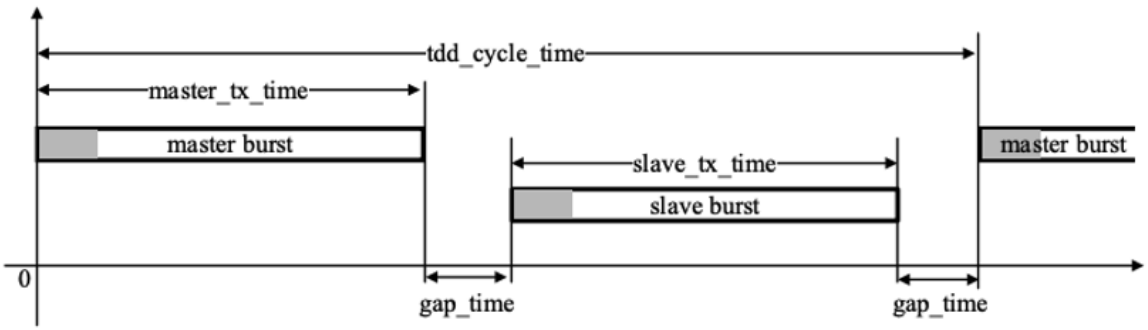


Figure 200-13 Master/Slave TDD cycle illustration

tx_mode	Master_tx_time (ns)	Slave_tx_time (ns)	tdd_cycle_time (ns)
SEND_TS	4586.67	4586.67	9600
SEND_TA	560	8826.67	
SEND_TA_EXT			
SEND_N			

Table 200-7 master_tx_time and slave_tx_time

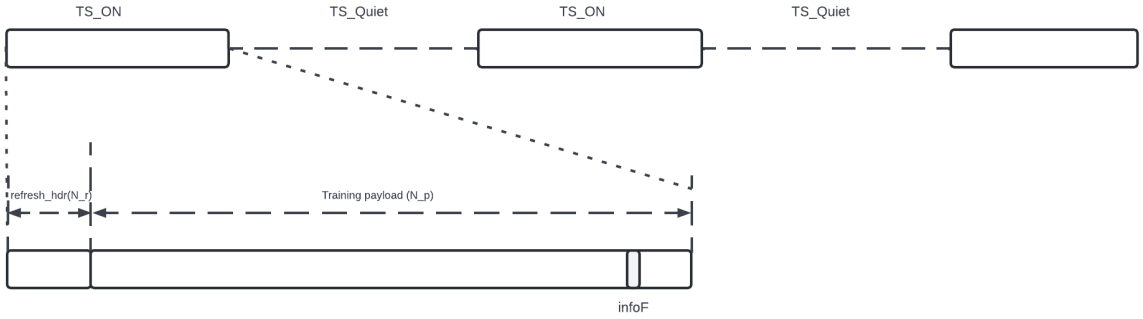


Figure 200-14-1 Symmetric training timing and frame structure

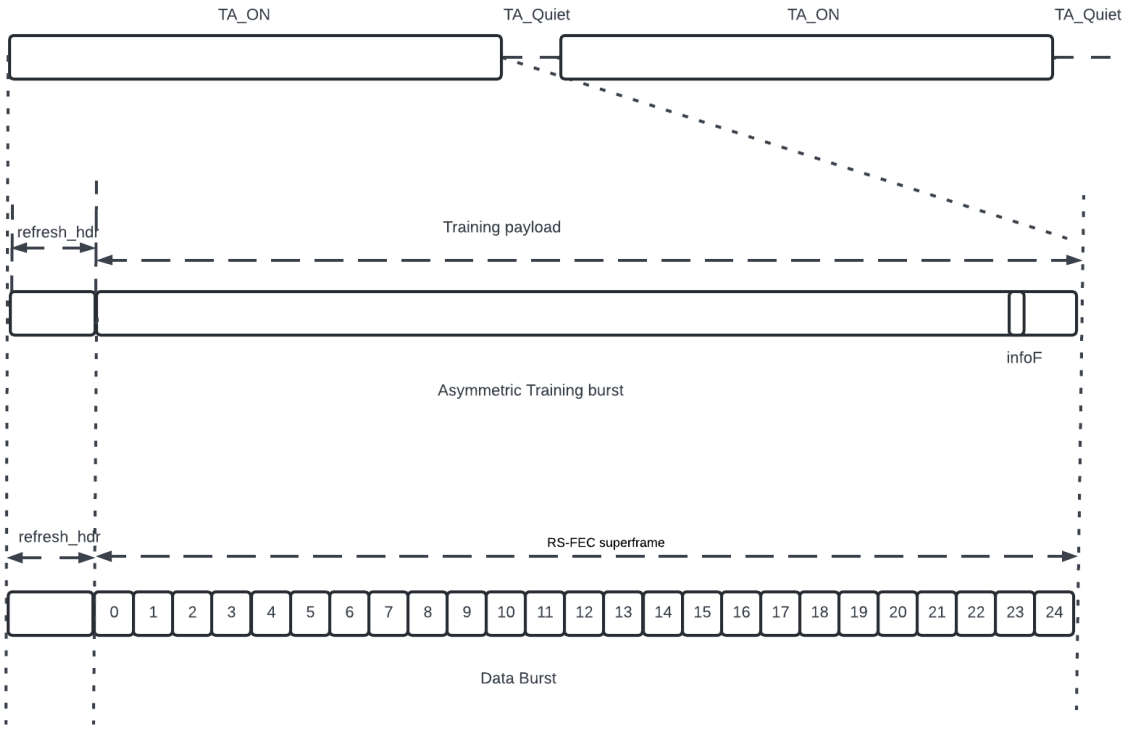


Figure 200-14-2 ASymmetric training/Data Mode timing and frame structure—MultiG+100MBASE-T1/V1 TX

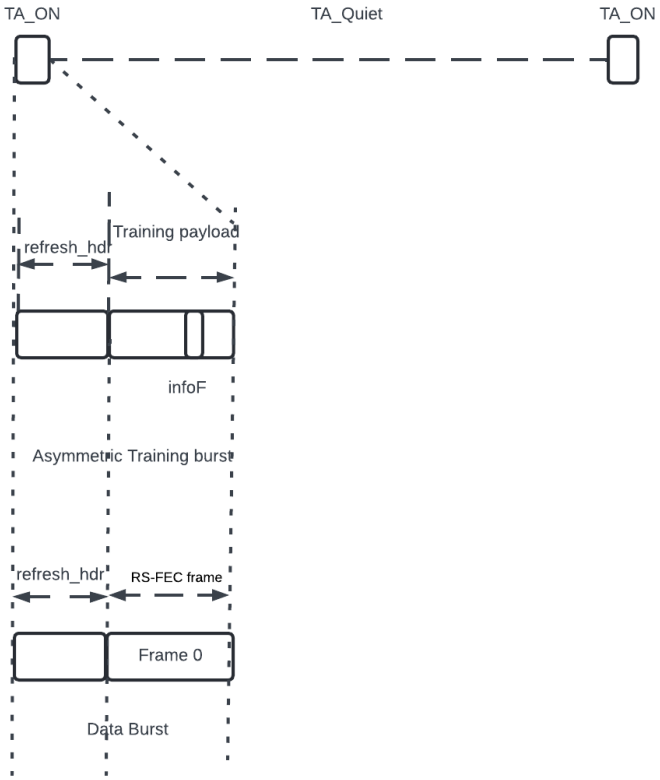


Figure 200-14-3 ASymmetric training/Data Mode timing and frame structure—100M+MultiGBASE-T1/V1 TX

200.4.7 PCS Detailed functions and state diagrams

200.4.7.1 State diagram conventions

As specified in MultiGBASE-T1 149.3.7.1

200.4.7.~~1~~2 State diagram parameters

200.4.7.~~1~~2.1 Constants

EBLOCK R<71:0>

72-bit vector to be sent to. the XGMII interface containing /E/ in all the eight character locations.

EBLOCK T<64:0>

65-bit vector to be sent to the RS-FEC encoder containing /E/ in all the eight character locations.

LBLOCK_R<71:0>

72-bit vector to be sent to the XGMII interface containing two Local Fault ordered sets. The Local Fault ordered set is defined in 46.3.4.

BLOCK_T<64:0>

65-bit vector to be sent to the RS-FEC encoder containing two Local Fault ordered sets.

~~LPBLOCK R<71:0>~~

~~12-bit vector to be sent to the XGMII containing /LI in all the eight character locations.~~

~~LPBLOCK T<64:0>~~

~~65-bit vector to be sent to the RS-FEC encoder containing /LI/ in all the eight character locations.~~

IBLOCK_R<71:0>

72-bit vector to be sent to the XGMII containing /I/ in all the eight character locations.

IBLOCK_T<64:0>

65-bit vector to be sent to the RS-FEC encoder containing /I/ in all the eight character locations.

RFER_CNT_LIMIT

TYPE: Integer

VALUE: 16

Number of Reed-Solomon frames with uncorrectable errors.

RFRX_CNT_LIMIT

TYPE: Integer

VALUE: 88

Number of Reed-Solomon frames received over bit error ratio interval.

UBLOCK_R<71:0>

72-bit vector to be sent to the XGMII containing two Link Interruption ordered sets.
The Link Interruption ordered set is defined in 46.3.4.

200.4.7.~~1~~2.2 Variables

rfer_test_lf

Boolean variable that is set TRUE when a new Reed-Solomon frame is available for testing and FALSE when RFER_TEST_LF state is entered. A new Reed-Solomon frame is available for testing when the Block Sync process has accumulated enough symbols from the PMA to evaluate the next Reed-Solomon frame.

block lock

- Boolean variable that is set TRUE when receiver acquires block delineation. If 40(TBD) consecutive RS-FEC frame errors are detected, the block_lock flag is de-asserted. The block_lock flag is re-asserted upon detection of a valid RS-FEC frame.

hi_rfer

Boolean variable that is asserted TRUE when the rfer_ent reaches 16 (TBD) errors in one rfer timer interval.

lp_low_snr (TBD)

Boolean variable that is set TRUE when the link partner indicates TDD refresh is insufficient to maintain PHY SNR. It is set FALSE otherwise.

pcs_data_mode

Variable set by the PMA PHY Control function. See 200.6.4.1.

pcs_reset

Boolean variable that controls the resetting of the PCS. It is TRUE whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rx_coded<64:0>

Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 149-8. The leftmost bit in the figure is x_coded <0> and the rightmost bit is rx_coded <64>.

rx_raw<71:>

Vector containing two successive XGMII output transfers. RXC<3:0> for the first transfer are taken from rx_raw<3:0>. RXC<3:0> for the second transfer are taken from rx_raw<7:4>. RXD<31:0> for the first transfer are taken from rx_raw<39:8>. RXD<31:0> for the second transfer are taken from rx_raw<71:40>.

rf_valid

Boolean indication that is set TRUE if received Reed-Solomon frame is valid. Reed-Solomon frame is valid if and only if all parity checks of the Reed-Solomon code are satisfied.

tx coded<64:0>

Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 149-8. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx coded<64>.

tx_raw<71:0>

Vector containing two successive XGMII transfers. TXC<3:0> for the first transfer are placed in tx_raw<3:0>. TXC<3:0> for the second transfer are placed in tx raw<7:4>. TXD<31:0> for the first transfer are placed in tx raw<39:8>. TXD<31:0> for the second transfer are placed in tx raw<71:40>.

tdd_detect

Set TRUE when the receiver has reliably detected TDD signaling. It is set FALSE otherwise.

pcs_tx_mode (TBD)

A variable indicating the signaling to be sent from PCS Transmit process.

The parameter pcs_tx_mode can take on one of the following values of the form:

NORMAL:	This value is continuously asserted during transmission of sequences of symbols representing a XGMII data stream in the data mode.
T_2p5G:	This value is continuously asserted in case transmission of sequences of symbols representing the symmetric training mode is to take place. Both MASTER and SLAVE send 3Gsps PAM2 training frames.
T_PAM2:	This value is continuously asserted in case transmission of sequences of symbols representing the asymmetric training mode is to take place. 100M+MultiGBASE-T1/V1 PHY sends 3Gsps PAM2 TDD training frames. MultiG+100MBASE-T1/V1 PHY sends target Baud rate with PAM2 TDD training frames
T_PAM2_4:	This value is continuously asserted in case transmission of sequences of symbols representing the asymmetric extended training mode is to take place for MultiG+100MBASET-T1/V1 in 10Gbps mode. 100M+MultiGBASE-T1/V1 sends 3Gsps PAM2 training frames. MultiG+100MBASE-T1/V1 sends 6Gsps PAM2/PAM4 training frames
QUIET:	This value is continuously asserted in case transmission of zero symbols is required

rs_fec_frame_done

A Boolean value. This variable is set TRUE when the final symbol of each RS-FEC frame is transmitted. It is set FALSE otherwise.

rx_tdd_active

A Boolean variable that is set TRUE by the PHY control telling the PCS receive to start operating in the TDD receive mode and set FALSE otherwise. The TDD receive mode begins when the PHY detect the presence of the TDD bursts from link partner. This signal will be de-asserted if TDD bursts are not detected in user-defined timeout period (usually 3~5 TDD cycles)-- TBD.

rx_on

A Boolean variable that is set TRUE when the PHY PCS receive function is operating in the training/data frame receive mode and set FALSE otherwise. During symmetric training, this starts after burst is detected by the PMA (indicated by detect_lp_burst from PMA) and ends when the receive burst has ended. It can also be controlled by pre-defined timer after timing and frame synchronization is achieved.

rx_data_active

A Boolean variable that is set TRUE when the PHY PCS receive function is operating in the data frame receive mode and set FALSE otherwise. This can be controlled by pre-defined timer after timing and frame synchronization is achieved.

tx_tdd_active

A Boolean variable that is set TRUE by the PHY control telling the PCS to start operating in the TDD transmit mode. It is set FALSE otherwise.

tx_on

A Boolean variable that is set TRUE during the TDD transmit mode, when the PHY PCS is transmitting training or data frames. It is set FALSE when PCS is transmitting QUIET symbols.

tx_data_active

A Boolean variable that is set TRUE during the TDD transmit mode, when PHY PCS is transmitting RS-FEC data frames. It is set FALSE otherwise.

tx_qt_active

A Boolean variable that is set TRUE during the TDD transmit mode, when the PHY is transmitting quiet signaling. It is set FALSE otherwise.

200.4.7.2.3 Timers (TBD)

Rfer_timer (TBD)

TDD_on_s_timer

A timer used to control the duration for the Transmission of symmetric PAM2 training sequence during TRAINING0 and COUNTDOWN0 state of PHY control state. A value of 4586.67 ns is defined.

TDD_qt_s_timer

A timer used to control the duration for the QUIET period of symmetric PAM2 training during TRAINING0 and COUNTDOWN0 state of PHY control state. A value of 5013.33 ns is defined.

TDD_on_a_timer

A timer used to control the duration for the Transmission of asymmetric training sequence during TRAINING1, TRAINING2, COUNTDOWN1 and COUNTDOWN2 state of PHY control state. A value of 560 ns for the MASTER PHY and a value of 8826.67 ns for the SLAVE PHY.

TDD_qt_a_timer

A timer used to control the duration for the QUIET period of asymmetric training during TRAINING1, TRAINING2, COUNTDOWN1 and COUNTDOWN2 state of PHY control state. A value of 9040 ns for the MASTER PHY and a value of 773.33 ns for the SLAVE PHY.

TDD_on_d_timer

A timer used to control the duration for the Transmission of asymmetric training sequence during DATA state of PHY control state. A value of 560 ns for the MASTER PHY and a value of 8826.67 ns for the SLAVE PHY.

TDD_qt_d_timer

A timer used to control the duration for the QUIET period DATA state of PHY control state. A value of 9040 ns for the MASTER PHY and a value of 773.33 ns for the SLAVE PHY.

200.4.7.2.4 Functions

DECODE(rx_coded<64:0>)

In the PCS Receive process, this function takes as its argument 65-bit rx_coded<64:0> from the RS-FEC decoder and decodes the 65B RS-FEC bit vector returning a vector rx_raw<71:0>, which is sent to the XGMII. The DECODE function shall decode the block based on code specified in 200.4.2.2.2.

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector received from the XGMII, returning 65-bit vector tx_coded. The ENCODE function shall encode the block as specified in 200.4.2.2.2.

R BLOCK_ TYPE = {C, S, T, D, E, ~~I, LI, LII~~}

~~When the EEE capability is not supported, this function classifies each 65-bit rx_coded vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.~~
~~When the EEE capability is supported, this function classifies each 65-bit rx_coded vector as belonging to one or more of the eight types depending on its contents. A vector may simultaneously belong to the C and I types when it contains eight valid control characters that are all /1/, but in e~~Every ~~other~~ case of the vector belongs to only one type.
Values: C; The vector contains a data/ctrl header of 1 and one of the following

a) A block type field of 0x1E and ~~eight~~ seven valid control characters other than /E/ ~~and /LI/;~~
b) A block type field 0x2D or 0x4B, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.

S; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.

T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.
D; The vector contains a data/ctrl header of 0.
~~I; If the optional EEE capability is supported, then the I type is a special case of the C type where the vector contains a data/tri header of 1, a block type field of 0x1E, and eight control characters of I/.~~
~~LI: If the optional EEE capability is supported, then the LI type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1E, and eight control characters of /L/.~~
~~LII: If the optional EEE capability is supported, then the LII type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1E, and one of the following:~~
~~a) Four control characters of /LI/ followed by four control characters of /I/;~~
~~b) Four control characters of /I/ followed by four control characters of /LI/~~
E; The vector does not meet the criteria for any other value.
A valid control character is one containing a ~~MultiGBASE-T~~ control code specified in Table 200-2. A valid O code is one containing an O code specified in Table 200-2.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_ TYPE NEXT(TBD)

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

T_BLOCK_TYPE = {C, S, T, D, E, ~~I, LI, LII~~}
~~When the EEE capability is not supported, this function classifies each 72-bit tx_raw vector as belonging to one of the five types {C, S, T, D, B} depending on its contents.~~
~~When the EEE capability is supported, this function classifies each 72-bit tx_raw vector as belonging to~~

~~one or more of the eight types depending on its contents. A vector may simultaneously belong to the C and I types when it contains eight valid control characters that are all /1, but in e~~Every ~~other~~ case of the vector belongs to only one type.

Values: C; The vector contains one of the following:

a) ~~Eight~~ Seven valid control characters other than /0/,/S/, /T/, /E/, ~~and /LI/~~;

b)One valid ordered set and four valid control characters other than /0/,/S/, and /T/;

c)Two valid ordered sets.

S; The vector contains an /S/ in its first or fifth character. Any characters before the S character are valid control characters other than /0/, /S/ and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.

~~I; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.~~

~~D; The vector contains eight data characters.~~

~~I; If the optional EEE capability is supported, then the I type is a special case of the C type where the vector contains eight control characters of .~~

~~LI; If the optional EEE capability is supported, then the LI type occurs when the vector contains eight control characters of /LI/.~~

~~LII; If the optional EEE capability is supported, then the LII type occurs when the vector contains one of the following:~~

~~a) Four control characters of /LI/ followed by four control characters of /I;~~

~~b) Four control characters of /I/ followed by four control characters of /LI/.~~

E; The vector does not meet the criteria for any other value.

A tx raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 200-2. A valid ordered set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /0/. A valid /O/ is any character with a value for O code in Table 200-2.

T_TYPE(tx_raw<71:0>)

Returns the T_BLOCK_ TYPE of the t_raw <71:0> bit vector.

T_TYPE_NEXT (TBD)

Prescient end of packet check function. It returns the FRAME_ TYPE of the tx_raw vector immediately following the current tx_raw vector.

200.4.7.2.5 Counters

rfer _cnt

Count up to a maximum of RFER CNT LIMIT of the number of invalid Reed-Solomon frames within the current RFRX_CNT_LIMIT Reed-Solomon frame period.

rfrx_cht

Count number Reed-Solomon frames received during current period.

200.4.7.2.6 Messages

RX_FRAME

A signal sent to PCS Receive indicating that a full Reed-Solomon frame has been decoded and the variable rf_valid is updated.

200.4.7.3 State diagram

As specified in MultiGBASE-T1 in 200.3.7.3, with minor changes in Figure numbers..

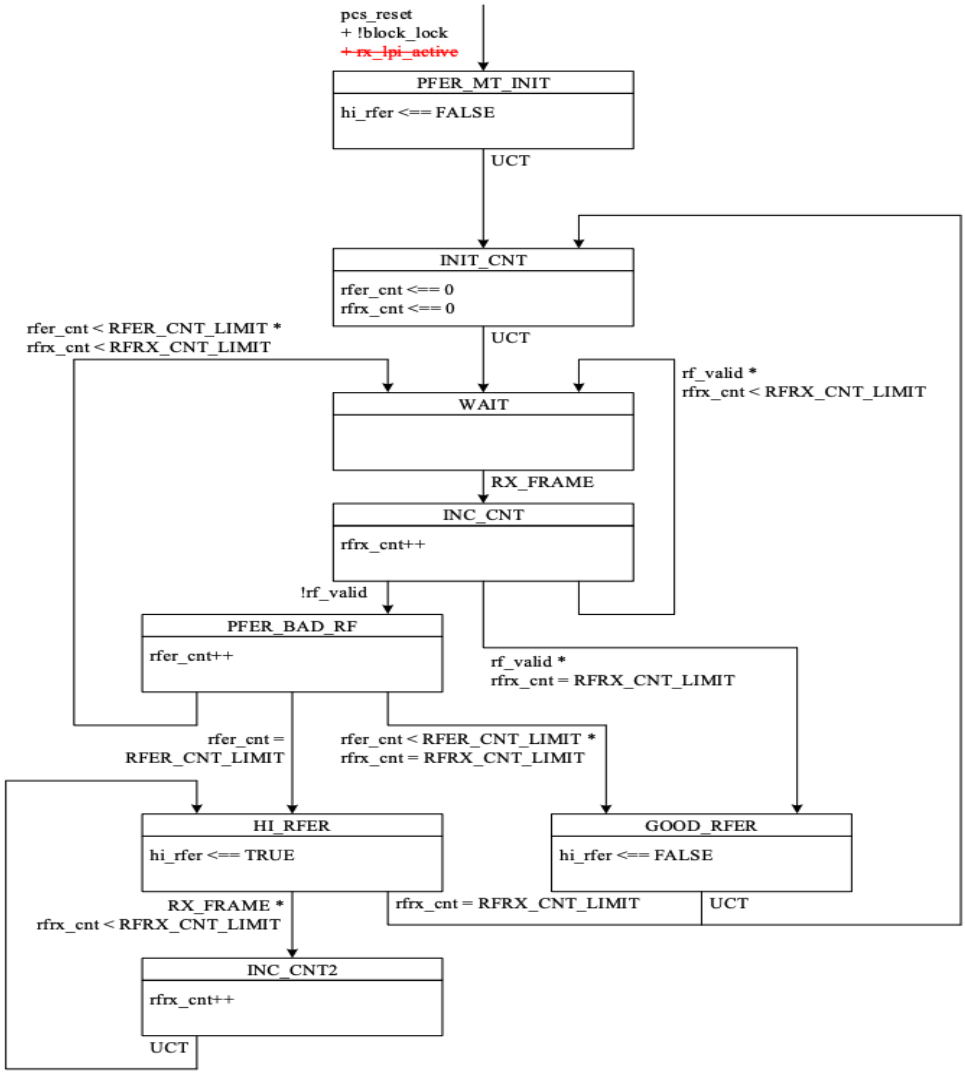


Figure 200-15 RFER Monitor Block Diagram

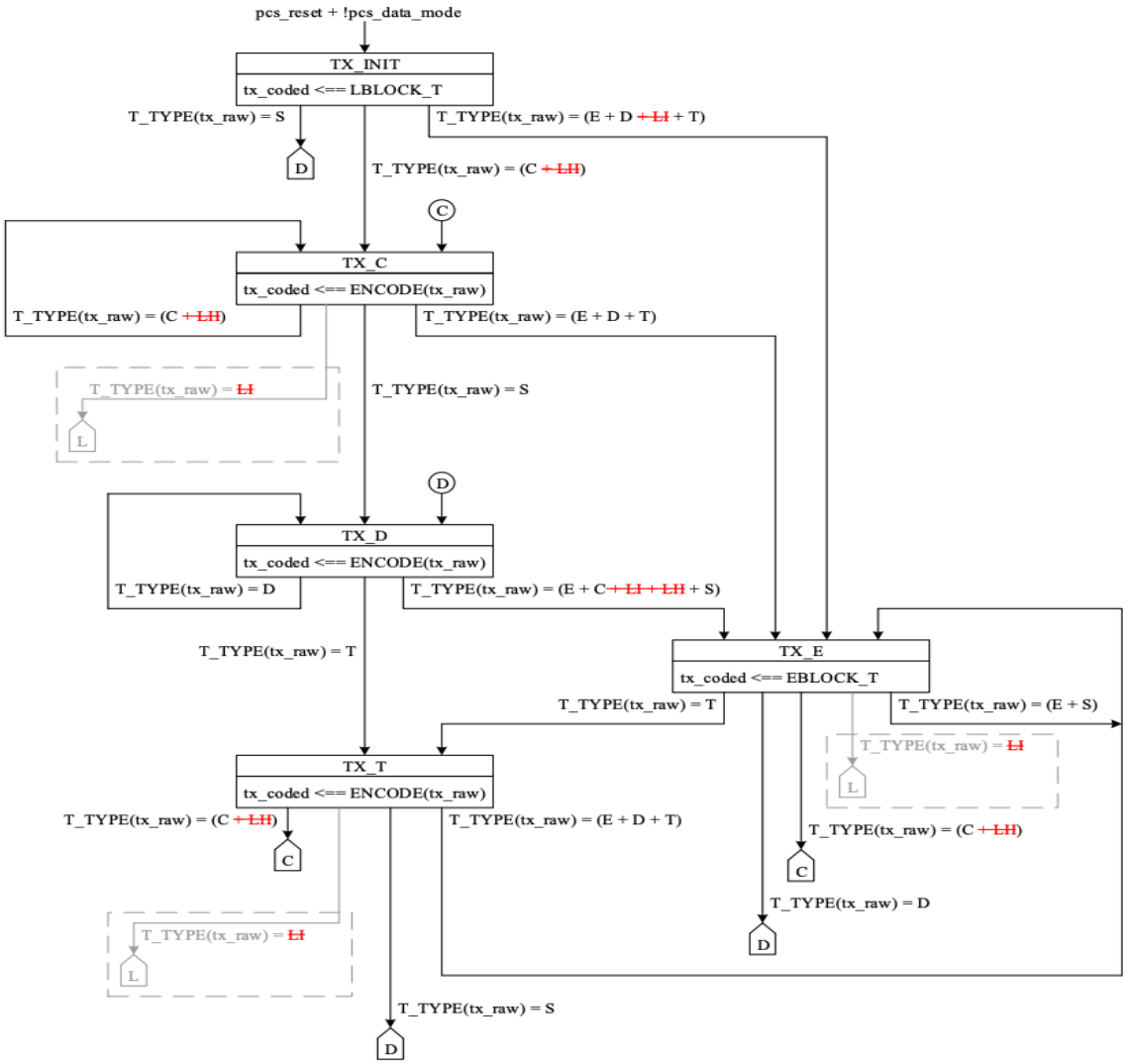


Figure 200-16 PCS 64B/65B Transmit state diagram

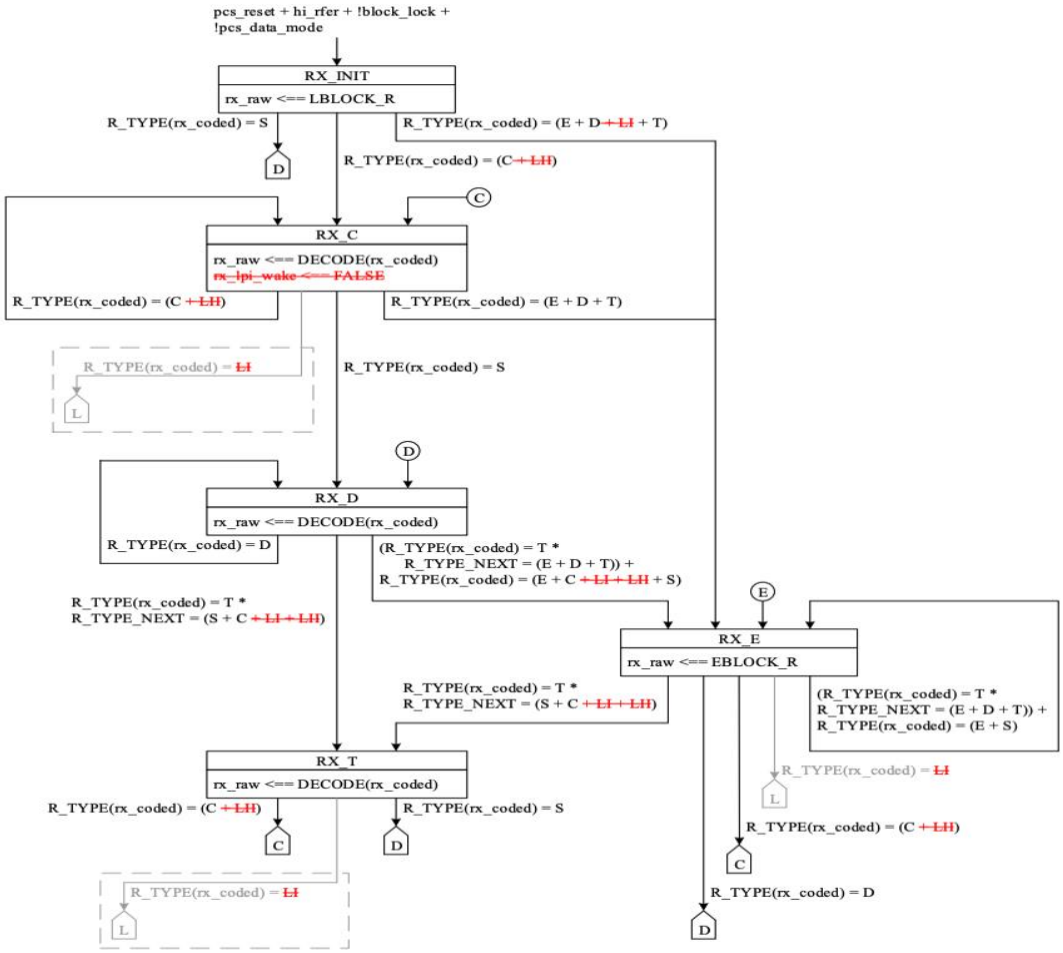


Figure 200-17 PCS 64B/65B Receive state diagram

200.4.8 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

200.4.8.1 Status

PCS_status

Indicates whether the PCS is in a fully operational state. It is only TRUE if pcs data mode is TRUE, block_ lock is TRUE, and hi_rfer is FALSE. This status is reflected in MDIO bit 4.2324.10 (TBD). A latch low view of this status is reflected in MDIO bit 4.2323.2 (TBD) and the inverse of this status is reflected in MDIO bit 4.2323.7(TBD).

Block_lock

Indicates the state of the block_lock variable. This status is reflected in MDIO bit 4.2324.8(TBD). A latching low version of this status is reflected in MDIO bit 4.2324.6(TBD)

Hi_rfer

Indicates the state of the hi_rfer variable. This status is reflected in MDIO bit 4.2324.9(TBD). A latching high version of this status is reflected in MDIO Bit 4.2324.7(TBD).

RX TDD indication (TBD)

Indicates the current state of the receive TDD function.

TX TDD indication (TBD)

Indicates the current state of the transmit TDD function.

200.4.8.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.
RFER_count:

6-bit counter that counts each time the RFER_BAD_RF of the RFER monitor state diagram (see Figure 200-15) is entered. This counter is reflected in MDIO register bits 4.2324<5:0>(TBD). The counter is reset when register 4.2324 (TBD) is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT _LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

200.4.9 MultiG+100MBASE-T1/V1 operations, administration, and maintenance (OAM) (TBD)

~~*Only if OAM is used in high speed direction.*~~

200.5 Physical Coding Sublayer (PCS) functions, 100M+MultiGBASE-T1/V1

As specified for MultiG+100MBASE-T1/V1 PCS in 200.4

~~**200.5.1 PCS service interface (MII)**~~

~~**200.5.2 PCS functions**~~

~~**200.5.2.1 PCS Reset function**~~

~~**200.5.2.2 PCS Transmit function**~~

~~**200.5.2.2.1 Use of blocks**~~

~~200.5.2.2.2 TBD transmission code~~

~~200.5.2.2.3 Notation conventions~~

~~200.5.2.2.4 Block structure~~

~~200.5.2.2.5 Control codes~~

~~200.5.2.2.6 Ordered sets~~

~~200.5.2.2.7 Idle (/I/)~~

~~200.5.2.2.8 LPI (/LI/)~~

~~200.5.2.2.9 Start (/S/)~~

~~200.5.2.2.10 Terminate (/T/)~~

~~200.5.2.2.11 Ordered set (/O/)~~

~~200.5.2.2.12 Error (/E/)~~

~~200.5.2.2.13 Transmit process~~

~~200.5.2.2.14 RS-FEC framing and RS-FEC encoder~~

~~200.5.2.2.15 Reed-Solomon encoder~~

~~200.5.2.2.16 PCS scrambler~~

~~200.5.2.2.17 TBD encoding~~

~~200.5.2.2.18 EEE capability Only need if supporting EEE~~

~~200.5.2.3 PCS Receive function~~

~~200.5.2.3.1 Frame and block synchronization~~

~~200.5.2.3.2 PCS descrambler~~

~~200.5.2.3.3 Invalid blocks~~

~~200.5.3 Test-pattern generators~~

~~200.5.4 Side-stream scrambler polynomials~~

~~200.5.5 PMA training frame~~

~~**200.5.5.1 Generation of symbol Tn**~~

~~**200.5.5.2 PMA training mode descrambler polynomials**~~

~~**200.5.6 LPI signaling Only need if supporting EEE**~~

~~**200.5.7 Detailed functions and state diagrams**~~

~~**200.5.7.1 State diagram parameters**~~

~~**200.5.7.1.1 Constants**~~

~~**200.5.7.1.2 Variables**~~

~~**200.5.8 PCS management**~~

~~**200.5.9 100M+MultiGBASE-T1/V1 operations, administration, and maintenance (OAM)**~~

~~**Only if OAM is used in low speed direction.**~~

200.6 Physical Medium Attachment (PMA) sublayer, MultiG+100MBASE-T1/V1

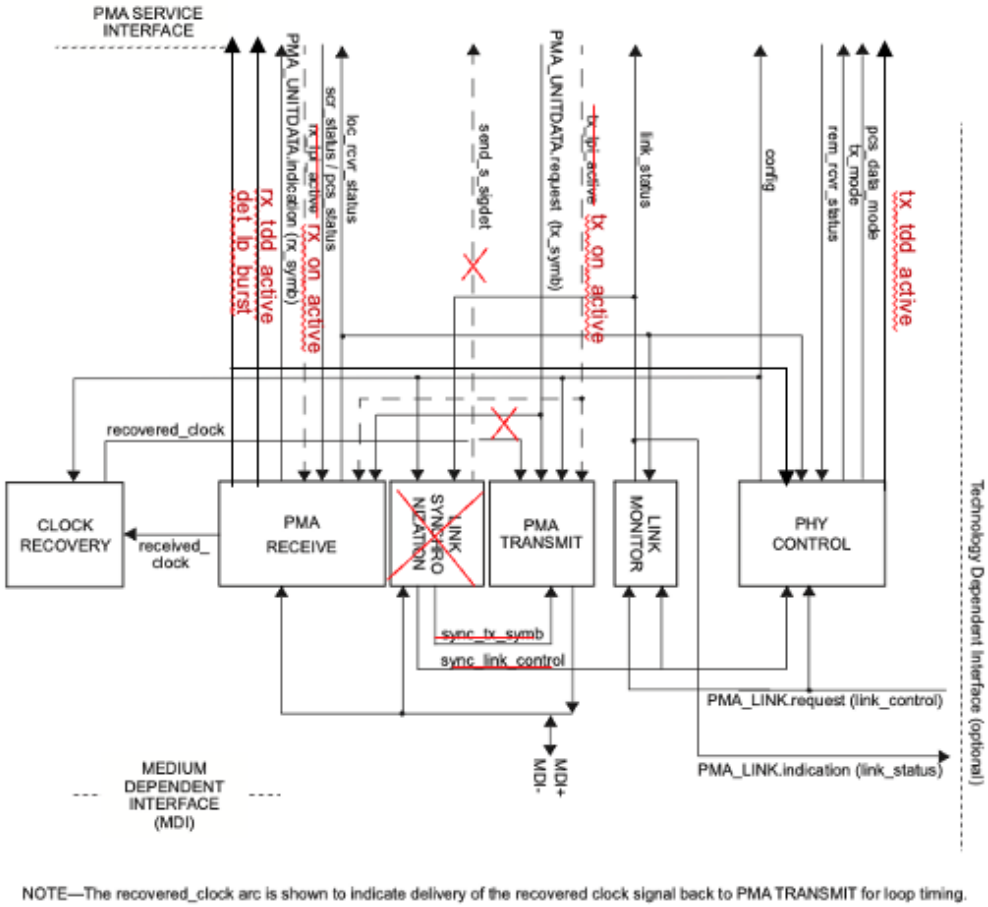
I did not include all subclauses as they can vary with implementation. You can look at any PHY project that is similar to see which may be needed. Other subclauses may be added as baselines are chosen.

200.6.1 PMA functional specifications

149.4.1 PMA functional specifications

The PMA couples messages from the PMA service interface specified in ~~149~~.2.2 to the MultiGBASE-T1 baseband medium, specified in ~~149~~.7.

The interface between the PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in ~~149~~.8.



NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

Figure ~~149~~–26—PMA reference diagram

200.6.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery, All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 200-26, shows how the operating functions relate to the messages of the PMA service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 200-26.

200.6.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power for the device containing the PMA has not reached the operating state.

b) The receipt of a request for reset from the management entity.

PMA Reset sets pma_reset = ON while any of the above reset conditions hold TRUE. All state diagrams take the open-ended pma reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The 100M+MultiGBASE-T1/V1 or MultiG+100MBASE-T1/V1 PMA takes no longer than 100 (TBD 50?) ms to enter the PCS DATA state after exiting from reset or low power mode (see Figure 200-32), if Link Partner has already exited DISABLE_TRANSMITTER state.

200.6.2.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a two-level or four-level modulated signal on the single balanced pair of conductors or a single ended coaxial cable (TBD). When the PHY Control state diagram (Figure 200-32) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by tx_symb onto the MDI, followed by a quiet period to complete a TDD cycle. The PMA shall repeat such TDD cycles with the predefined timing parameters specified in 200.4.6. The signals generated by PMA Transmit shall comply with the electrical specifications given in 200.x.2 (TBD).

When the PMA_CONFIG indication parameter config is MASTER, the PMA Transmit function shall source TX TCLK from a local clock source while meeting the transmit jitter requirements of 200.x.2.3(TBD). The MASTER-SLAVE relationship shall include loop timing. If the PMA_CONFIG indication parameter config is SLAVE, the PMA Transmit function shall source TX TCLK from the recovered clock of 200.4.2.8 while meeting the jitter requirements of 200.x.2.3(TBD)

200.6.2.2.1 Global PMA transmit disable

When the PMA transmit disable variable is set to TRUE, this function shall turn off the transmitter so that the average launch power of the transmitter is less than -53 (TBD)dBm

200.6.2.3 PMA Receive function

The PMA Receive function comprises a receiver for PAM2 or PAM4 signals on the balanced pair or the single ended pair. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over the receive pair and to present these sequences to the PCS Receive function. The PMA translates the signals received on the pair into the PMA_UNITDATA indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 2×10^{-10} (TBD)after RS-FEC decoding, over a channel meeting the requirements of 200.7 (TBD)

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization. No echo cancellation is needed due to the TDD nature of the duplexing method.

The PMA Receive function uses the parameters pcs_status and scr_status, and the state of the equalization, and estimation functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND Z from any other value (see the PHY Control state diagram in Figure 200_32). Failing to receive Link Partner's consecutive TDD bursts could trigger deassertion of loc_rcvr_status. The SEND_Z signal during the TDD QUIET period alone shall not trigger the DUT to de-assert its loc_rcvr_status. The precise algorithm for generation of loc_rcvr status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for pair polarity swaps.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.193.7. (TBD)

200.6.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram in Figure 200-32.

During PMA training (TRAINING and COUNTDOWN states in Figure 200-32), PHY Control information is exchanged between link partners with a 12-octet Infofield, which is XORed with the 96 bits starting after the *N_inf* bit of the training payload specified in 200.4.5.3. The Infofield is also denoted IF. The link partner is not required to decode every IF transmitted but is required to decode IFs at a rate that enables the correct actions prior to the training phase transition.

The 12-octet Infofield shall include the fields in 200.6.2.4.2 through 200.6.2.4.8, also shown in Figure 200-27 and Figure 200-28. Infofield shall be transmitted at least 16 (TBD) times with each change to octets 7 to 10.

PMA_state=00

octet 1	octet 2	octet 3	octet 4/5/6	octet 7	octet 8	Octet 9/10	octet 11/12
0xBB	0xA7	0x00	BC24	Message	delay counter	PHY capability bits	CRC16

Infofield TRAINING format

Figure 200-27

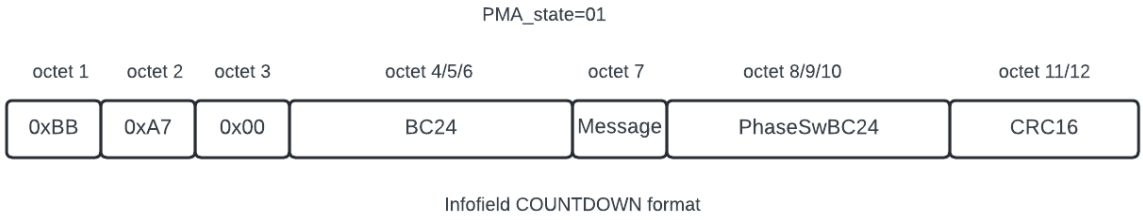


Figure 200-28

200.6.2.4.1 Infofield notation

For all the Infofield notations in the following subclauses, Reserved ‹bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The Infofield is transmitted following the notation where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

200.6.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of three octets [Octet 1<7:0>, Octet 2<7:0>, Octet 3<T:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Octet 1<7:0 > and so forth.

200.6.2.4.3 PHY burst count (BC24)

The PHY burst count consists of 3 (TBD) octets [Oct4<7:0>,Oct5<7:0>,Oct6,7:0>] and indicates the running count of PHY bursts sent LSB first. The BC24 continues to run uninterrupted for the duration of the link.

BC24 is defined to rollover to 0 after it reaches 16776959. BC24 could roll over in the case MASTER has started long before SLAVE send the 1st responding Burst.

200.6.2.4.4 Message Field

The Message Field is one octat. For both MASTER and SLAVE, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, training_phase<4:3>, reserved<2:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6>=00 indicates TRAINING, and PMA_state<7:6>=01 indicates COUNTDOWN.

The two training_phase-indicator bits Training_phase<4:3> shall communicate the training phase of the transmitting transceiver to the link partner. Training_phase<4:3> =00 indicate SYMMETRIC TRAINING, Training_phase<4:3>=01 indicates ASYMMETRIC TRAINING, and Training_phase<4:3>=10 indicates EXTENDED ASYMMETRIC TRAINING in 10Gbps mode.

All possible Message Field settings are listed in Table 200-10 for MASTER or SLAVE. Any other values shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA burst shall be the first row of Table 200-10 for MASTER, and the first or second row of Table 200-10 for SLAVE. Moreover, for a given Message Fields setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the Infofield variable is set to loc_rcvr_status<5>=1 and set to 0 otherwise.

PMA_state<7:6>	loc_rcvr_status	Training phase<4:3>	reserved	reserved	reserved
00	0	0	0	0	0
00	1	0	0	0	0
01	1	0	0	0	0
00*	0	1	0	0	0
00	1	1	0	0	0
01	1	1	0	0	0
00*	0	2	0	0	0
00*	1	2	0	0	0
01*	1	2	0	0	0

Table 200-10 -- Infofield message field valid MASTER or SLAVE settings

* Means this row could be skipped if not applicable

200.6.2.4.5 PHY capability bits

When PMA_state<7:6>= 00, then [Oct9<7:0>,Oct10<7:0>] contains the PHY capability bits. Each octet is sent LSB first.

The format of PHY capability bits is Oct10<1:0>= PrecoderSel, Oct10<2>= OAMEn, Oct10<4:3>=Negotiated(operation) High speed, Oct10<7:5>=Speed Capability. Oct9<7:0>=VendorSpecificData[7:0]. Other bits are reserved.

Speed Capability (MultiG+100MBASE-T1/V1 PHY set its TX capability, 100M+MultiGBASE-T1/V1 PHY set its RX capability): Oct10<5> 2.5G capable, Oct10<6> 5G capable, Oct10<7> 10G capable.

Negotiated High speed: 00 -- 2.5G, 01– 5G, 10 – 10G

OAMEn: The optional BASE-T1/V1 OAM capability shall be enabled only if both PHYs set the capability bit OAMen=1

PrecodeSel indicates the requested precoder.

The capability bit values shall be considered as valid only when loc_rcvr_status bit is 1.

The criteria to set Negotiated Speed is TBD

Table 200-11 – PHY capability bits

Oct 9								Oct 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
VendorSpecificData								PrecodeSel		OAMEn		Negotiated speed		Speed Capability 2.5G	Speed Capability 5G	Speed Capability 10G

200.6.2.4.6 TDD delay counter

When PMA_state<7:6>=00, then Oct8<7:0> contains TDD delay counter sent LSB first. The format of TDD delay counter is Oct<1:0>= Reserved. Oct<2>= delay_count_valid. Oct<7:3>= delay _count<4:0>.

TDD delay counter is only defined during the symmetric training phase, when PMA_state<7:6>=00. The initial value shall be set to 0.

After MASTER PHY detects SLAVE TDD burst position, it should estimate the channel delay, then set its delay_count in the TDD delay counter to a value between 0 to 31(TBD), as well as set delay_count_valid bit to 1. Each LSB unit represents 5.333 ns delay (16 symbols in 3G symbol rate).

SLAVE shall accept the received remote delay_count only when received remote delay_count_valid bit is set to 1. SLAVE shall store this delay_count number.

As acknowledgement of the reception of this delay_count, SLAVE shall send back its received delay count in its own delay_count field and set its delay_count_valid to 1, so MASTER can confirm the exchange of this information is completed. When MASTER or SLAVE finishes the exchange of delay count, the negotiated speed, and the PrecodeSel, it shall set Negotiation_done signal to 1. The PHY control can then move to COUNTDOWN0 state, if loc_rcvr_status and rem_rcvr_status are both OK.

Starting from Asymmetric training and to the data mode, SLAVE shall adjust its transmit burst position according to the stored delay_count. It should move its transmit starting time (relative to the last MASTER payload bit at the SLAVE MDI input) earlier by 26.666ns + delay_count *5.333ns, compared with symmetric training case (200.6.2.4.11).

Table 200-12 – TDD delay counter

Oct 8							
0	1	2	3	4	5	6	7
	Reserved	Delay_count_valid					Delay_count

Note: the TDD delay_counter fields and PHY capability bits field are only defined during symmetric training TRAINING0 state, but not defined in other states.

200.6.2.4.7 Phase switch PHY burst count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0> Oct10<7:0>] contains the data switch burst count (PhaseSwBC24) sent LSB first. PhaseSwBC24 indicates the burst count when MASTER transmitter switch from current training phase to the next training phase or Data mode. The last value of the BC24 prior to the transition is PhaseSwBC24-1.

Since phase switch is always initiated from the MASTER side transmitter, the PhaseSwBC24 value of SLAVE infofield will be ignored(TBD). MASTER will make the phase switch after sending the last burst (BC24=PhaseSwBC24-1), and receiving the last burst from the SLAVE. SLAVE will make the phase switch after receiving the last burst (BC24=PhaseSWBC24-1) from MASTER and finishing sending the last burst of its own.

200.6.2.4.8 Reserved fields

When PMA_state<7:6> is greater than 01, then [Oct8<7:0>, Oct9<7:0> Oct10<7:0>)] contains a reserved field. All Infofield fields denoted reserved are reserved for future use.

200.6.2.4.9 CRC16

Specified in Clause 149.4.2.4.8

200.6.2.4.10 PMA MDIO function mapping

Specified in Clause 149.4.2.4.9, with possible modifications

200.6.2.4.11 Startup sequence

The startup sequence shall comply with the state diagram description given in Figure 200-32. PMA_CONFIG is predetermined to be MASTER or SLAVE via management control during initialization or via default hardware setup.

During startup, prior to entering the TRAINING0 state, the SLAVE shall align its transmit PMA training frame to be 133.33 ns after the last PMA training payload bit from MASTER appears on the SLAVE input MDI. The SLAVE Infofield Burst count shall match the MASTER Infofield burst count from this previous PMA training frame.
In the TRAINING0 state, PAM 2 transmission is used and PHY capabilities, PrecoderSel and delay_count are exchanged with Infofields as specified in 200.6.2.4.5. The final negotiated speed mode will be determined (TBD)
At any COUNTDOWN state, if the local receiver status (indicated by loc_rcvr_status) transitions to NOT_OK, PHY Control returns to the SILENT0 state and attempts a retrain.

After starting TRAINING1/COUNTDOWN1 or TRANING2/COUNTDOWN2 or DATA MODE, the SLAVE shall use the MASTER transmitted delay_count to align its transmit PMA training frame to be 106.66ns – delay_count*5.33ns (TBD), after the last PMA training payload bit from the MASTER appears on the SLAVE input MDI.

MASTER link_fail_inhibit_timer is started when it detects 1st SLAVE transmitted PMA training frame. SLAVE link_fail_inhibit_timer is started when it sends first PMA training frame to the MASTER. The link_fail_inhibit_timer value is defined to be 50 ms (TBD), it is used to force a restart if the link up cannot be achieved within maximum allowed time.

MASTER and SLAVE will move from TRAINING0 state to COUNTDOWN0 state, if local_rcvr_status and rem_rcvr_status are both asserted, and negotiation_done bit is OK.

200.6.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link status. Failure of the underlying receive channel causes the PMA to set link status to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the link.

The Link Monitor function shall comply with the state diagram of Figure 200-33.

Upon power on reset, or release from power down, the PHY sets link control = DISABLE. During this period, link_status = FAIL is asserted. When the PHY link control is set to ENABLE, the Link Monitor state diagram begins monitoring the PCS and receiver lock status. As soon as reliable transmission is achieved, with pcs_data_mode=TRUE, the variable link_ status = OK is asserted, upon which further PHY operations can take place.

~~**200.6.2.6 PHY Link Synchronization**~~

~~**200.6.2.6.1 State diagram variables**~~

~~**200.6.2.6.2 State diagram timers**~~

~~**200.6.2.6.3 Messages**~~

~~**200.6.2.6.4 State diagrams**~~

200.6.2.7 ~~Refresh monitor function Only needed if EEE is implemented.~~ TDD monitor function(TBD)

The TDD monitor shall comply with the state diagram of Figure 200-34 (TBD). The TDD monitor sets the PMA TDD status variable, which forces a link retrain if a TDD signal is not reliably detected within a moving time window equivalent to 10 (TBD) complete TDD cycles (nominally equal to 96(TBD) us).

200.6.2.8 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RFER indicated in 200.6.2.3 is achieved. The received clock signal is expected to be stable and ready for use when training has been completed. The received clock signal is supplied to the PMA Transmit function by received _clock.

200.6.3 MDI

Communication through the MDI is summarized in 200.6.3.1 and 200.6.3.2.

200.6.3.1 MDI signals transmitted by the PHY

Specified in 149.4.3.1

200.6.3.2 Signals received at the MDI

Specified in 149.4.3.2

200.6.4 State variables

200.6.4.1 State diagram variables

config

The PMA generates this variable continuously and passes it to the PCS via the PMA_CONFIG.indiation primitive.

Values: MASTER or SLAVE

link_control

This variable is defined in 200.2.1.1.1 (TBD)

link_status

The link_status parameter set by PMA Link Monitor state diagram and communicated through the PMA_LINK.indication primitive.

Values: OK or FAIL

loc_countdown_done

This variable is only used by the MASTER. It is set to false when the PHY Control state diagram is in the DISABLE_TRANSMITTER state or SILENT state, or after entering the new TRAINING state, and is set to TRUE once the MASTER finishes sending the last MASTER countdown infofield and receiving the responding(last) infofield from the SLAVE at the current TRAINING stage.

loc_rcvr_status

Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY at the current TRAINING stage. This variable is transmitted in the loc_rcvr_status bit of the InfoField by the local PHY.

OK: the receive link for the local PHY is operating reliably

NOT_OK: operation of the receive link for the local PHY is unreliable

loc_SNR_margin

This variable report whether the SLAVE has sufficient SNR margin to start its TX transmission. This usually assumes the loop timing has been achieved. The criteria for setting the parameter is left to the implementer.

OK: the local device has sufficient SNR margin

NOT_OK: the local device does not have sufficient SNR margin

pcs_data_mode

Generated by the PMA PHY Control function and indicates whether or not the local PHY may transition its PCS state diagrams out of their initialization states. The current value of the pcs_data_mode is passed to the PCS via the PMA_PCSDATAMODE.indication primitive.

PMA_tdd_status (TBD??)

This variable indicates the status of the TDD Monitor as described in Figure 200-34 TBD??

OK: TDD burst is detected reliably

NOT_OK: TDD burst is not detected reliably

pma_reset

Allows reset of all PMA functions. It is set by PMA Reset.

Values: ON, OFF

PMA_state

Variable for the value transmitted in the PMA_state<> of the InfoField by the local PHY

Values: 00: TRAINING state, 01 COUNTDOWN state

rem_countdown_done

This variable is only used by the SLAVE. It is set to false when the PHY Control state diagram is in the DSIABLE_TRANSMITTER state or SLIENT state, or after entering the new TRAINING state, and is set to TRUE once the SLAVE receives the last countdown infofield from MASTER and finishes sending one infofield from SLAVE at the current TRAINING stage.

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not. This variable is received in the loc_rcvr_status bit in the InfoField from the remote PHY. This variable is set to NOT_OK if the PCS has not decoded valid InfoFields from the remote PHY

OK: the receive link for the remote PHY is operating reliably

Reliable operation of the receive link for the remote PHY is not detected

tx_mode

The PMA generates this variable continuously and passes it to the PCS via the PMA_TXMODE.indication primitive(200.2.2.1).

SEND_N

SEND_TS

SEND_TA

SEND_TA_EXT

SEND_Z

tx_tdd_active

The PMA PHY control generates this variable continuously and passes it to the PCS via the PMA_TX_TDD_ACTIVE.indication primitive(200.2.2.10)

rx_tdd_active

The PMA PHY control generates this variable continuously and passes it to the PCS via the PMA_RX_TDD_ACTIVE.indication primitive(200.2.2.11)

negotiation_done

During symmetric training phase, after loc_rcvr_status=1, the MASTER and SLAVE shall exchange capabilities, delay_count and negotiated speed, and then set negotiation_done bit.

OK: Negotiation is done, can move to COUNTDOWN0 state

NOK: Negotiation is not done, stay in TRAINING0 state.

200.6.4.2 Timers

All timers operate in the manner described in 14.2.3.3

minwait_timer

A timer used to determine the minimum amount of time the PHY Control stays in the SILENT (…)state. The timer shall expire 500 us(TBD) +/- 50 us after being started

link_fail_inhibit_timer

A timer used to limit the amount of time during which a receiver dwells in the TRAINING and COUNTDOWN state. The timer shall expire 50(TBD) ms +/- 0.5 ms after being started.

MASTER: This timer will be started when MASTER side receive the 1st burst from the SLAVE

SLAVE: This timer will be started when SLAVE side send the 1st burst to the MASTER.

tdd_rx_monitor_timer (TBD)

This timer is used to monitor link quality during the TDD receive mode. If the PHY does not detect reliable TDD signaling before this timer expires then a full retrain is performed.

Values: The condition tdd_rx_monitor_timer_done becomes TRUE upon timer expiration.

Duration: This timer shall have a period equal to 10 complete TDD signal periods, equivalent to (96 us TBD??).

200.6.5 State diagram

The PHY Control state diagram is shown in Figure. 200-32 PHY Control state diagram

The Link Monitor state diagram is shown in Figure. 200-33 Link Monitor state diagram

The TDD monitor state diagram is show in Figure .200-34 TDD Monitor state diagram (TBD)

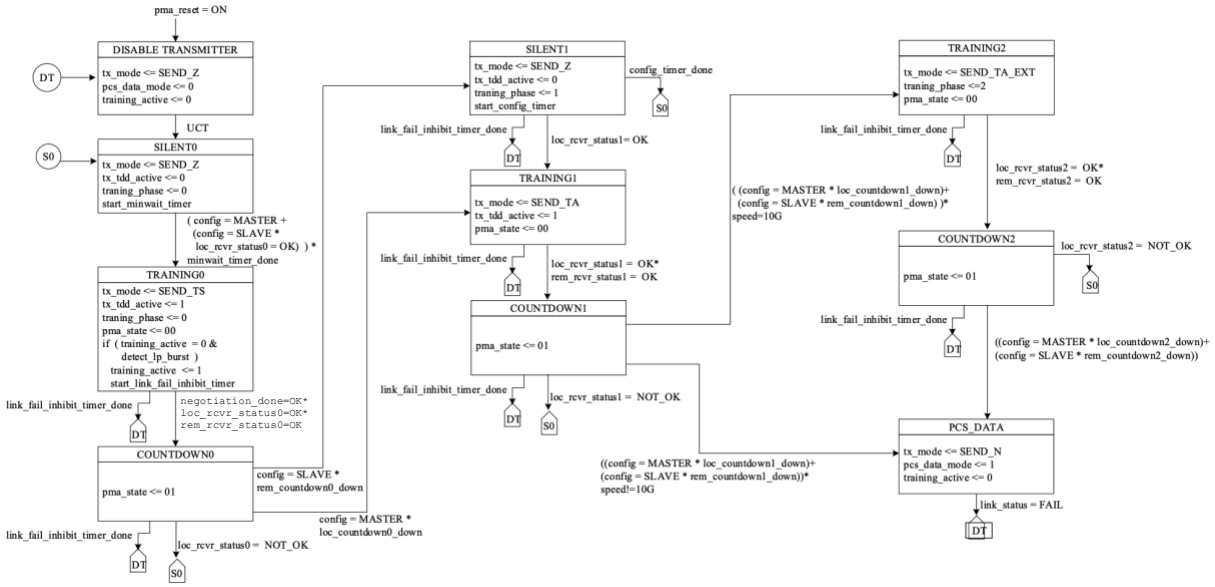


Figure 200-32 PHYC Control state diagram

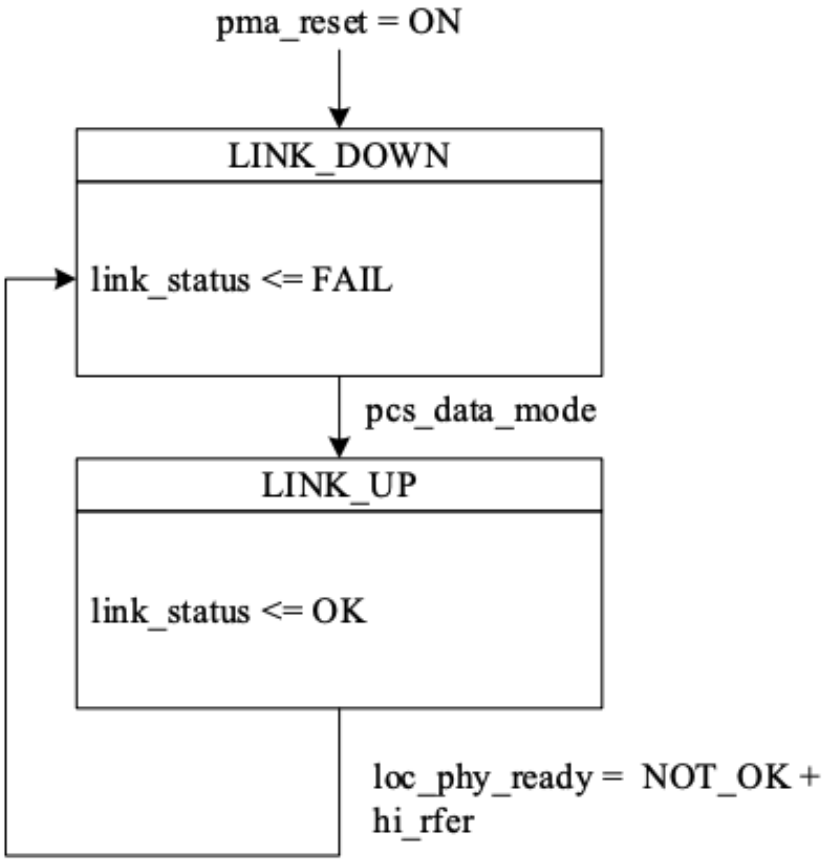


Figure 200-33 Link monitor state diagram

Figure 200-34 TDD monitor state diagram (TBD)

200.7 Physical Medium Attachment (PMA) sublayer, 100M+MultiGBASE-T1/V1

As specified in MultiG+100MBASE-T1/V1 PMA sublayer in 200.6

I did not include all subclauses as they can vary with implementation. You can look at any PHY project that is similar to see which may be needed. Other subclauses may be added as baselines are chosen.

~~**200.7.1 PMA functional specifications**~~

~~**200.7.2 PMA functions**~~

~~200.7.2.1 PMA Reset function~~

~~200.7.2.2 PMA Transmit~~

~~200.7.2.3 PMA Receive function~~

~~200.7.2.4 PHY Control function~~

~~200.7.2.5 Link Monitor function~~

~~200.7.2.6 PHY Link Synchronization~~

~~200.7.2.7 Refresh monitor function Only needed if EEE is implemented.~~

~~200.7.2.8 Clock Recovery function~~

~~200.7.3 MDI, T1~~

~~200.7.3.1 MDI signals transmitted by the PHY~~

~~200.7.3.2 Signals received at the MDI 200.7.4 MDI, V1~~

~~200.7.4.1 MDI signals transmitted by the PHY~~

~~200.7.4.2 Signals received at the MDI~~

~~200.7.5 State variables~~

~~200.7.6 State diagrams~~

200.8. PMA electrical specifications

200.8.1 Test Modes

200.8.1.1 Test fixtures

200.8.2 Transmitter electrical specifications

200.8.2.1 Maximum output droop

200.8.2.2 Transmitter linearity

200.8.2.3 Transmitter timing jitter

200.8.2.3.1 Transmit MDI random jitter in MASTER mode

200.8.2.3.2 Transmit MDI deterministic jitter in MASTER mode

200.8.2.4 Transmitter power spectral density (PSD) and power level

In test mode 5(TBD), the transmit signal on the MDI is as in the normal mode but it is continuous with no quiet gap and refresh period. the Transmit power measured in the test mode 5, shall be in the range specified in the table 200-12 (TBD).

	STP		Coax	
	Min	Max	Min	Max
2.5G/100M	0	2	-3	-1
5G	2	4	-1	1
10G	0	2	-3	-1

Table 200-12 – Power Levels

The power spectral density of the transmitter of 100M+MultiGBASE-T1 and MultiG+100MBASE-T1, measured into a 100 ohm differential load using test fixture 4(TBD) shown in Figure 200- (TBD), shall be between the upper and lower masks specified in Equation 200-14 and Equation 200-15.

The upper and lower masks for each PHY type of 100M+MultiG BASE-T1, MultiG+100MBASE-T1, are shown in Figure 200-34, Figure 200-35 and Figure 200-36. See Table 200-13 for the definition of R (Tx Symbol Rate Scaling factor). See Table 200-14 for the definition of PSD mask K factor.

PHY type	R
100M+MultiG BASE-T1/V1	0.5
2.5G+100M BASE-T1/V1	0.5
5G+100M BASE-T1/V1	1
10G+100M BASE-T1/V1	1

Table 200-13 – Tx Symbol Rate Scaling factor

PHY type	K
100M+MultiG BASE-T1/V1	0
2.5G+MultiG BASE-T1/V1	0
5G+MultiG BASE-T1/V1	0
10G+MulitG BASE-T1/V1	2

Table 200-14 – PSD mask K factor

$$UPSD(f) \begin{cases} -89 - K & \text{dBm/Hz} \quad 40 < f < 1200 \times R \\ -87 - K - f / (600 \times R) & \text{dBm/Hz} \quad 1200 \times R < f < 3000 \times R \\ -80 - K - f / (250 \times R) & \text{dBm/Hz} \quad 3000 \times R < f < 5000 \times R \end{cases}$$

Equation: 200-14

$$LPSD(f) \begin{cases} -93 - K & \text{dBm/Hz} \quad 40 < f < 600 \times R \\ -92 - K - f / (600 \times R) & \text{dBm/Hz} \quad 600 \times R < f < 2400 \times R \\ -86.4 - K - f / (250 \times R) & \text{dBm/Hz} \quad 2400 \times R < f < 3500 \times R \end{cases}$$

Equation: 200-15

Where f is the frequency in MHz

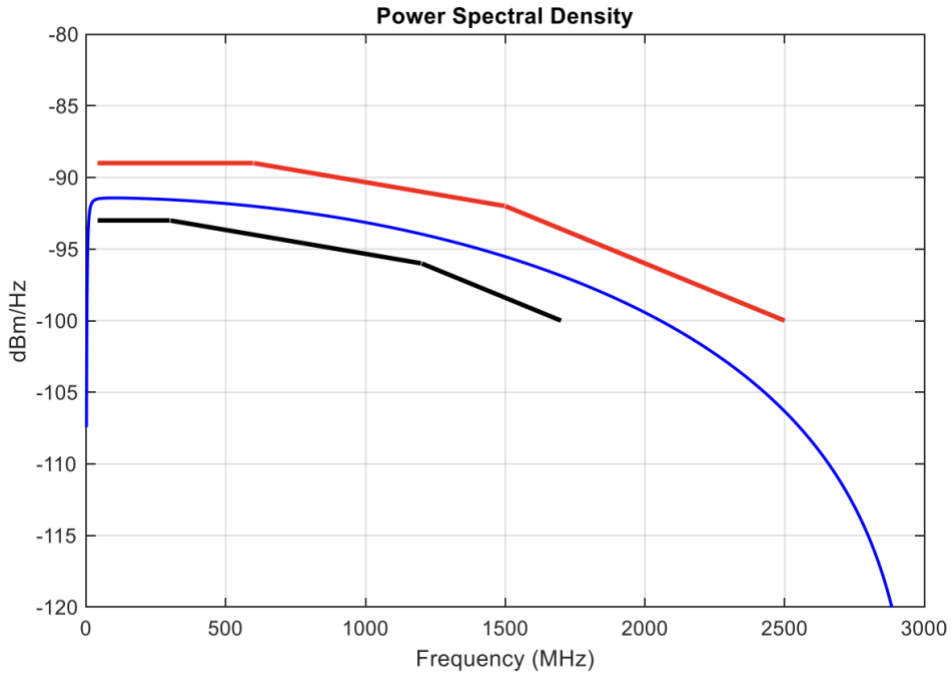


Figure: 200-34(TBD) Transmitter Power Spectral Density for 100M+MultiGBASE-T1 or 2.5G+100MBASE-T1, upper and lower masks

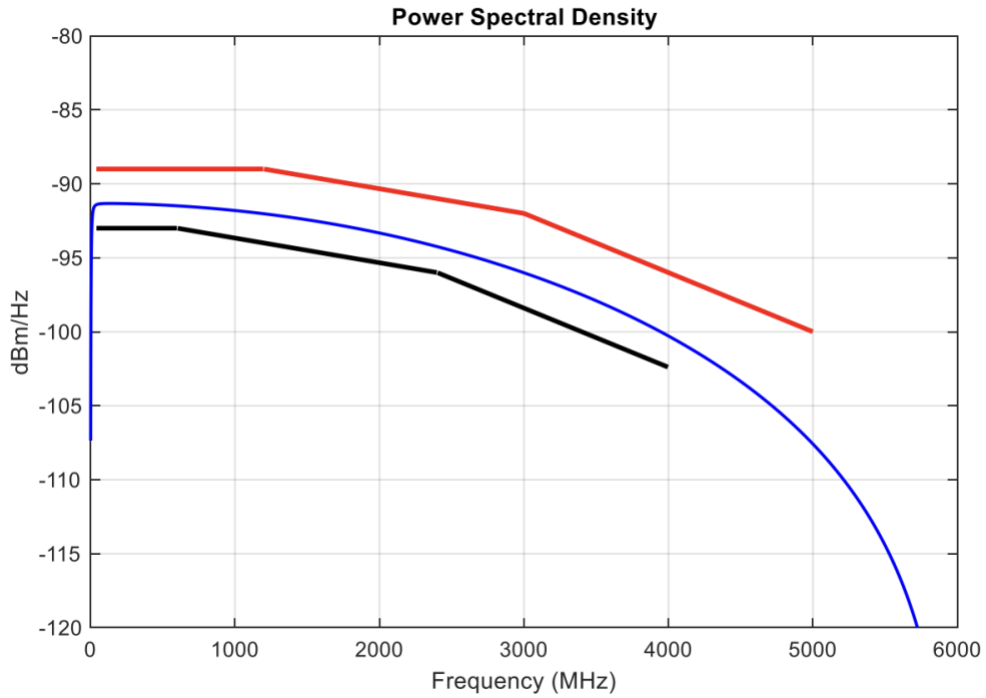


Figure: 200-35(TBD) Transmitter Power Spectral Density for 5G+100MBASE-T1, upper and lower masks

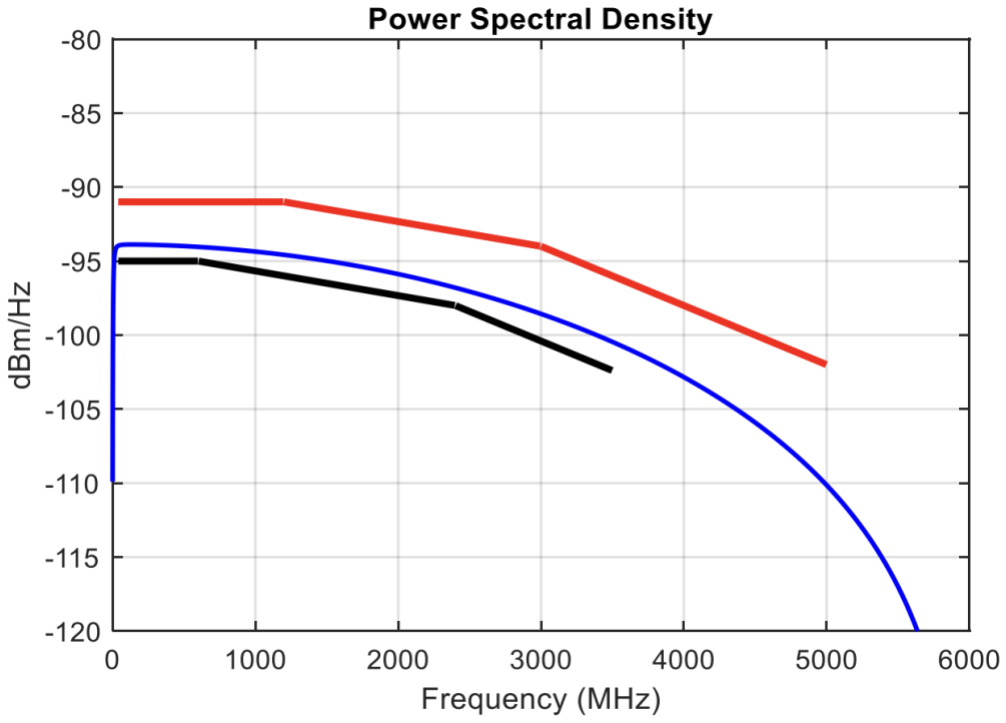


Figure: 200-36(TBD) Transmitter Power Spectral Density for 10G+100MBASE-T1, upper and lower masks

For PHY types 100M+MultiGBASE-V1 or MultiG+100MBASE-V1, with Single Ended termination of 50 ohm, both upper and lower PSD Masks are lower by 3dB from Equation 200-14, Equation 200-15, Figure 200-34, Figure 200-35 and Figure 200-36.

200.8.2.5 Transmitter peak differential output (TBD)

200.8.2.6 Transmitter clock frequency

200.8.3 Receiver electrical specifications

200.8.3.1 Receiver differential input signals

200.8.3.2 Alien crosstalk noise rejection

200.9 Management interface (TBD)

200.10 Link segment characteristics

200.10.1 Link transmission parameters

200.10.1.1 Insertion Loss

200.10.1.1.1 Insertion loss for 100M+MultiGBASE-V1 and MultiG+100MBASE-V1 PHY

The link-segment insertion loss for 100M+MultiGBASE-V1 and MultiG+100MBASE-V1 link segment shall meet the values determined using Equation 200-16

$$IL \leq 15\left(0.000055f + 0.023\sqrt{f} + \frac{0.032}{\sqrt{f}} + 0.02\right) - 0.05\sqrt{f}$$
$$f\ in\ MHz, f \geq 10\ MHz$$

Equation: 200-16

The insertion loss is illustrated in Figure 200-38

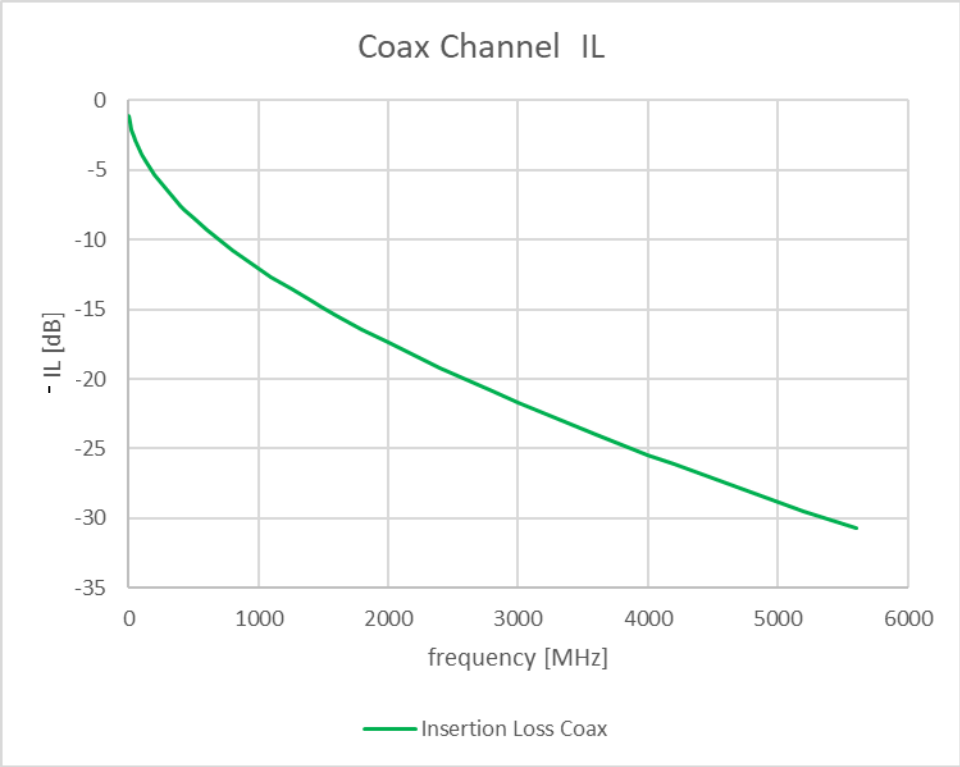


Figure: 200-38 Insertion loss calculated using Equation 200-16

200.10.1.1.2 Insertion loss for 100M+MultiGBASE-T1 and MultiG+100MBASE-T1 PHY (TBD)

200.10.1.2 Differential characteristic impedance

200.10.1.3 Return loss

200.10.1.3.1 100M+MultiGBASE-V1 and MultiG+100MBASE-V1 link segment return loss

The link segment return loss shall meet the values determined by using Equation (200- 17) at all frequencies from 10MHz to 5GHz. The reference impedance for the return loss specification is 50 ohm.

$$RL \geq \begin{pmatrix} 12.5 & 10\ MHz \leq f < 500\ MHz \\ 12.5 - 3\frac{f-500}{1500} & 500\ MHz \leq f < 2000\ MHz \\ 9.5 - 3\frac{f-2000}{2500} & 2000\ MHz \leq f < 4500\ MHz \\ 6.5 & 4500\ MHz \leq f \leq 5000\ MHz \end{pmatrix} \text{dB}$$

Equation: 200-17

Where f is the frequency in MHz;

The return loss is illustrated in Figure 200-39 [editorial Note: New plot with RL limit only]

Figure: 200-39 Return loss calculated using Equation 200-17

200.10.1.3.2 100M+MultiGBASE-T1 and MultiG+100MBASE-T1 link segment return loss (TBD)

200.10.1.4 Coupling attenuation

200.10.1.5 Screening attenuation (..??)

200.10.1.6 Maximum link delay

200.10.2 Coupling parameters between link segments

200.10.2.1 Power sum alien near-end crosstalk (PSANEXT)

200.10.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

200.11 MDI specification

200.11.1 MDI connectors

200.11.2 MDI electrical specification

200.11.2.1 MDI return loss

200.11.3 MDI fault tolerance