Comments on the 802.3dm Complexity and EMC performance

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Foreword

- It was shown earlier[1] that a CLTE+DFE equalizer can be used to provide a very good performance for a 2.5Gbps TDD receiver.
- There was a claim that suggested TDD receiver on the camera side is 250% more complex than a FDD[2] receiver. Those assumptions made and the estimates do not agree with an actual implementation of a SerDes receiver that is provided in this presentation.
- A 3Gsps slicer was implemented to confirm the area. It is noted that some receiver blocks are smaller for higher bandwidth signaling. The overall area estimation shows that the receiver blocks considered in comparison are not larger than those for FDD[2].
- Additionally, this presentation addresses testing requirement for EMC verification of a PHY solution. Some of the parameters affecting the test results and long-term performance is discussed.

1- https://www.ieee802.org/3/dm/public/0325/Chini_3dm_02b_0325.pdf

2- https://www.ieee802.org/3/dm/public/0325/[redacted]_FDD_PHY_Simulation_Results_and_PHY_Complexity_rev1p0.pdf

The Claim on TDD and ACT Receiver Complexity versus FDD[1]

- A contribution to 802.3dm compared the complexity of FDD[1] with TDD and ACT.

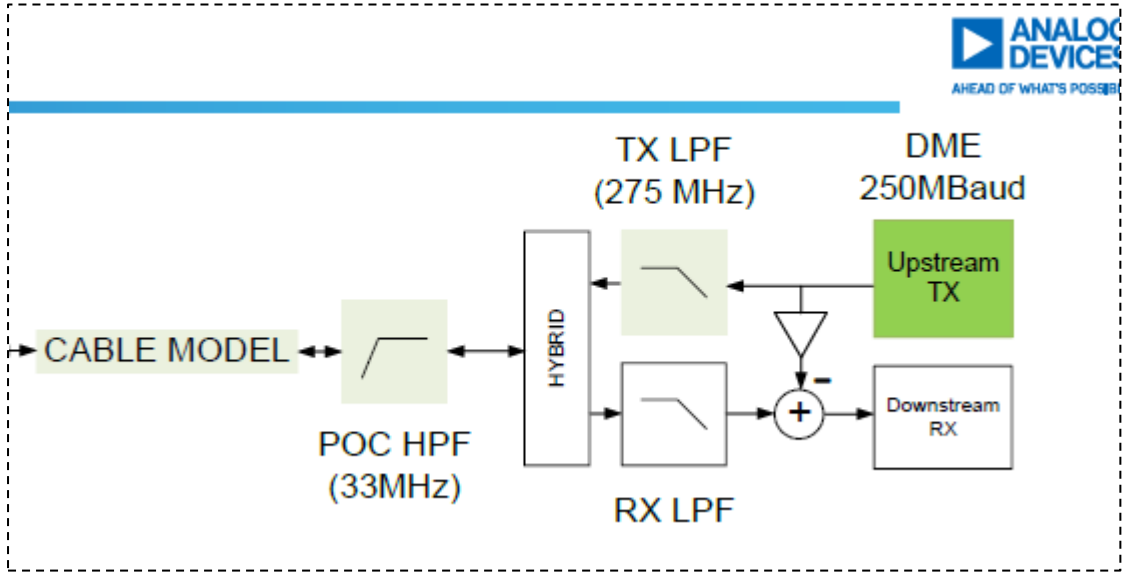
	FDD[1]	ACT	TDD
Camera Receiver Complexity	Much Less Complex	Much Less Complex	Much more complex > 250%
High Speed receiver Complexity (ECU side)	Least Complex	Most Complex > 200%	More Complex

- This earlier presentation[1] claimed that the receiver complexity is 250% larger in the camera side for TDD and 200% larger in the ECU side for ACT.
- The suggested block diagram for FDD[1] receiver is shown in the next two pages with comments.

1- https://www.ieee802.org/3/dm/public/0325[redacted]E_FDD_PHY_Simulation_Results_and_PHY_Complexity_rev1p0.pdf

FDD[1] Receiver Block Diagram, ECU (High Speed) Side

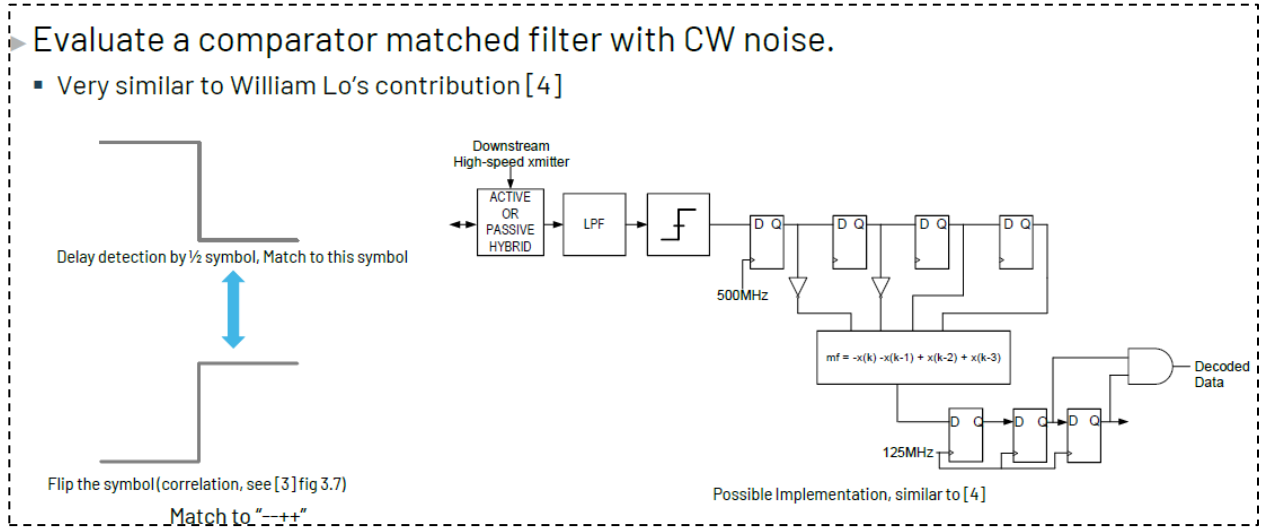
- A high-level ECU receiver for FDD[1] is shown to use an **echo canceller**. The details of the receiver and echo cancellation filter is not provided.
- ACT is said to be 200% more complex, noting long FFE and some DFE.
- TDD is marked as “more complex” than FDD[1] for the ECU side(!) but there is no design or detailed quantitative analysis to support this claim. TDD does not have an echo canceller and uses a smaller FEC than proposed for FDD[1].
  How can the TDD receiver on the ECU side be more complex than FDD which has an echo canceller[1]?!



1- https://www.ieee802.org/3/dm/public/0325/[redacted]_FDD_PHY_Simulation_Results_and_PHY_Complexity_rev1p0.pdf

FDD[1] Receiver Block Diagram, Low Speed Side

- For low-speed side, the receiver block diagram used for complexity comparison is like an earlier presentation[2] where area is estimated to be 0.012mm^2.
- The LPF is a 2nd order Butterworth.
- Sampling Clock is 500MHz.
- Clock frequency and phase synchronization and tracking is not addressed in this implementation. The phase interpolator to tune clock phase and frequency is missing in the diagram.



1- https://www.ieee802.org/3/dm/public/0325/[redacted]_FDD_PHY_Simulation_Results_and_PHY_Complexity_rev1p0.pdf

2- https://www.ieee802.org/3/dm/public/0125/Lo_3dm_02a_0125.pdf

TDD Equalizer Area on the Camera Side

- Two equalization formats have been discussed[1] for TDD.
  1. CTLE + VGA + DFE +Slicer
  2. CTLE + Slicer
- For the upstream, TDD signal baud rate is 3Gsps and duty cycle is less than 6%. The processing rate is only **175Msps** including the refresh period (as compared to **500Msps** for FDD[1]).
- A **10G SerDes PHY** in 16nm used to estimate area for TDD equalizer area.
- SerDes design experts suggest only 30% to 40% reduction in area when running in 3Gsps.
- The following blocks considered in the estimation to calculate the total area of **0.0108mm^2** for 3Gsps analog equalizer.

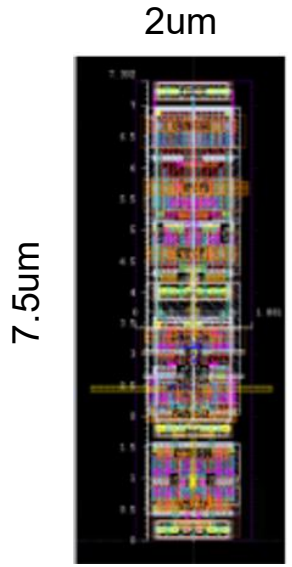
CTLE
Variable Gain Amplifier + Adder
DFE + S/P
Two Slicers (for data and error)
Slicer Calibration circuit
Phase Interpolator (for re-timer)

Note: Calibration and phase interpolator is missing from the suggested FDD receiver.

1- https://www.ieee802.org/3/dm/public/0325/[redacted]_FDD_PHY_Simulation_Results_and_PHY_Complexity_rev1p0.pdf

TDD Equalizer area in the Camera side, continued

- A simpler Camera receiver design uses a CTLE plus Slicer. CTLE is basically a filter and the RC components for a filter are smaller when bandwidth is higher.
- The slicer runs at 3GHz versus 500MHz for ACT. A circuit was designed to estimate the 3Gsps slicer area in 16nm technology.
- The area of a single slicer which runs at 3GHz is only 15um^2 or 0.000015mm^2
- A good receiver will have a slicer offset calibration circuit which is much larger in area than slicer itself. The calibration circuit however runs on a slow rate and would not be more than what is needed for a 500MHz slicer.
- Including CLTE + Slicer + Calibration circuit + Phase Interpolator + S/P, the estimated area for this simpler implementation is less than **0.005mm^2**



Blocks in a 10G SerDes PHY (PMA)

- Review of a 10G SerDes PHY shows that the portion of the receiver dedicated to a mixed mode equalizer (CLTE and DFE) is not more than **10%** of the total PHY-PMA area in a 10G SerDes PHY-PMA.
  - SerDes PHYs are designed to transmit on one lane and receive on another lane (two lanes).
  - There is a separate termination circuits for each lane. The line termination includes differential and common mode circuits.
  - There are pads and ESD protection blocks for each of the two pins of a transmitter and separately for the receiver.
  - For a single PHY, PLL area is larger than 50% of total PMA area. Along with clock distribution channels, almost 60% of PHY-PMA area is used for PLL and clock channels. The rest of the PHY PMA area is divided between RX and TX blocks.
  - The pads (bumps), ESD protection, terminations (for differential mode and common mode) , the AC coupling and supervisory circuits take majority of PMA receiver area.
  - Note that for TDD transceiver, the TX/RX terminations and ESD protection circuits are shared.

PHY-PCS complexity

- Scrambler/descrambler and FEC coding/decoding are part of PCS. The PCS block that is dominant in complexity is FEC decoder.
- RS FEC decoders can significantly grow in complexity (area) with the code length and GF radix. FEC codes proposed to 802.3dm for downstream is as following:
  - **TDD** proposal is RS (130, 122, 8bit)
  - **FDD**[1] proposal is RS (144, 122, 8bit)
  - **ACT** proposal is RS (360, 326, 10b)
- The RS decoder of ACT at ECU side, is at least **400%** higher than the one proposed for TDD (the verified area from the actual implementations is even more than this!).
- For TDD, the FEC decoding is not required (optional) for 2.5Gbps since dp-SNR has a large margin for 1e-12 BER requirement.

1- https://www.ieee802.org/3/dm/public/0325/[redacted]_FDD_PHY_Simulation_Results_and_PHY_Complexity_rev1p0.pdf

Comments on EMC performance

- To verify emissions, one should test with both AVERAGE and the PEAK detectors.
- When looking into emission using PSD of transmit signal, one should know that the PSD is a measure of long-term average transmit power, not the temporary peak.
- The peak spectrum is measured after passing through a narrowband filter specified by resolution bandwidth (RBW). The filter combines the adjacent symbols and with certain patterns appearing temporarily in the filter band, then the larger peaks are observed. Therefore, PSD alone can not be used to predict peak emission.
- Another factor to consider for EMC is the mixed cable types. The testing should confirm the EMC performance for mixed cable segments combing RG175 and RTK031 types and not only RTK031.
- The final judgement on emission is in-car test results. Multiple link segment formats and various lengths should be measured in several different car types to evaluate the EMC performance (Emissions and Immunity).

Comments on EMC Performance, continued

- The effect of aging (mechanical + temperature) on **screening attenuation** of the flexible portion of link segment is shown to be quite severe. A new cable used for EMC testing does not reveal the performance over a longer period. It is important to optimize for best EMC performance practically possible to minimize the risk of emissions or the immunity for the longer period.
- Putting constraints on aging does not resolve the aging problem. It just makes a PHY solution less appealing than the others for automotive applications.
- For automotive immunity performance, two fundamental parameters are the **Transmit Level and cable Insertion Loss.** FEC does not correct for CW or long RF pulse noises. If a PHY proposal suggests a transmit level that is significantly less than proven incumbents, and at the same time cable insertion loss that is significantly more than incumbents, then there is a risk that a PHY built on such a proposal fails immunity in real use cases.
- A bench performance does not guarantee in-car performance. Such a PHY may practically be limited to shorter cable length for the automotive applications.

Summary and conclusion

- Review of a SerDes PHY-PMA shows the CTLE+DFE equalizer is not more than 10% of total PHY area.
- For a 3Gsps receiver, the estimated area for an equalizer plus re-timer is between 0.005mm^2 to 0.011mm^2 depending on DFE and other supporting blocks. Adding area for a 130B FIFO, the area is not more than 0.012mm^2 projected for an ACT/FDD[1,2] receiver.
- Based on some existing PHYs, the FEC decoder area was compared for the 10bit RS code specified for ACT (high speed direction) and the 8bit RS code specified for TDD. The area of ACT-FEC decoder is larger by more than 400% than TDD-FEC.
- On EMC verification, important details on PEAK emission measurement and setup factors; cable types, In-car versus bench verification and aging effect on EMC were discussed. Limiting aging with specification, does not help long-term performance, it rather makes a proposal less attractive.
- It is also noted that, a proposal to 802.3dm which suggests a transmit level less than proven incumbents for 2.5Gbps/5Gbps, It has immunity risk for automotive applications. Alternatively, it must be used for shorter links.

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2- https://www.ieee802.org/3/dm/public/0125/Lo_3dm_02a_0125.pdf

Thank you

Questions?