Summary of Latest Updates to PCS/PMA Logic for ACT/GMSLE Transceiver

William Lo

July 29, 2025

Objective

- Summarize points of consensus on PCS and PMA logic of ACT/GMSLE PHY
  - Make it easier to generate and understand text

- Things that did not change from Lo_3dm_01_051425.pdf in backup slides

64/65 Encoder/Decoder

Downstream

- No change to clause 149

Input Data	data ctrl header	Block Payload							
Bit Position: / Data Block Format:	0	1							64
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block							
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Upstream

- Transmit – no change to clause 149
- Encoder and Decoder state machines identical

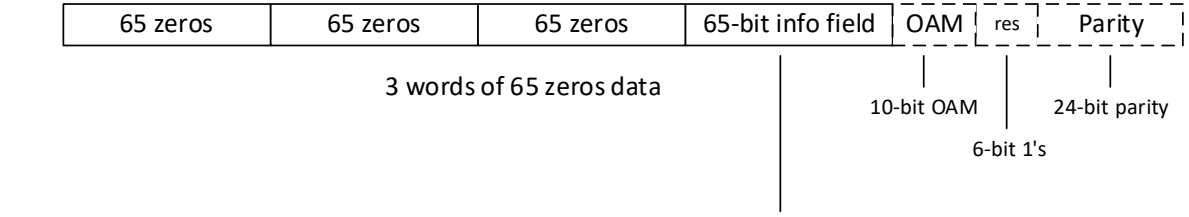
Training Frame

Downstream

- No change in logical framing to clause 149 except speed change
- 10G - No change 5.625 Gbaud
  - Training frame duration is 4 RS-Frame time
- 5G - 5.625 Gbaud
  - Was 2.8125 Gbaud in 802.3ch
  - Training frame duration is now 2 RS-Frame time
- 2.5G – 2.8125 Gbaud
  - Was 1.40625 Gbaud in 802.3ch
  - Training frame duration is now2 RS-Frame time

Upstream

- Baked into the data path
- Same DME signaling
- No countdown needed



C/D								
1	Block	D0	D1	D2	D3	D4	D5	D6
1	0x5A	Reserved	Reserved	Reserved	Message	PHY Capability Bits		

Training Infofield

Downstream

- Message Field – Same as clause 149
- PHY Capability Bits
  - Eliminate – InterleaverDepth
  - Eliminate – PrecoderSel

Upstream

- Message Field – Same as clause 149
- Eliminate Partial Frame Count
- Simplification of PHY Control state diagram
  - No countdown needed
  - See next side

PHY Control State Machine

- Similar to 802.3ch
  - Changes in red
- New variable: phy_role
  - US_TX : 100M+MultiGBASE-T1/V1 PHY
  - DS_TX : MultiG+100MBASE-T1/V1 PHY
- 100M+MultiGBASE-T1/V1 PHY
  - Send complete set of infofield training frames with PMA_state = 01 before SEND_N
  - Wait for countdown to be done on high speed receive
- MultiG+100MBASE-T1/V1 PHY
  - Transmit training frames until countdown is done on high speed transmit

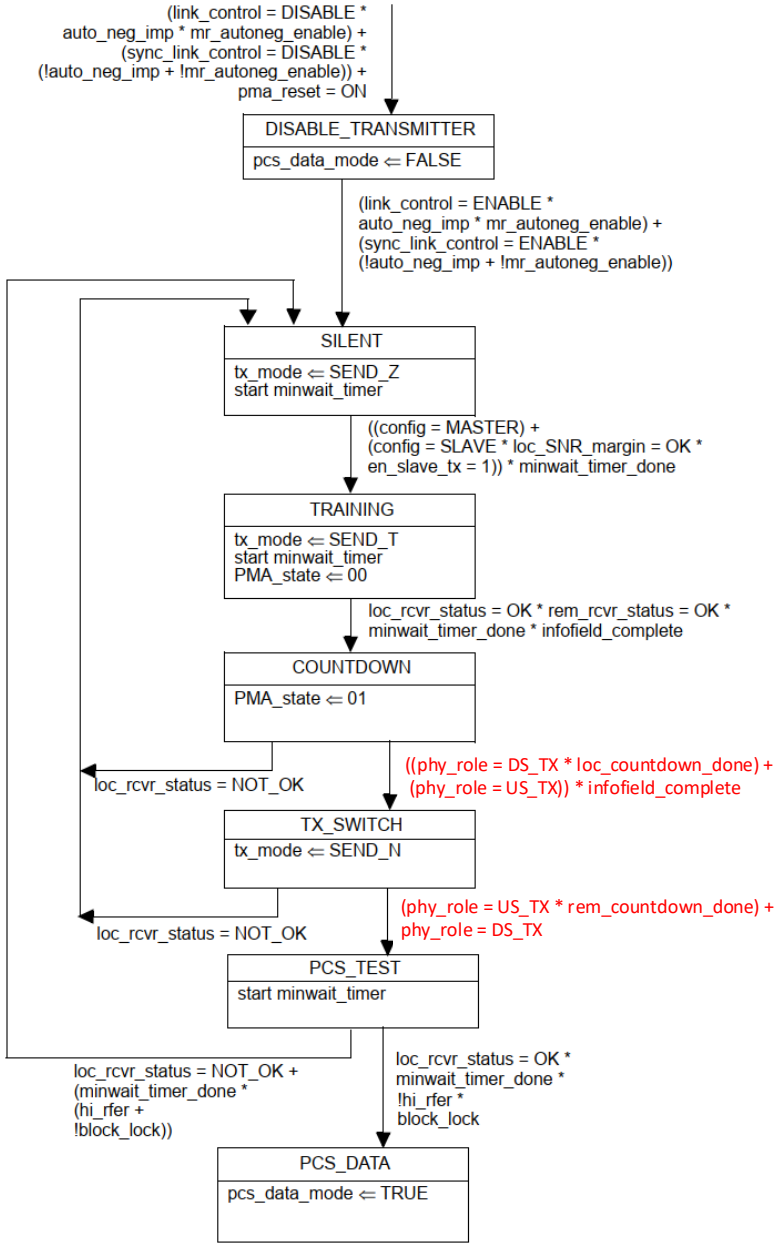
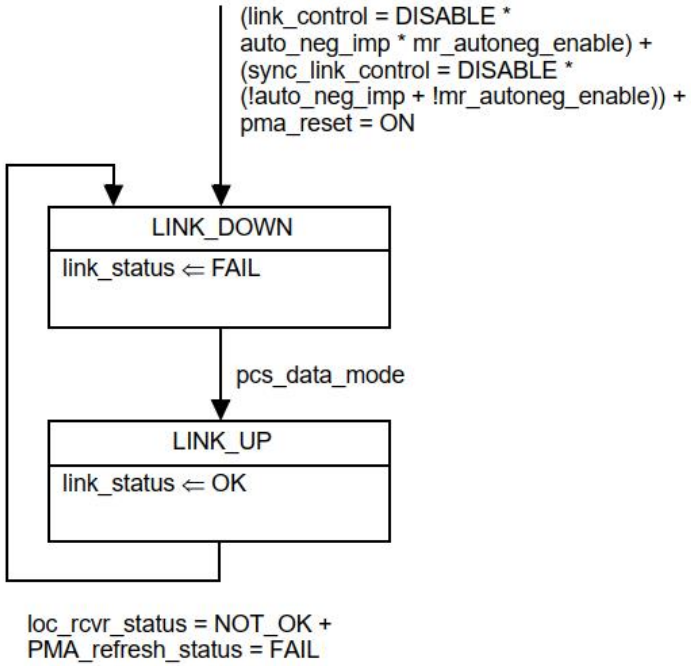


Figure 149–32—PHY Control state diagram

Link Monitor State Diagram

- Same as 802.3ch



Link Sync

- Text in development
- Based on:
  - https://www.ieee802.org/3/dm/public/050125/Lo_3dm_01_050125.pdf
  - Offline discussions on whether or not to remove randomization
  - Proposed timers may be reduced with elimination of randomization
- Pulse is 4-bit pattern at 117.1875 MHz converted to DME symbols for upstream and downstream.
  - Study on best pattern(s) to use

Auto-Negotiation

- Priority Resolution
- See Lo_3dm_02_072925.pdf for explanation

		Link Partner																							
		25GBASE-T1	10GBASE-T1	100M+10GBASE-T1/V1 (L)	100M+10GBASE-T1/V1 (F)	10G+100MBASE-T1/V1 (L)	10G+100MBASE-T1/V1 (F)	5GBASE-T1	100M+5GBASE-T1/V1 (L)	100M+5GBASE-T1/V1 (F)	5G+100MBASE-T1/V1 (L)	5G+100MBASE-T1/V1 (F)	2.5GBASE-T1	100M+2.5GBASE-T1/V1 (L)	100M+2.5GBASE-T1/V1 (F)	2.5G+100MBASE-T1/V1 (L)	2.5G+100MBASE-T1/V1 (F)	1000BASE-T1	100BASE-T1L	100BASE-T1	10BASE-T1S Full Duplex	10BASE-T1S Half Duplex	10BASE-T1L
PHY	25GBASE-T1	1																						
	10GBASE-T1		2																					
	100M+10GBASE-T1/V1 (L)						3																	
	100M+10GBASE-T1/V1 (F)					4																		
	10G+100MBASE-T1/V1 (L)				4																			
	10G+100MBASE-T1/V1 (F)			3																				
	5GBASE-T1							5																
	100M+5GBASE-T1/V1 (L)											6												
	100M+5GBASE-T1/V1 (F)										7													
	5G+100MBASE-T1/V1 (L)									7														
	5G+100MBASE-T1/V1 (F)								6															
	2.5GBASE-T1												8											
	100M+2.5GBASE-T1/V1 (L)																9							
	100M+2.5GBASE-T1/V1 (F)															10								
	2.5G+100MBASE-T1/V1 (L)														10									
	2.5G+100MBASE-T1/V1 (F)													9										
	1000BASE-T1																	11						
	100BASE-T1L																		12					
	100BASE-T1																			13				
	10BASE-T1S Full Duplex																				14			
	10BASE-T1S Half Duplex																					15		
	10BASE-T1L																							16

New Registers

- Device 1 – Add 802.3dm capabilities (total 12 capabilities)
  - Ability register (See register 1.77.11:0 in text)
  - Control register (See 1.2100.4:0 settings 16 to 27 in text)
- Device 7 - Add 802.3dm capabilities
  - Auto-Negotiation Technology Ability Field Assignments (6 new bits)
  - A11 to A16 used (See 98B.3 in text)

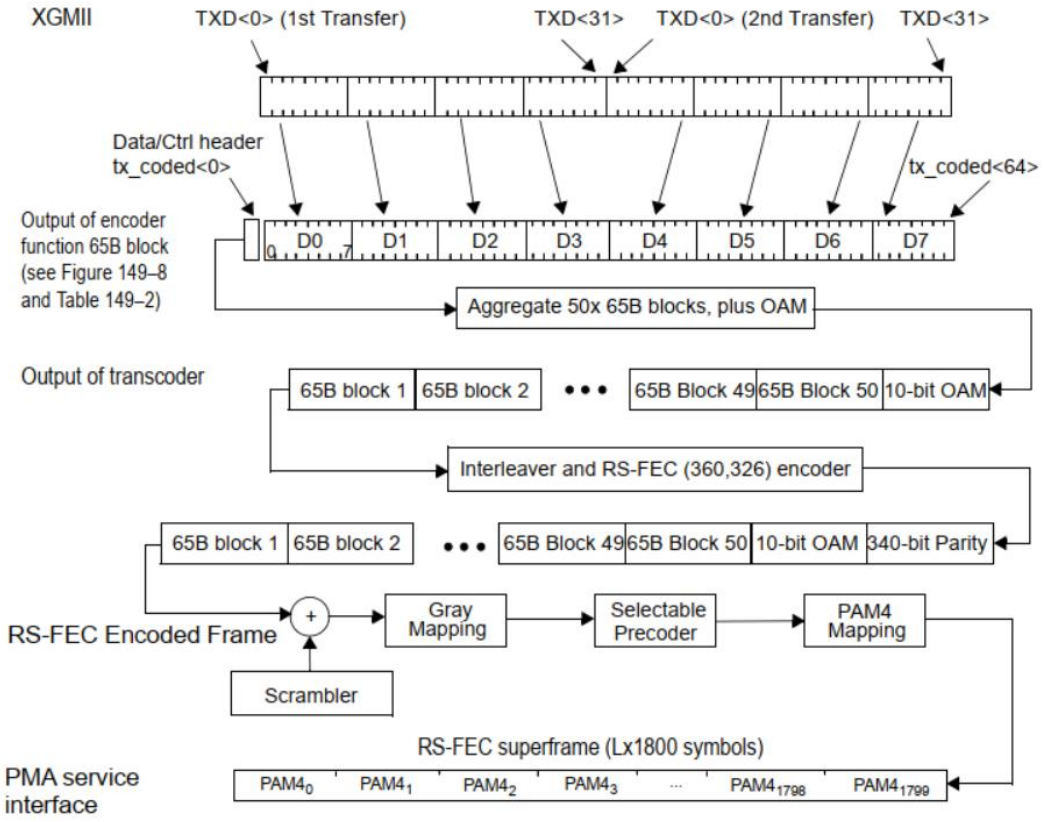
SAME AS

LO_3DM_01_051425.PDF

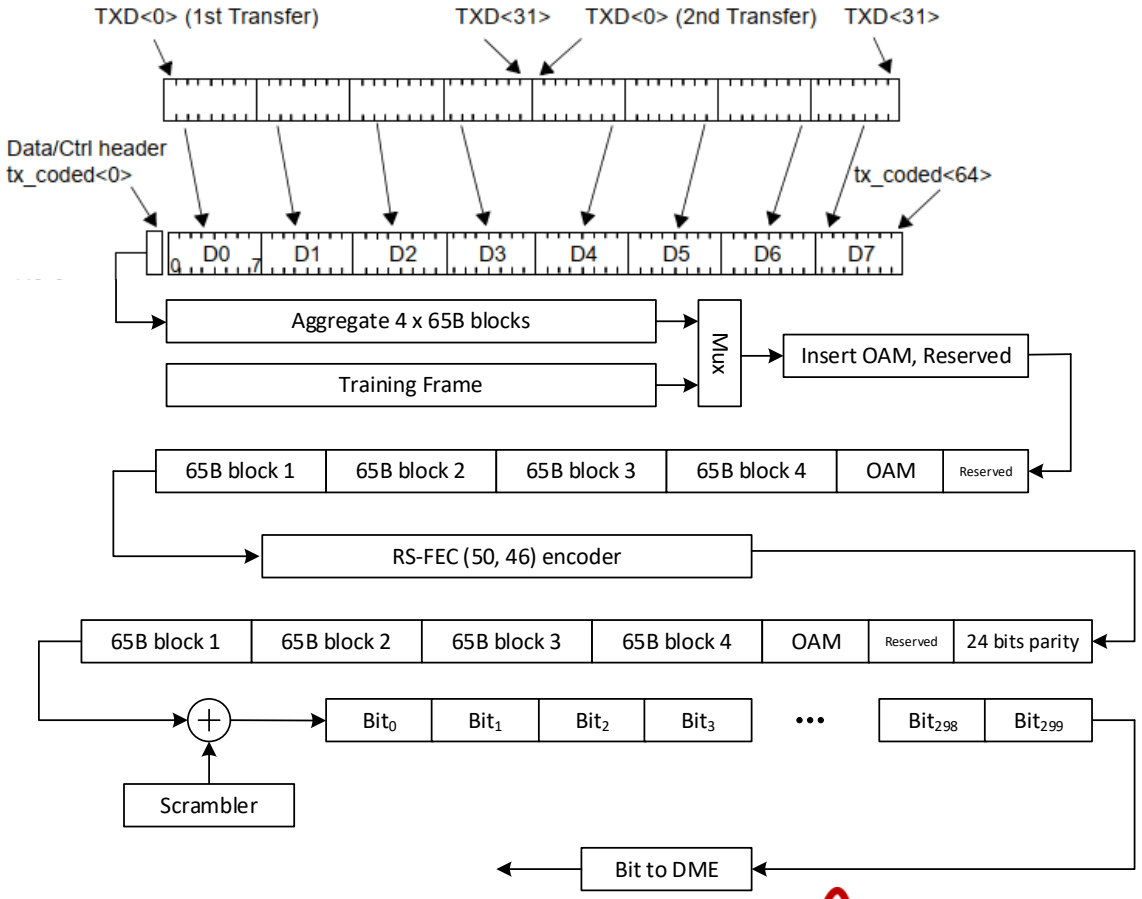
Transmit Path Overview

Downstream

- No change to clause 149



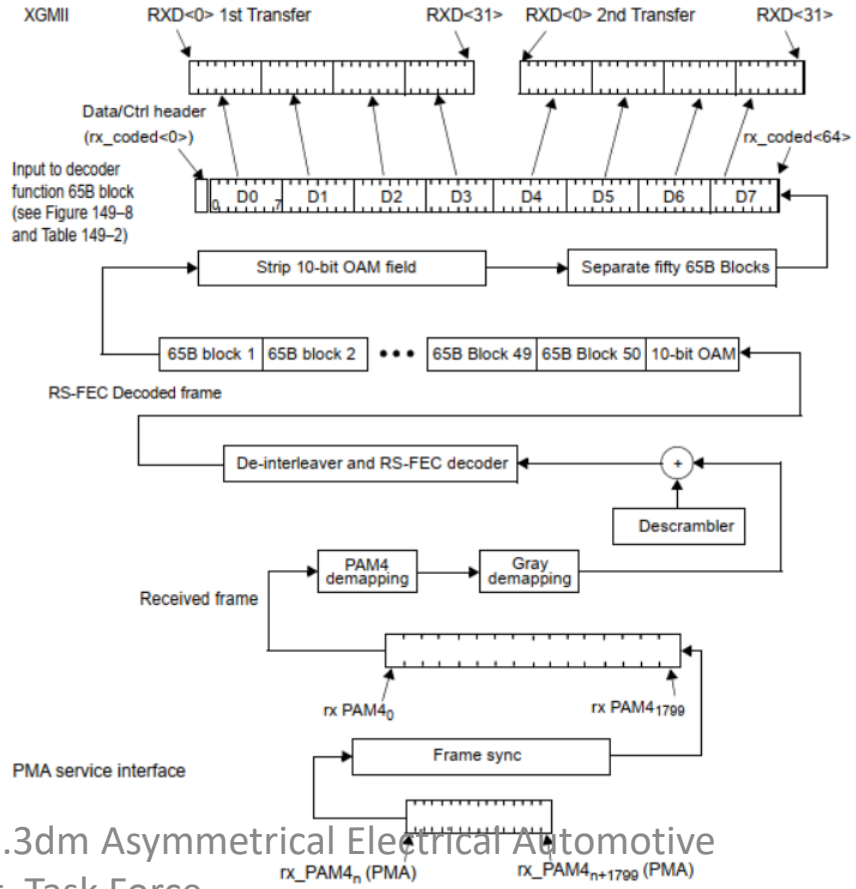
Upstream



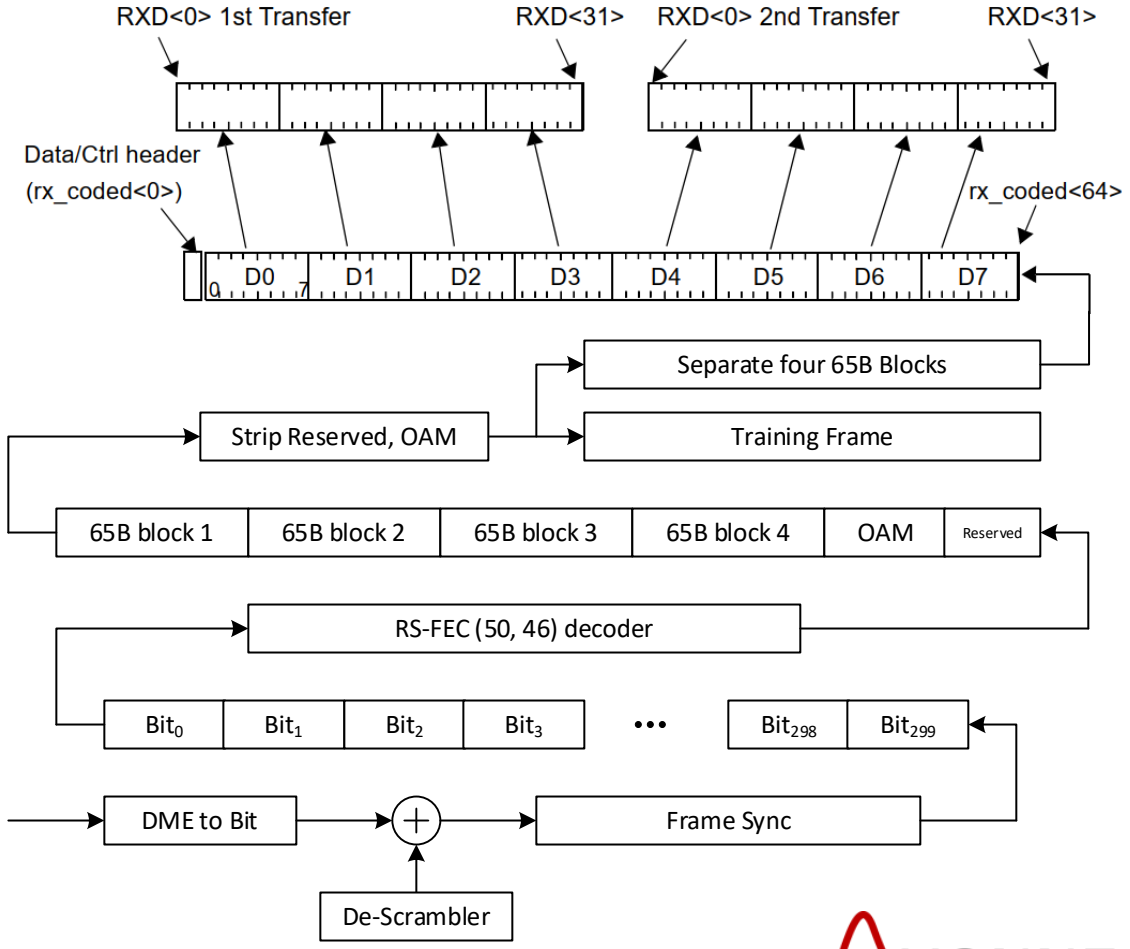
Receive Path Overview

Downstream

- No change to clause 149



Upstream



XGMII and Reconcilation Sublayer

Downstream

- No change to clause 46

Upstream

- No change to clause 46
- Clock speed is 1/100 of 10G.
  - Nominally 1.5625 MHz Clock
- Note
  - 100M MAC coupled to a reconciliation sublayer that supports start/terminate symbols and ordered set

Block Aggregation

Downstream

- No change to clause 149
- 50 blocks of 64/65 + 10-bit OAM

Upstream

- 4 blocks of 64/65 + 10 bit OAM + 6 bits (all 1’s)

Reed Solomon

Downstream

- No change to clause 46
- RS(360, 326) GF(2^{10})
- g(x) = $\prod_{j=0}^{33}(x - \alpha^j)$
- $\alpha = x^{10} + x^3 + 1$
- no, 2x, 4x interleave – 10G
- no, 2x interleave – 5G
- no interleave – 2.5G

Upstream

- RS(50, 46) GF(2^6)
- g(x) = $\prod_{j=0}^{3}(x - \alpha^j)$
- $\alpha = x^6 + x + 1$
- no interleave

Scrambler/Descrambler

Downstream

- 802.3ch
  - Master: $g(x) = x^{33} + x^{13} + 1$
  - Slave: $g(x) = x^{33} + x^{20} + 1$
- 802.3dm
  - $g(x) = x^{33} + x^{20} + 1$
  - Independent of Master vs. Slave

Upstream

- $g(x) = x^{33} + x^{13} + 1$
- Independent of Master vs. Slave

Bit to Line Mapping

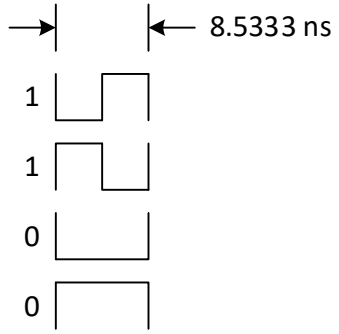
Downstream

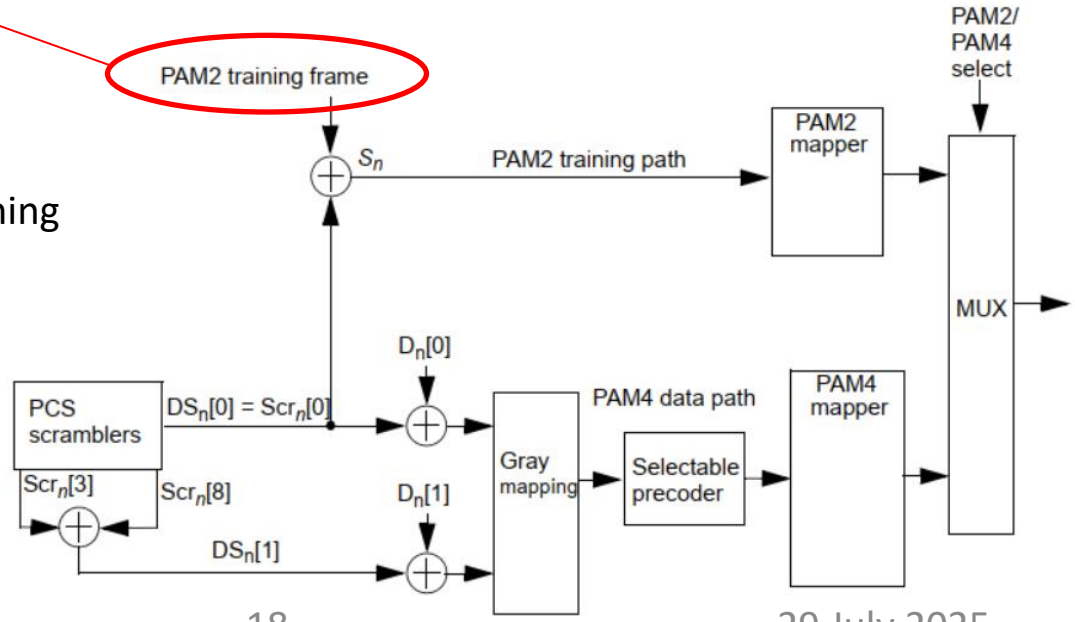
- 10G – no change from clause 149
  - 5.625 Gb/s PAM4 symbols
- 2.5/5G use training path for PAM2 PCS data
  - 5.625 Gb/s PAM2 – 5G
  - 2.8125 Gb/s PAM2 – 2.5G
  - Maintain same mapping as PAM2 training

    0 ➔ +1, 1 ➔ -1

Upstream

- Bit to DME





OAM

Downstream

- No change to clause 149

Upstream

- No change to clause 149
  - Pack 10-bit symbol onto RS frame

Reuse Existing Registers

- 1.2309 – PMA Control
- 1.2310 – PMA Status
- 1.2311 – Training
- 1.2312 – Link Partner Training
- 1.2313 – Testmode Control – (may need modification??)
- 1.2314 – SNR
- 1.2315 – Minimum SNR
- 1.2316 – User defined Register
- 1.2317 – Link Partner User defined Register

Reuse Existing Registers

- 3.2308 – OAM Transmit
- 3.2309 to 3.2312 – OAM Message
- 3.2313 – OAM Receive
- 3.2301 to 3.2317 – Link Partner OAM Message
- 3.2318 to 3.2319 – OAM Status Message
- 3.2320 to 3.2321 – Link Partner OAM Status Message

Reuse Existing Registers

- 3.2322 – PCS control except bit 14 loopback does not apply
- 3.2323 – PCS Status
  - bits 8 to 11 may or may not apply
- 3.2324 – PCS Status 2

THANK YOU