Support document providing comparison information for the options for 802.3dm

IEEE 802.3dm

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2. Motivation.

- Currently, two technical proposals are competing within IEEE 802.3dm.
- The fundamental difference between the two proposals is in their selected duplexing schemes.
- This documents compares the two proposals and the different rationales.
- It may serve as a “technically qualified overview at a glance” reference for individuals wanting to understand and form their own opinion.
- The intention with this comparison document is
  - to clarify where there are agreements and disagreements.
  - to make the disagreements understandable.
- This document
  - does not present a unified opinion.
  - does not favor one proposal over the other.
- The authors who prepared this document intend it as an unbiased reference.

3. Duplexing methods (1)

- TDD — Proposed in dm

Symmetric or asymmetric DS and US traffic alternate at, more or less, the same frequencies.

- SCT — Used in e.g. ch

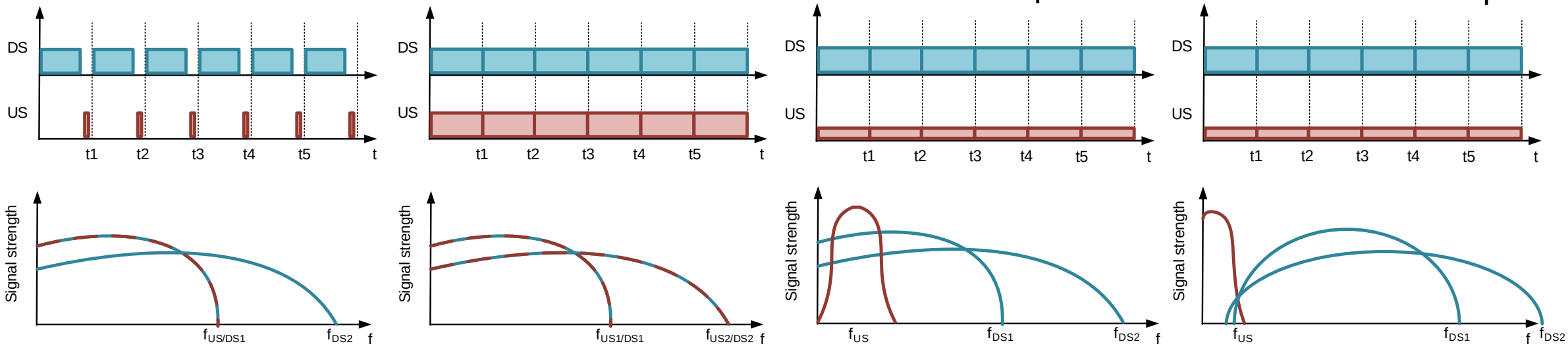
Symmetric DS and US traffic are transmitted concurrently at the same frequencies.

- ACT — Proposed in dm and used in some incumbents

Asymmetric DS and US traffic are transmitted concurrently at different frequencies with full overlap.

- FDD — Used in some incumbents

Asymmetric DS and US traffic are transmitted concurrently at different frequencies with minimal overlap.



DS = Downstream (high-speed in case of asymmetry)
US = Upstream (low speed in case of asymmetry)

FDD = Frequency Division Duplexing
TDD = Time Division Duplexing

SCT = Symmetric Concurrent Transmission
ACT = Asymmetric Concurrent Transmission

3. Duplexing methods (2)

TDD

- DS line rate needs to accommodate US traffic, guard times, and resynch header.
- US transmitter and receiver work at a frequency similar to that of DS.
- Requires PHY FIFOs for rate adaptation.
- Trade off between PHY latency and DS line rate increase.
- Change of high-speed direction requires mainly reversing DS and US burst lengths.
- PHY signal transmission per direction has gaps to accommodate reverse direction.
- Transmission at xMII would be continuous.

ACT

- DS line rate only accommodates DS traffic and may be somewhat lower than for TDD.
- US transmitter and receiver work at a much lower frequency than the DS.
- Rate adaptation not necessary.
- No trade off between PHY latency and DS line rate.
- To use low-speed direction for high-speed not easily possible.
- PHY signals are transmitted continuously (unless EEE).
- Transmission at xMII would be continuous.

1) These slides make no statement on to what degree the differences actually matter. Whether or not they matter is a question of exact system parameters, implementation, and perspective of user. They are listed to help the following, more detailed comparison discussion.

3. Duplexing methods (3)

TDD

- Energy only of either DS or US signals on the channel.
- Peak PSD is lower than for ACT in case of the same DS power.
- No need for a hybrid to separate US and DS signals at the US and DS receivers.
- No trade-off between signal overlap and effort to separate the signals.
- No handling of residual echo required.
- High flexibility between the ratio of US and DS data rates.
- Not affected by near-end cross talk.

ACT

- Energy of DS and US signals simultaneously on channel.
- Peak PSD is higher than for TDD in case of the same DS power.
- Needs a hybrid to separate US and DS signals at the US and DS receivers.
- Trade-off between signal overlap/SNR and effort to separate the signals.
- Residual echo affects the data reception.
- Has to keep a minimum ratio between US and DS data rates.
- Affected by near-end cross talk.

1) These slides make no statement on to what degree the differences actually matter. Whether or not they matter is a question of exact system parameters, implementation, and perspective of user. They are listed to help the following, more detailed comparison discussion.

4. Where the two proposals differ.[1] (1)

„TDD“[2]

- Alternating transmission

	2.5 Gbps	5 Gbps	10 Gbps
DS modulation	PAM 2	PAM 2	PAM 4
DS line rate	3 Gbps	6 Gbps	6 Gsps
US modulation	PAM 2		
US line rate	3 Gbps		

- RS FEC
  - DS (130, 122)
  - US (130, 124)

„ACT“[2]

- Simultaneous transmission

	2.5 Gbps	5 Gbps	10 Gbps
DS modulation	PAM 2	PAM 2	PAM 4
DS line rate	2.8125 Gbps	5.625 Gbps	5.625 Gsps
US modulation	DME		
US line rate	234 Mbps		

- RS FEC
  - DS (360, 326)
  - US (50,46)

[1] Other differences are consequences mainly derived from these items

[2] On the following, ACT/TDD without “” identifies the technical principal, with “” means the exact proposal. Sometimes, both uses would be correct. This is not distinguished.

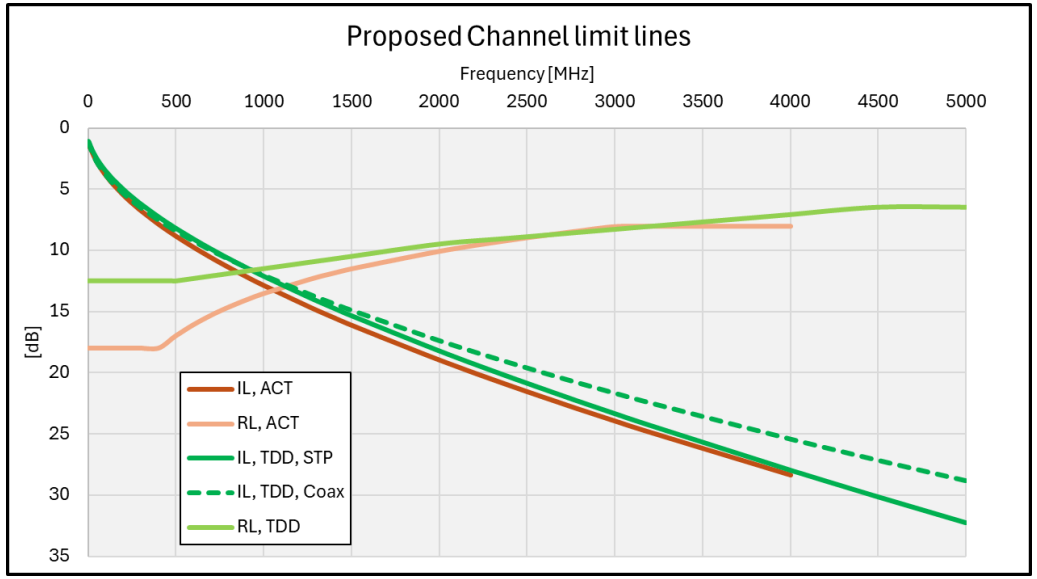
4. Where the two proposals differ.[1)] (2)

„TDD“

- Separate IL limit for Coax and STP
- f_{max} = 5 GHz
- 6dB less RL for lower frequencies than ACT

„ACT“

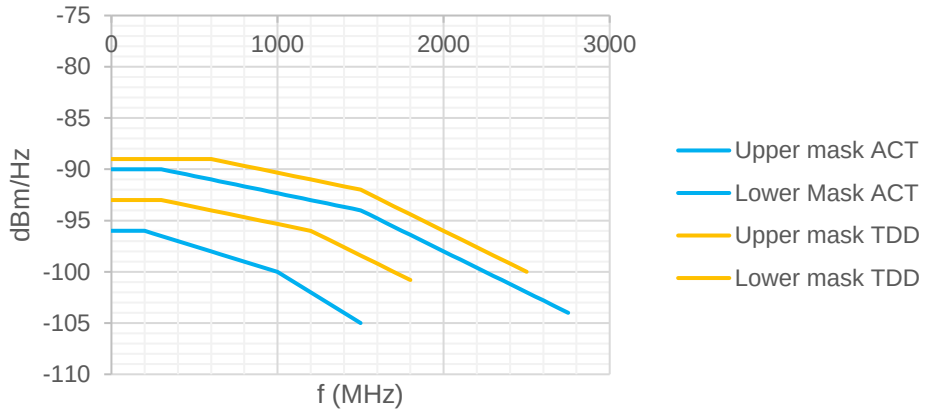
- One IL limit for Coax and STP
- f_{max} = 4 GHz
- 6dB more RL needed for lower frequencies



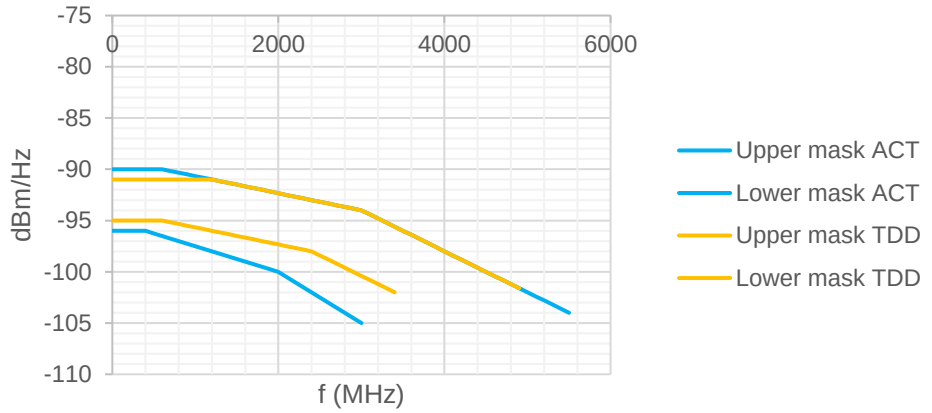
[1)] Other differences are consequences mainly derived from these items

4. Where the two proposals differ.[1] (3)

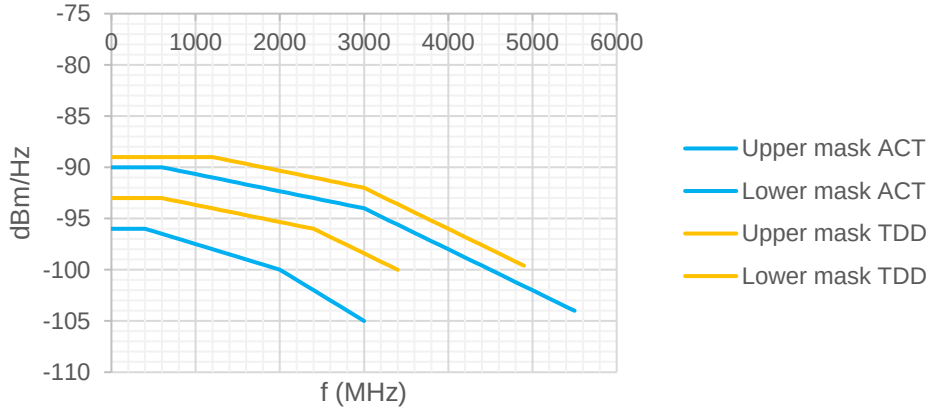
PSD masks, STP[2], Downstream, 2.5G



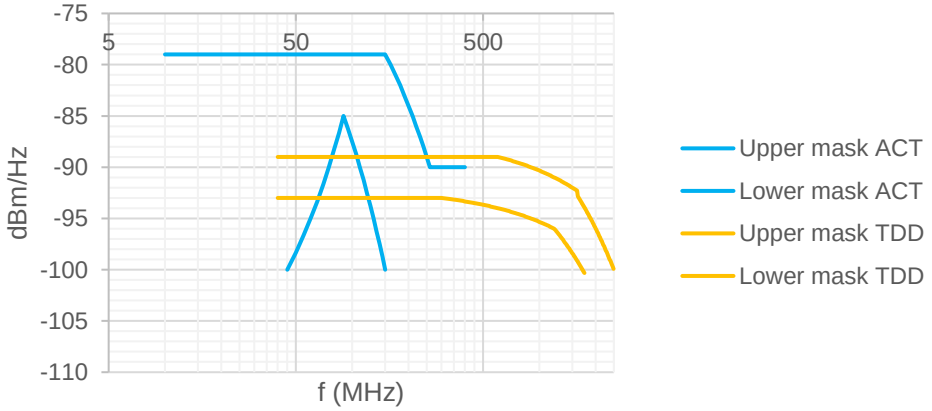
PSD masks, STP, Downstream, 10G



PSD masks, STP, Downstream, 5G



PSD masks, STP, Upstream



„TDD“ Source: Update on PSD Mask Proposal for 802.3dm
„ACT“ Source: sedarat_3dm_202505a.pdf

“ACT”: US continuous 234MBaud and simultaneous to DS
“TDD”: US bursts of 3GBaud and alternating to DS

1) Other differences are consequences mainly derived from these items
2) Limits for coaxial cabling are –3dB in all cases

4. Where the two proposals differ.[1] (4)

„TDD“

Transmit Power at MDI in dBm

DR	Coax		STP	
	Min	Max	Min	Max
10G	-3	-1	0	2
5G	-1	1	2	4
2.5G	-3	-1	0	2
100M	-3	-1	0	2

Source: https://www.ieee802.org/3/dm/public/0125/Chini_3dm_03a_0125.pdf

Power during the active period (6% duty cycle for US and 92% for DS).

„ACT“

Transmit Power at MDI in dBm

DR	Coax		STP	
	Min	Max	Min	Max
10G	-4	-1	-1	2
5G	-4	-1	-1	2
2.5G	-7	-4	-4	-1
100M	-6	-3	-3	0

Source: https://www.ieee802.org/3/dm/public/0525/sedarat_3dm_202505a.pdf

Power on the line adds DS and US power.

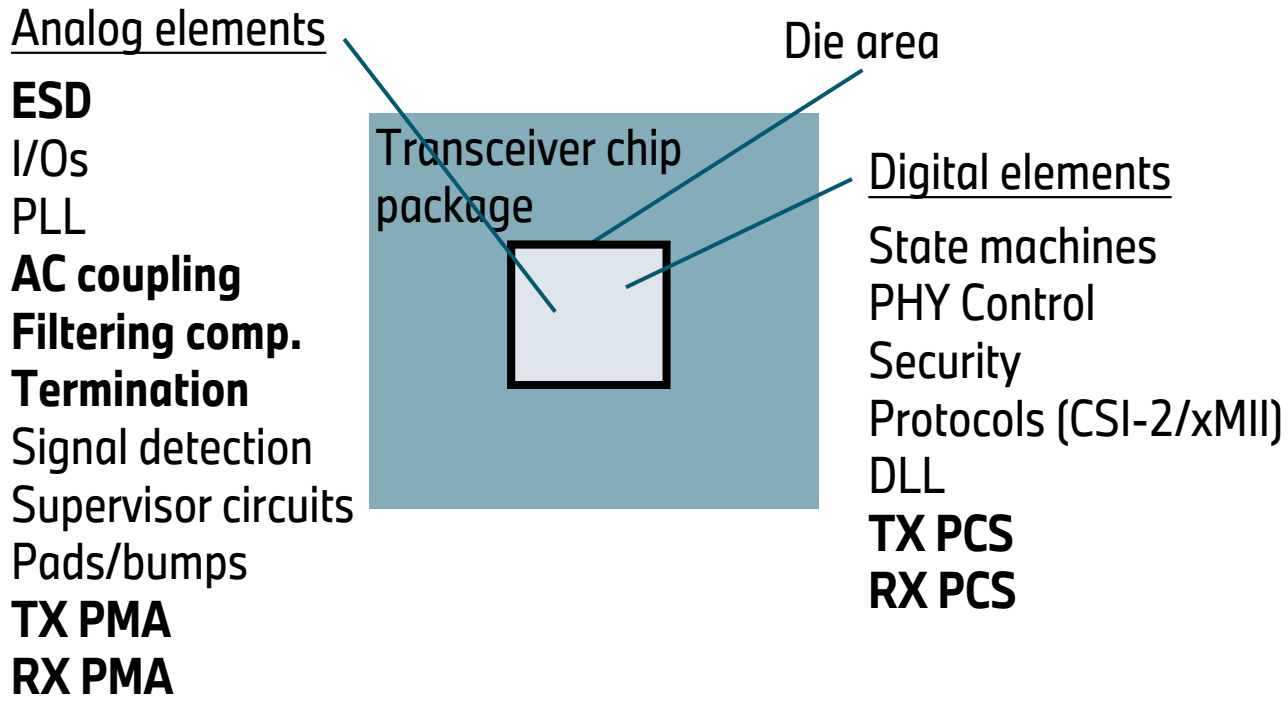
[1] Other differences are consequences mainly derived from these items

5. Criteria

1. PHY and transceiver complexity
   a) „Camera side“
   b) „ECU side“
   c) Power consumption
2. Performance
   a) EMC emissions
   b) EMC immunity
   c) Cable reach (min/max)
   d) Latency
3. Relative system costs
   a) Power over circuitry
   b) Crystal
   c) Bi-directional use of ports
   d) Power rails
4. Other
   a) Auto-negotiation
   b) Reuse from auto.-SerDes
   c) Reuse from auto.-Ethernet
   d) Path towards higher data rates
   e) Compatibility with TSN
   f) Debuggability, diagnostics

5. Criteria evaluation
1a) Complexity camera side (1)

- Every transceiver chip contains a number of different functions and elements that define the complexity of the camera side transceiver chip.
- The required die size of the transceiver chip thereby also depends on product features (e.g., security, protocols, …), implementation (process), and only to some extent, on the selected proposal for 802.3dm.
- The items that are affected are by the “ACT”/”TDD” selection are marked in **bold**.



5. Criteria evaluation
1a) Complexity camera side (2)

	„TDD“	„ACT“
AC coupling, filtering, termination, ESD, sync, start-up	?	?
RX PMA elements considered	CTLE, slicer, calibration, phase interpolator, S/P ****) (VGA, adder, DFE, slicer, slicer)	Hybrid, but no echo canceller, no equalizer *)
RX PMA estimated die size	250% more complex ***) vs 0.005mm²/ 0.0108mm² for analog equalizer ****)	<0.012mm² (RX only *))
RX PCS elements	RS (130, 124) optional, scrambler, 65B64B	RS (50,46), scrambler, 65B64B
TX PMA elements	Line driver, PAM2/4	Line driver, PAM2/4
TX PMA estimated die size	?	?
TX PCS elements	RS (130, 122) optional for 2.5, 5 Gbps, scrambler 64B65B	RS (360, 326), for all speeds, scrambler, 64B65B
PLL, I/Os, signal bumps,…	?	?
Overall die size	10 Gbps for both RX/TX PMA + PLL < 0.13mm² **)	?

*) Lo_3dm_02a_0125.pdf **) Chini_3dm_02b_0325.pdf ***) Cordero_3dm_031025.pdf ****) Chini_3dm_02_07272025.pdf

5. Criteria evaluation
1a) Complexity camera side (3)

ESD

- May be triggered by Max V on wire plus RF interference.
- With Max V (“ACT”) > Max V (“TDD”) larger risk of triggering ESD protection.

	Max V on wire [V] **)	Peak @1.1V [V]*)	Peak @1.8V [V]*)
„TDD“	Max (0.6, 0.35) =0.6	1.1/2+0.6/3 =0.85	1.8/2+0.6/2 =1.1
„ACT“	0.65+0.32 =0.97	1.1/2+0.97/2 =1.04	1.8/2+0.97/2 =1.385

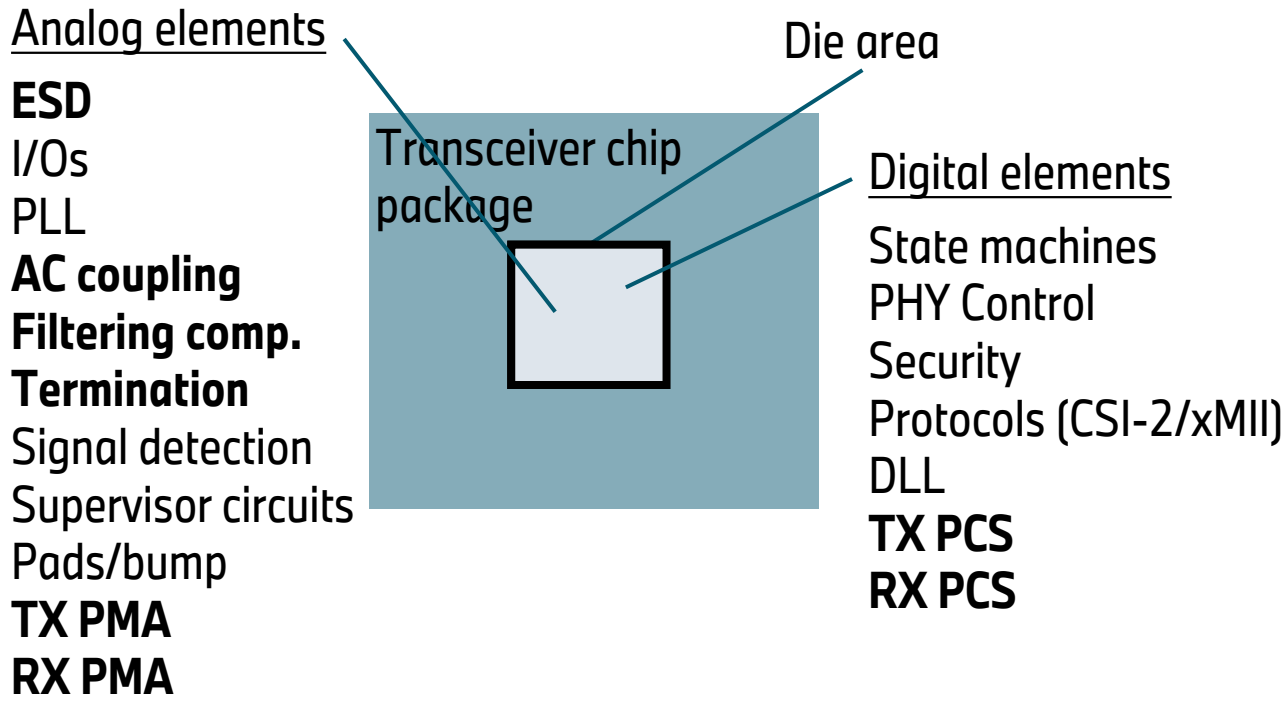
Impact in case of imager integration

- Is implementation specific but risks need to be taken into consideration (especially for smaller process nodes, which tend to use lower voltages).
- Integration with sensor typically requires use of 1.1V or 1.8V rails.
- “ACT” TX may need to use 1.8V (see table), which will increase power consumption in 50 Ω environment and may result in slower IO devices.
- “TDD” TX may use 1.1V (see table)
- Low headroom also impacts linearity.

*) Assumes voltage mode DAC as this is lowest power implementation, which needs to add half the supply.
**) see 1c) Power consumption (2)

5. Criteria evaluation
1b) Complexity ECU side (1)

- Every transceiver chip contains a number of different functions and elements that define the complexity of the camera side transceiver chip.
- The required die size of the transceiver chip thereby also depends on product features (e.g., security, protocols, …), implementation (process), and only to some extent, on the selected proposal for 802.3dm.
- The items that are affected are by the “ACT”/”TDD” selection are marked in **bold**.



5. Criteria evaluation
1b) Complexity ECU side (2)

	„TDD“	„ACT“
AC coupling, filtering, termination, ESD, sync, start-up	?	?
RX PMA elements	CTLE, VGA, adder, DFE +S/P, two slicers, slicer calibration, phase interpolator*)	Hybrid, HPF, DFE equalizer w/o echo cancellation ****)
RX PMA estimated die size	0.0108mm² for analog equalizer *)	200% more complex than GMSL***), assuming echo compensation for GMSL
RX PCS elements	RS (130, 124) optional, scrambler 64B65B	RS (50, 44), scrambler, 64B65B
TX PMA elements	Line driver, PAM2	Line driver, PAM2
TX PMA estimated die size	?	?
TX PCS elements	RS (130, 122) optional for 2.5, 5 Gbps, scrambler 64B65B	RS (360, 326), for all speeds, scrambler, 64B65B, 400% more complex than TDD*)
PLL, I/Os, signal bumps,…	?	?
Overall die size	10Gbps for both RX/TX PMA+PLL < 0.13mm² **) as for camera side	

*) Chini_3dm_02_07272025.pdf **) Chini_3dm_02b_0325.pdf ***) Cordero_3dm_031025.pdf ****) jonsson_3dm_02_06_26_25.pdf

5. Criteria evaluation
1b) Complexity ECU side (3)

ESD

- Same situation as for camera side.
- Superimposed voltages for “ACT” + RFI on the wire might trigger ESD protection circuitry more easily than for “TDD”.

Impact in case of switch integration

- Not constrained to 1.1V/1.8V.
- A reasonable minimum supply for Vmode DAC can be 1.35V and above (0.675 + 0.97/2 = 1.16V).
- Care to be taken to ensure no overstress of high-speed core devices (junction voltages must be below stress limits).

5. Criteria evaluation
1c) Power consumption (1)

- Every transceiver chip contains a number of different functions and elements that define the complexity of the transceiver chips (see also 1a) and 1b)).
- Furthermore, the power consumption of the transceiver chips does not only depend on the complexity of the implementation, but also on the duty cycle of the communication.
- Low power consumption is in general important, but especially on the camera side, where heat dissipation affects the imager quality. A target for the overall PHY function to be integrateable into an imager IC was given as 200 mW***).

***) 091423/2023-09-06_Automotive%20camera%20PHY%20requirements%20study_V2.1.pdf

5. Criteria evaluation
1c) Power consumption (2)

	„TDD“	„ACT“
	US 6% duty cycle, DS 92% duty cycle	US and DS have 100% duty cycle
LS receiver PMA	< 3mW **)	< 3mW *)
LS receiver PCS	?	?
HS transmitter	50Ω environment & .6V p2p	50Ω environment & .65V p2p ***)
Overall sensor side	Target is < 200mW	Target is < 200mW
HS receiver PMA	< 10mW **)	?
HS receiver PCS	?	?
LS transmitter	50Ω environment & .35V p2p 6%@3Gbps	50Ω environment & .32V p2p ***) 100%@234Mbps
Overall ECU side	?	?

*) Lo_3dm_02a_0125.pdf

**) Chini_3dm_02b_0325.pdf

***) derived from sedarat_3dm_202505a.pdf

5. Criteria evaluation
2a) EMC immunity (1)

„TDD“

Has no signal overlap in the time domain. Frequency is spread over a wide band.

“TDD” does not need an echo canceller to achieve SNR performance with a good margin to avoid bit errors when hit by a strong RF ingress noise.

Immunity test results exist for TDD-based ASA-ML have been presented:

Zerna_3dm_01a_150512_EMC_Coax.pdf

Zerna_3dm_01a_250729.pdf

„ACT“

Has full spectral signal overlap of US and DS signals.

In an implementation without echo canceller, the residue of the echo reduces the SNR with a small margin to 17dB @ BER=10^-12.

Filtering of in-band signal is not possible.

To improve the SNR and with that the EMC immunity, “ACT” could implement a “costly” echo canceller/echo compensation.

ACT intends to use 2dB lower power at 5G and 3dB lower power at 2.5 G than recent incumbent solutions (1Vpp), reducing its immunity compared with the incumbents.

5. Criteria evaluation
2b) EMC emissions (1)

„TDD“

Energy of only either US or DS signal simultaneously on the channel.

“TDD” is less prone to emissions in the car, in particular when Coax cables have aged and shielding is weakened.

Emissions test results exist for TDD-based ASA-ML have been presented:

Dalmia_Ng_EMI_STP_3dm_01_04172025.pdf

Dalmia_Ng_EMI_COAX_3dm_01_04172025.pdf

„ACT“

Energy of both US and DS signal simultaneously on the channel.

“ACT” sends a narrowband signal in the FM band, which increases the chance for emissions.

“ACT” relies on shielding effectiveness of cables that are subject to aging*). Especially for coaxial cabling, the coupling attenuation is reduced with aging.

*) 1000BASE-T1 went to STP exactly for the need to reduce emissions, even though on the bench it passes class 5 of CISPR 25 with a good margin

5. Criteria evaluation
2c) Min/Max cable reach (1)

General comments:

- IEEE 802.3 PHYs specify electrical parameters for a channel.
- 802.3 PHYs do not specify specific cables.
- Nominal cable length and characteristics are used as a basis to define electrical parameters.
- Once the electrical parameters are defined, any cable that meets the parameters can be used regardless of actual length.
  - Example: If cable parameters are derived from high-volume 15m cables, but a higher quality 20m cable can meet the electrical parameters and satisfy the maximum link segment delay specification, it is automatically allowed by the standard.
  - A short cable is automatically allowed, if it meets all electrical parameters. Typically, there is no minimum reach specified by 802.3.
- The major electrical parameters defined include
  - Insertion loss (IL)
  - Return loss (RL)
  - Screening attenuation (SA)
  - Propagation delay

5. Criteria evaluation
2c) Min/Max cable reach (2)

The 802.3dm project has an objective for (up to at least) 15 m cable reach, which was backed by market data, and which already includes a 30% safety margin.*)
No requirement was defined for a minimum cable reach. For automated cable assemblies, link segments under 25 cm are typically difficult to manufacture and thus represent a lower limit.

„TDD“

IL proposal supports 15 m reach on commonly used coaxial cables and 10 m on commonly used STP cables.

Assuming there is a cable that meets the IL/RL/SA requirements for longer cables, the maximum length is defined by the inter burst gap and the cable velocity ratio.

Is less prone to RL and can therefore support also very short link lengths. 10 cm links have been supported in practical implementations.

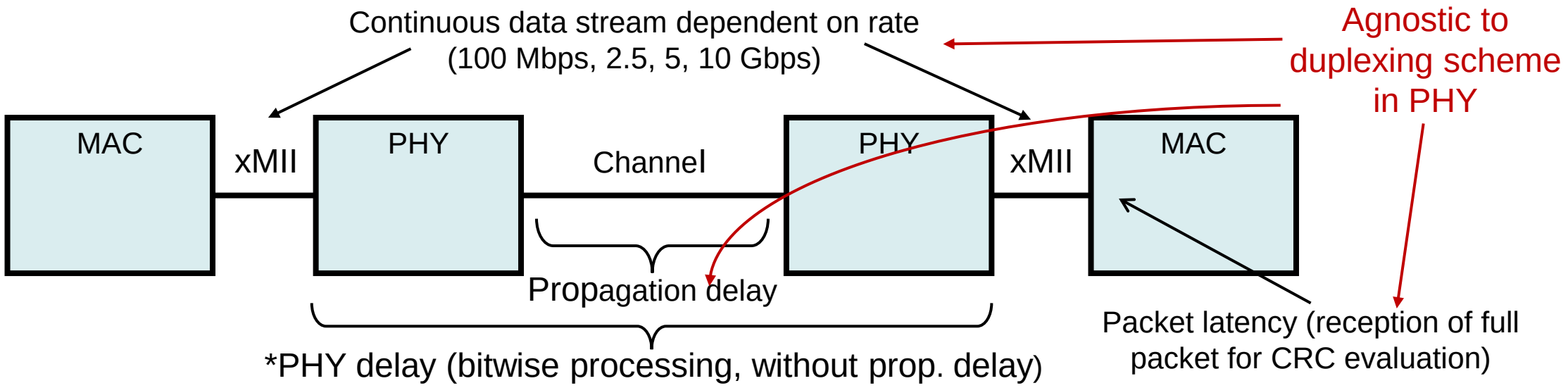
„ACT“

If an echo canceller is used, its complexity increases with the cable reach, so the maximum reach is complexity limited.

If no echo canceller is used on either side of the communication, there are no reach constraints provided there is a cable that meets the IL/RL/SA requirements.

*) matheus_ISAAC_03_1411202327_v1.0b.pdf

5. Criteria evaluation
2d) Latency/Delay (1)



PHY delay*	"TDD"	"ACT"
Upstream delay (including FEC)	9.6µs for all speed grades[1]	~8µs[2]
Downstream delay (including FEC)	~1.1us[3]	2.048µs[2]

1 Chini_3dm_01a_0125.pdf
2 Houck_Cordero_ComparativeAnalysis
3 Dalmia_Goel_3dm_01a_11112024.pdf

5. Criteria evaluation
3a) Power over circuitry (1)

„TDD“

- Can meet the MDI return loss limit adopted in dm.
- One single inductor can meet the high inductance requirement (smaller size).

„ACT“

- Can meet the MDI return loss limit adopted in dm.
- One single inductor is expected to meet the high inductance requirement**).
- Improvement over incumbents with NRZ, which use two to four inductors*).

Example inductors****):

	Footprint [mm²]	Inductance [uH] ***)	Part Number	Max DCR @ 25C [mΩ]	SRF [MHz]	I(mA), 20% drop, 20% temp rise
„TDD“	1.8 x 1.0	1	PFL1609-102	230	445	690
„ACT“	3.3 x 2.67	6.8	1210POCB-682**)	210	120	690 (105C)

*) user-guides/public-gmsl2-hardware-design-and-validation-guide.pdf
**) Houck_3dm_02_0121_5.pdf
***) For inductors without shield: The larger the inductor the more cross talk and the more high frequency emissions.
****) Chini_3dm_01_07272025.pdf

5. Criteria evaluation
3b) Crystalless (1)

*) Ng_3dm_01_05122025.pdf
**) Houck_Fuller_3dm_03_1111.pdf

Without crystal, the sensor side transceiver IC:

- Must recover the clock from the “Low speed” US RX data.
- Must have a reference clock and clock and data recovery (CDR) on the chip.

„TDD“

- Non-continuous data stream*)
  - Clock and phase recovery tracked with 3 Gbps burst data (incl. high-frequency jitter)
  - ~104kHz “TDD” cycle beat can additionally assist in centering reference oscillator.
- Higher IL reduces eye opening
  - Usual eye-opening equalization techniques needed
- Needs equalization for larger eye to suppress RFI (available anyway)

„ACT“

- Continuous, transition rich data**)
  - But at very low data rate
  - Unbalanced eye affects sampling point
- Poor RL reduces eye opening
  - Sensitive to reflections @ MDI
- Hybrid may negatively impact eye opening
- Needs equalization for larger eye to suppress RFI (not necessarily planned)

5. Criteria evaluation
3b) Crystalless (2)

- In the crystalless environment the transmitter must still conform to low random jitter transmit data outputs.
- Other SerDes TX jitter requirements, that affect the CDR implementation are:

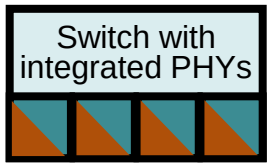
Standard	TX jitter	Notes
802.3ch 10Gbps	1ps rms	Clause 149.5.2.3.1 (175.78125 MHz test clock)
A-PHY Gear4 10.8Gbps	1.41ps rms	IEEE 2977, Sections 9.1.5.1, 9.1.2.3 (2 GHz test clock)

- Similar requirements are expected for 802.3dm.

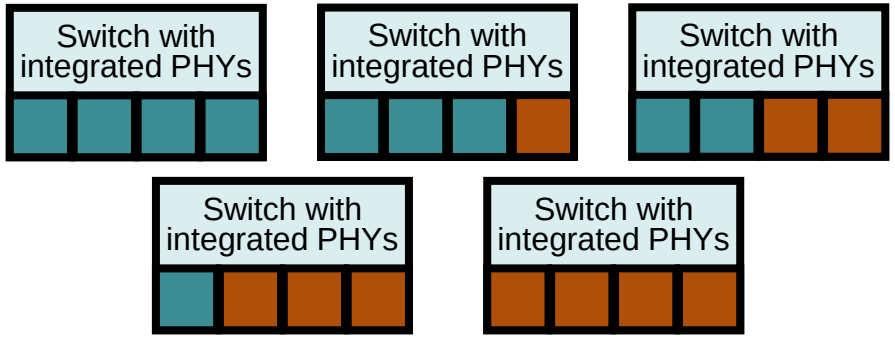
5. Criteria evaluation
3c) Bi-directional use of ports (1)

- The possibility to change the high-speed direction in an asymmetric PHY, reduces the number of IC products that need to be provided and qualified.
- The easier the change of high-speed direction can be achieved, i.e., the smaller the added complexity, the more likely that products will support this.
- This is of interest especially on ECU side.
- On the ECU side, the ease to turn around the high-speed direction significantly reduces variants especially in case of switch integration, for customers and suppliers.

Example, switch with 4 integrated PHYs:



One efficient product when change of high-speed direction is easy to realize



Five products when the change of high-speed direction is costly to realize

HS RX, LS TX

HS TX, LS RX

5. Criteria evaluation
3c) Bi-directional use of ports (2)

„TDD“

- In general, Tx needs additional support to 6GHz baud rate PAM2 and 6GHz baud rate PAM4; Rx needs no change.
- For PMA:
  - Only additional Tx mode for 6GHz baud rate PAM4.
  - A negligible additional complexity for the change of “TDD” duty.
- For PCS, it depends on the difference between HS and LS, RS-FEC may be dominated:
  - RS-FEC: HS (130, 122) and LS (130, 124)
  - PCS scrambler: no difference between HS and LS
  - Side-stream scrambler: no difference between HS and LS
  - Interleaving/de-interleaving: additional support for L = 2&4, complexity is related to RS-FEC.
  - PCS TRx bit ordering: minor

- Developing a PHY that allows to change the high-speed direction would need to support three different speeds (2.5G, 5G, 10G).

„ACT“

- In general, Tx and Rx need additional support to all three high speeds and low speed, respectively.

- For PMA:
  - Basically, it need to combine two different TRx, resulting in a large increase in complexity.
- For PCS, it depends on the difference between HS and LS, RS-FEC may be dominated :
  - RS-FEC: HS (360, 326) and LS (50, 46)
  - PCS scrambler: negligible additional complexity for 10 Gbps
  - Side-stream scrambler: no difference between HS and LS
  - Interleaving/de-interleaving: additional support for L = 2&4, complexity is related to RS-FEC.
  - PCS TRx bit ordering: minor

- Developing a PHY that allows to change the high-speed direction would need to support four different TX/RX designs (2.5/5G&100M, 100&2.5/5G, 10G&100M, 100M&10G)

5. Criteria evaluation
3d) Power rails (1)

Motivation:

- With limited PCB space in a camera, saving power rails (regulators) results in a relative cost advantage.
- A small number of rails and/or being able to share power rails with the imager sensor (typical values are 1V, 1.2V, 1.8V for I/Os) are seen as advantageous.

In general, the required power rails are product and implementation specific.

The question is, whether there is a principal difference in the amount of signal processing that might affect the power rails (e.g. a core voltage of ~0.8V is often used for high compute DSP tasks (equalizer, etc.) as needed for IEEE 802.3ch).

- The amount of signal processing needed depends especially on the absolute amount of data to be processed. In case of “ACT” and “TDD”, very similar amount of data is processed. This means, that based on the signal processing, there is no practical difference between the power rails usable for “ACT” and “TDD”.

5. Criteria evaluation
4a) Autoneg (1)

„TDD“

The startup of the “TDD” inherently includes auto-negotiation for link speed.

The objective of 100ms start-up time is met.

“TDD” has inherent timing information in the PHY layer that allows producing delay compensated GPIO for shutter synchronization.

„ACT“

Auto-negotiation not an inherent part. Would need to be specified and implemented separately.

The objective of 100ms start-up time is met.

There is no PHY layer reference for GPIO delay compensation for shutter synchronization. Higher layer packet synchronization is required.

5. Criteria evaluation
4b) Reuse from Auto-SerDes (1)

There are three perspectives for reuse:

1. Reuse of building blocks when developing and dm IC
   - In the technology as such (signal processing, …)
   - For the product (power supply, filter, …)
2. Allowing for dual mode PHYs with limited complexity
3. Reuse of eco system (cables, connectors, test spec, EMC …)

The following will focus on technical commonalities and differences in the specification and whether this allows for reuse in the eco system.
Aspects that depend on the implementation (like power supply) are not covered.

5. Criteria evaluation
4b) Reuse from Auto-SerDes (2)

	„TDD“	ASA-ML	GMSL 2/3*)	“ACT”
Duplexing	TDD	TDD	Full frequency overlap	Full frequency overlap
Scrambler length	33	23	58	33
DS line coding	64B/65B	n/a (64B/65B)	9B/10B	64B/65B
DS RS FEC	(130, 122)	(216, 214)/ (240/214)	(128, 120)	(360, 326)
DS line rate	3/6/6 GBaud	4/8/6 GBaud	3/6/6 GBaud	2.8/5.6/5.6 GBaud
DS mod	PAM 2/2/4	PAM 2/2/4	PAM 2/2/4	PAM 2/2/4
US line coding	64B/65B	n/a (64B/65B)	9B/10B	64B/65B
US RS FEC	(130, 124)	(108, 106)	None	(50,46)
US mod	PAM 2	PAM 2	PAM 2	DME
US line rate	3 Gbps	4 Gbps	187.5 Mbps	234 Mbps

*) Slide 7 in Cordero_baseline.pdf

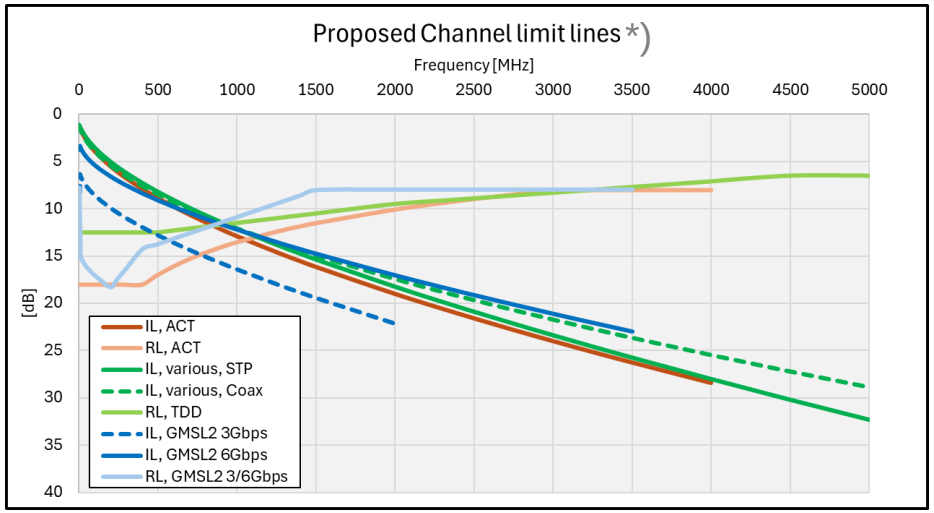
5. Criteria evaluation
4b) Reuse from Auto-SerDes (3)

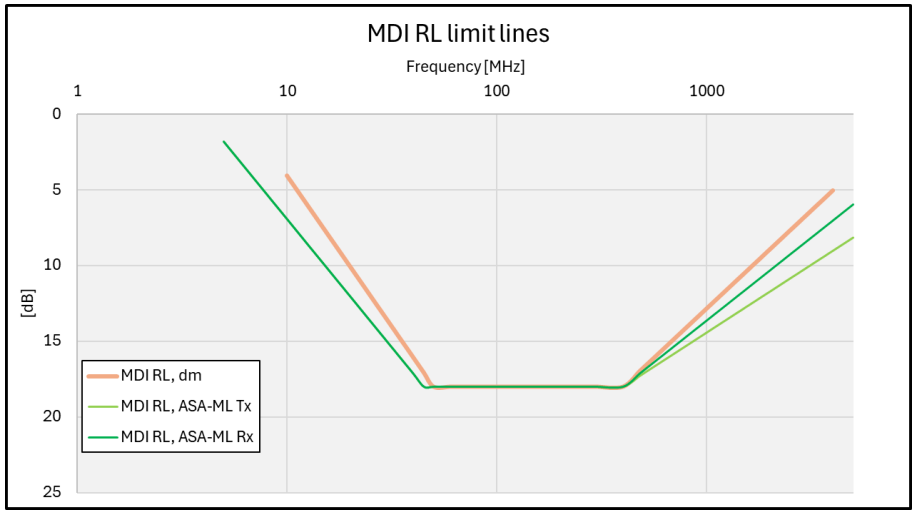
„TDD“

- Uses the same IL, RL and similar MDI RL as ASA-ML and can reuse the respective channel and components specification.
- Qualified cables and connectors available.
- Reuse possible also for EMC test and PoC circuitry. ASA-ML EMC results relevant.

„ACT“

- Proposed channel limit lines for “ACT” are different from those of GMSL 2/3.
- As the spectral signal overlap is different for “ACT” and GMSL2/3 reuse of EMC results can only give an indication.
- Power over circuitry for “ACT” is improved over that of GMSL 2/3.





*) gmsl2-channel-specification-user-guide.pdf, including MDI

5. Criteria evaluation
4c) Reuse from Auto-Ethernet (1)

„TDD“

The “TDD” proposal reuses the following items for **both** directions from IEEE 802.3ch:

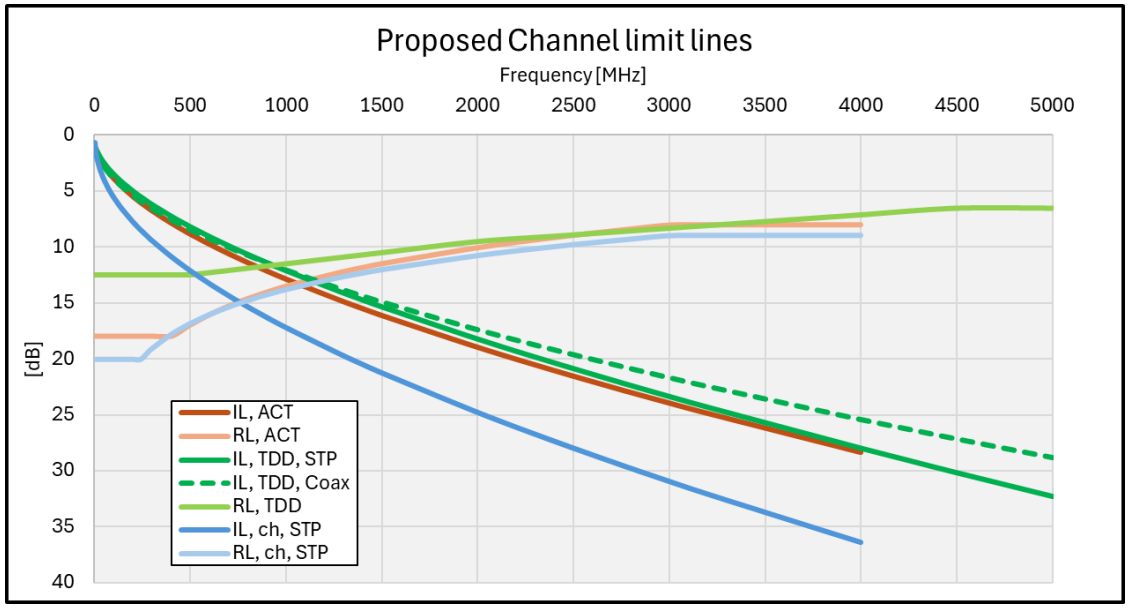
1. PCS Transmit and Receive state diagram, 64/65B block structure, control codes, ordered sets definitions.
2. PCS Transmit and Receive bit ordering, with slight modifications.
3. Training infofield format with slight modifications
4. 33-bit side-stream scrambler, PAM2 mapping and PAM4 gray mapping/precoder, interleaver structures.
5. PHY control state diagram TRAINING/ COUNTDOWN concept, with slight modifications.
6. RFER monitor, link monitor.

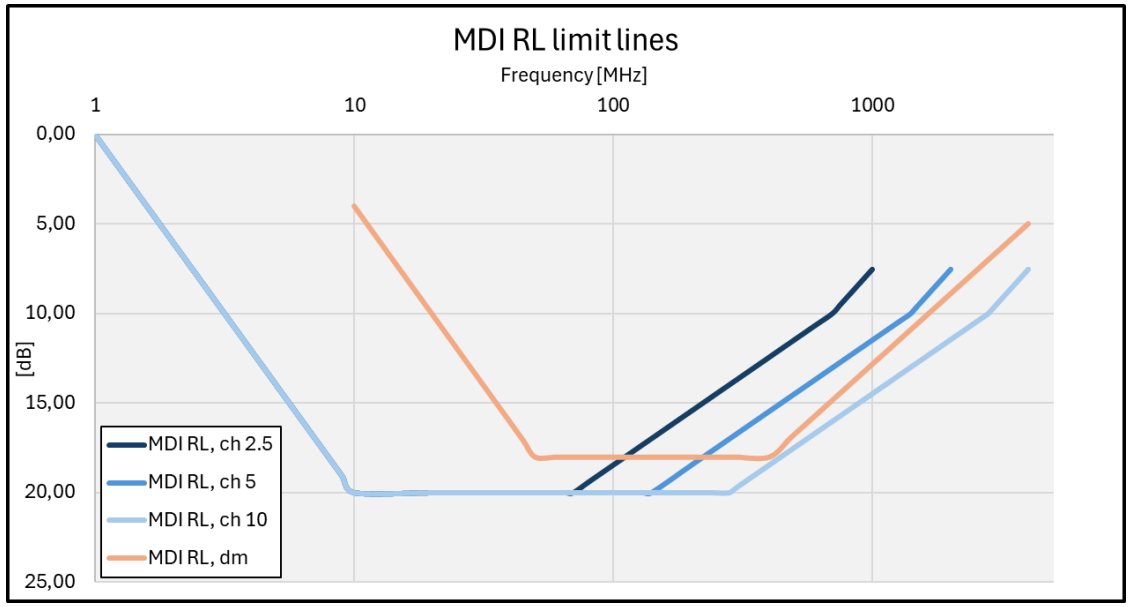
„ACT“

- The 10Gbps DS “ACT” reuses the main functions of the 802.3ch transmit path.
- The 2.5 and 5 Gbps DS reuse the main functions of the 802.3ch PCS transmit path except for PAM level and line rate.
- There is no technical overlap in the US or the duplexing.

5. Criteria evaluation
4c) Reuse from Auto-Ethernet (2)

- Neither of the proposals reuses the IL, RL, nor MDI RL limit lines from ch.
- The 802.3ch channel is only defined for STP cables.





5. Criteria evaluation
4c) Reuse from Auto-Ethernet (3)

- There might be interest to have dual mode symmetric 802.3ch and asymmetric 802.3dm PHYs for switch integration.
- Because of the echo canceller ch requires, 802.3ch will have a fully digital implementation.
- To be cost efficient, dm allows for mixed signal/analog implementations, smaller power over delivery circuit, different power rails, ...
- A dual mode ch/dm PHY would significantly increase the relative costs for the asymmetric communication in both cases.
- The difference is in the add on if the base is 802.3ch symmetric communication.

„TDD“

ECU or camera side

„ACT“

ECU/“deserializer“ side

Camera/“serializer“ side

- In both cases, to add ch-mode to a dm PHY would be a large add-on
- For a ch-PHY to add an “ACT”-mode would be less effort than to an a “TDD”-mode

5. Criteria evaluation
4d) Path towards higher rates (1)

- When a PHY development is done, it is typically followed by the question for the next generation.
- For 802.3dm, the following two properties have already been identified in the discussion. While they did not make it into the objectives or PAR of dm the potential ease of extendibility is nevertheless of interest.

1. Higher DS data rates (esp. 15 Gbps, 25 Gbps), e.g. zimmerman_3ISAAC_01b_012224.pdf
2. Higher US data rates (esp. 1 Gbps), e.g., matheus_ISAAC_01c_10042023.pdf

	“TDD”	“ACT”
15/25 Gbps DS	Line rate will be somewhat higher than for “ACT”. However, the constraints will be very similar to those of “ACT”.	Line rate will be somewhat lower than for “TDD”. Constraints will be similar as when moving from 802.3ch to cy.
1 Gbps US	For 2.5G/1G, 5G/1G, and 10G/1G the fundamental architecture stays the same. The US/DS duration changes and the line rate should be adapted. It is a minor change.	For 2.5G/1G, 5G/1G, and 10G/1G the fundamental architecture would need to change, which means major changes to the PHY definition.

5. Criteria evaluation
4e) Compatibility with TSN (1)

- The MAC sees continuous data streams between MAC and physical layer without knowledge of or being impacted by the duplexing scheme of the PHY.
- It thereby makes no difference whether a physical xMII is implemented between RS and PHY or not. The IEEE 802.3 spec mandates the same functional behavior even when there is no xMII implemented.
- TSN functions without interrelations to the PHY therefore cannot be affected by the duplexing scheme of the PHY. If they are affected by the asymmetry, this applies equally to both proposals.
- One important TSN function that does have interrelation with the PHY is 802.1AS/gPTP.
- The question is especially, whether the accuracy of the pdelay measurements in a TDD system is affected by the quiet gaps.
- Hutchison_Arunarthi_3dm_01_07272025.pdf shows that this is not the case as
  - Also in a TDD system there is a constant delay between the TX and RX RS layers,
  - TDD-based 802.3dm would be fully compatible with upper layers in 802,
  - 802.3 Clause 90 has addressed this topic well in the past.

5. Criteria evaluation
4f) Debuggability/diagnostics(1)

Being able to monitor and diagnose a technology is important for its deployment.

In principle, it is expected that both technologies can be monitored and debugged and that there are no fundamental differences in the possibilities to obtain e.g., a signal quality indicator (SQI) in test mode or during run-time.

Some expected differences are:

„TDD“

- PHY debugging on “TDD” is easy with a splitter and an oscilloscope.
- The US “TDD” transmitter runs at a higher frequency and therefore allows a better resolution when locating a short or open with TDR.

„ACT“

- An “ACT” signal cannot be properly displayed on an oscilloscope as US/DS are mixed.
- In “ACT”, the US transmitter is a low-frequency transmitter. Hence the TDR resolution/accuracy to detect the location of a short or open would be lower/worse than for a “TDD” transmitter.

6. Summary

- These slides provide an overview on the main difference between the two proposal for IEEE 802.3dm “TDD” and “ACT”.
- These slides provide criteria for evaluating the „TDD“ and „ACT“ proposals.
  - These criteria contain items that are directly relevant to fulfill PAR and objectives.
  - These criteria contain additional items relevant from a (relative) total cost of ownership and usability perspective.
- These slides provide data and links on the fulfillment of specific criteria.

- These slides present a first version. Later versions might refine the presented data, based on information and discussions available in 802.3dm.

Thank You!