P802.3dm proposed Clause 45

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July 2025

Purpose

- Clause 45 updates are required for all new PHYs
- None of the required information is dependent on the duplexing method
- I have not included the text that describes the bits in this presentation, but it is available in the companion pdf that shows the entire Clause 45 proposal

45.2.1 PMA/PMD registers

Change the reserved row for 1.77 through 1.79 in Table 45-3 (as modified by IEEE Std 802.3cz-2023, IEEE Std 802.3df-2024, and IEEE Std 802.3dj-20xx) as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.77	Asymmetrical BASE-T1/V1 PMA/PMD extended ability	45.2.1.60f
1.~~77~~78 through 1.79	Reserved	
…		

45.2.1.7.4 Transmit fault (1.8.11)

***Insert new rows in Table 45-9 immediately after row for 2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1 as follows** (unchanged rows not shown):*

Table 45–9—Transmit fault description location

PMA/PMD	Description location
…	
2.5G+100MBASE-T1, 5G+100MBASE-T1, 10G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-V1, 10G+100MBASE-V1	149.4.2.2
100M+2.5GMBASE-T1, 100M+5GBASE-T1, 100M+10GBASE-T1, 100M+2.5GBASE-V1, 100M+5GMBASE-V1, 100M+10GBASE-V1	200.7.2.2
…	

45.2.1.7.5 Receive fault (1.8.10)

***Insert new rows in Table 45-10 immediately after row for 2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1 as follows** (unchanged rows not shown):*

Table 45–10—Receive fault description location

PMA/PMD	Description location
…	
2.5G+100MBASE-T1, 5G+100MBASE-T1, 10G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-V1, 10G+100MBASE-V1	149.4.2.3
100M+2.5GMBASE-T1, 100M+5GBASE-T1, 100M+10GBASE-T1, 100M+2.5GBASE-V1, 100M+5GMBASE-V1, 100M+10GBASE-V1	200.7.2.3
…	

45.2.1.60f Asymmetric BASE-T1/V1 PMA/PMD extended ability register (Register 1.77)

The assignment of bits in the Asymmetrical BASE-T1/V1 PMA/PMD extended ability register is shown in Table 45–58f.

Table 45–58f—Asymmetric BASE-T1/V1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.77.15:12	Reserved	Value always 0	RO
1.77.11	10G+100MBASE-V1 ability	1 = PMA/PMD is able to perform 10G+100MBASE-V1 0 = PMA/PMD is not able to perform 10G+100MBASE-V1	RO
1.77.10	100M+10GBASE-V1 ability	1 = PMA/PMD is able to perform 100M+10GBASE-V1 0 = PMA/PMD is not able to perform 100M+10GBASE-V1	RO
1.77.9	10G+100MBASE-T1 ability	1 = PMA/PMD is able to perform 10G+100MBASE-T1 0 = PMA/PMD is not able to perform 10G+100MBASE-T1/V1	RO
1.77.8	100M+10GBASE-T1 ability	1 = PMA/PMD is able to perform 100M+10GBASE-T1 0 = PMA/PMD is not able to perform 100M+10GBASE-T1	RO

45.2.1.60f Asymmetric BASE-T1/V1 PMA/PMD extended ability register (Register 1.77) (cont'd)

1.77.7	5G+100MBASE-V1 ability	1 = PMA/PMD is able to perform 5G+100MBASE-V1 0 = PMA/PMD is not able to perform 5G+100MBASE-V1	RO
1.77.6	100M+5GBASE-V1 ability	1 = PMA/PMD is able to perform 100M+5GBASE-V1 0 = PMA/PMD is not able to perform 100M+5GBASE-V1	RO
1.77.5	5G+100MBASE-T1 ability	1 = PMA/PMD is able to perform 5G+100MBASE-T1 0 = PMA/PMD is not able to perform 5G+100MBASE-T1	RO
1.77.4	100M+5GBASE-T1 ability	1 = PMA/PMD is able to perform 100M+5GBASE-T1 0 = PMA/PMD is not able to perform 100M+5GBASE-T1	RO

45.2.1.60f Asymmetric BASE-T1/V1 PMA/PMD extended ability register (Register 1.77) (cont'd)

Table 45–58f—Asymmetric BASE-T1/V1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.77.3	2.5G+100MBASE-V1 ability	1 = PMA/PMD is able to perform 2.5G+100MBASE-V1 0 = PMA/PMD is not able to perform 2.5G+100MBASE-V1	RO
1.77.2	100M+2.5GBASE-V1 ability	1 = PMA/PMD is able to perform 100M+2.5GBASE-V1 0 = PMA/PMD is not able to perform 100M+2.5GBASE-V1	RO
1.77.1	2.5G+100MBASE-T1 ability	1 = PMA/PMD is able to perform 2.5G+100MBASE-T1 0 = PMA/PMD is not able to perform 2.5G+100MBASE-T1	RO
1.77.0	100M+2.5GBASE-T1 ability	1 = PMA/PMD is able to perform 100M+2.5GBASE-T1 0 = PMA/PMD is not able to perform 100M+2.5GBASE-T1	RO

[a]R/W = Read/Write, RO = Read only

45.2.1.214 BASE-T1 PMA/PMD control register (Register 1.2100)

Replace the rows for bits 1.2100.13:4 and 1.2100.3:0 in Table 45–178 (as modified by IEEE Std 802.3cy-2023 and IEEE Std 802.3da-202x) as follows (unchanged rows not shown):

Table 45–178—BASE-T1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.2100.13:5	Reserved	Value always 0	RO
1.2100.4:0	Type Selection	4 3 2 1 0 1 1 1 x x= Reserved 1 1 0 1 1 = 10G+100MBASE-V1 1 1 0 1 0 = 100M+10GBASE-V1 1 1 0 0 1 = 10G+100MBASE-T1 1 1 0 0 0 = 100M+10GBASE-T1 1 0 1 1 1 = 5G+100MBASE-V1 1 0 1 1 0 = 100M+5GBASE-V1 1 0 1 0 1 = 5G+100MBASE-T1 1 0 1 0 0 = 100M+5GBASE-T1 1 0 0 1 1 = 2.5G+100MBASE-V1 1 0 0 1 0 = 100M+2.5GBASE-V1 1 0 0 0 1 = 2.5G+100MBASE-T1 1 0 0 0 0 = 100M+2.5GBASE-T1 0 1 1 x x = Reserved 0 1 0 1 x = Reserved 0 1 0 0 1 = Reserved 0 1 0 0 0 = 10BASE-T1M 0 0 1 1 1 = 25GBASE-T1 0 0 1 1 0 = 10GBASE-T1 0 0 1 0 1 = 5GBASE-T1 0 0 1 0 0 = 2.5GBASE-T1 0 0 0 1 1 = 10BASE-T1S 0 0 0 1 0 = 10BASE-T1L 0 0 0 0 1 = 1000BASE-T1 0 0 0 0 0 = 100BASE-T1	R/W

[a]R/W = Read/Write, RO = Read only

Questions?

Thanks!