Power over Coaxial Cable Optimization and Signaling Trade-off

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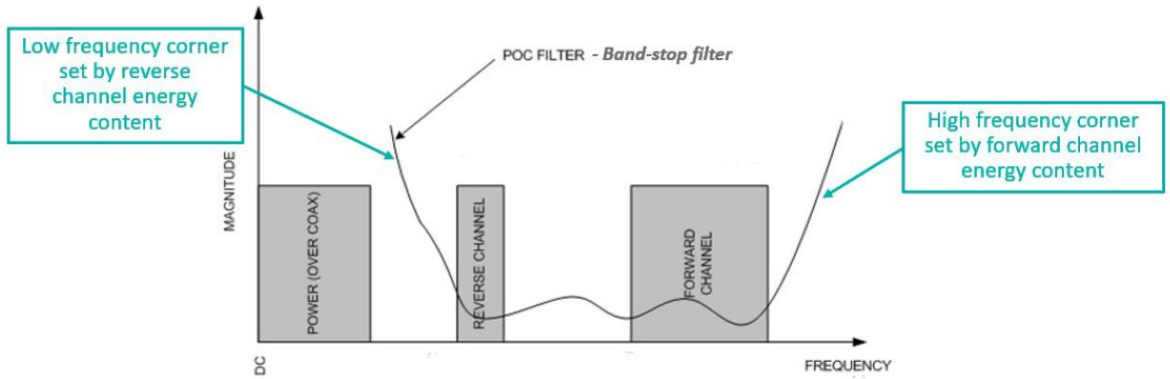
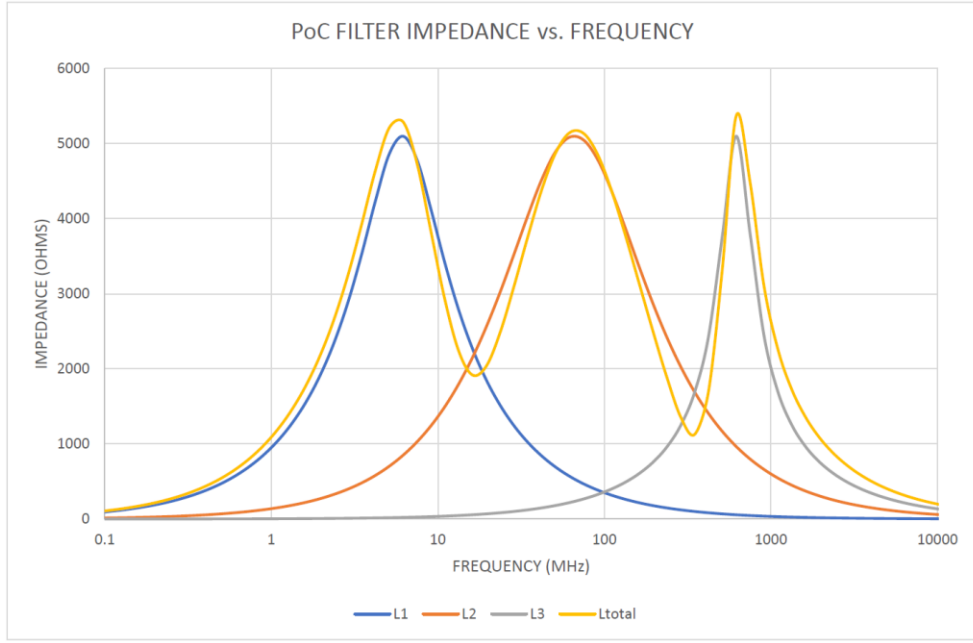
Foreword

- Power over coaxial (PoC) cable is widely used in automotive image sensor applications.
- Early automotive SerDes solutions used larger and multiple inductors in the PoC filter. A good example is GMSL1 that supported 1Mbps in reverse link and required PoC inductors larger than 100µH.
- Newer generation, GMSL2 optimized PoC inductor size to 22µH range using higher reverse link speed of 187.5MHz and 9b10b encoding. A series of power inductors are proposed in order to cover both higher speed forward channel and lower speed reverse channel.
- For 802.3dm, the particular specification that affects power inductor size is MDI Return Loss (RL). There is already a proposal for MDI-RL to 802.3dm that allows small and power efficient PoC filter design.
- This presentation discusses the significant benefits of the optimized PoC filter as compared to some existing solutions. There is, however, a trade-of in signaling and baud rate which should be observed.

PoC filter design principle and examples for GMSL2-ADI [1]

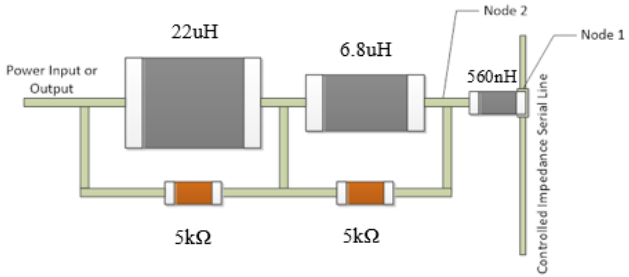




Three main users of bandwidth

- Power over Coax
- Reverse channel
- Forward channel

Cascading multiple inductors to cover the whole bandwidth



1. https://www.analog.com/media/en/technical-documentation/user-guides/gmsl2-hardware-design-guide.pdf

PoC filer examples[1] and total DCR for GMSL2

- Examples of optimized PoC solutions for GMSL2 are shown in “gmsl2-hardware-design-guide.pdf”[1]

1	C-2L-300 Coilcraft	2	L1: PFL1005-561 L2: 1210POC-223 || 5.1kΩ	560nH – 620MHz 22uH – 66MHz	440mA – 20% 520mA – 105C	***300 mA @ 105C***	Verified on EV kits

PFL1005-561 : 540mΩ @25°C

1210POC-223 : 880mΩ @25°C

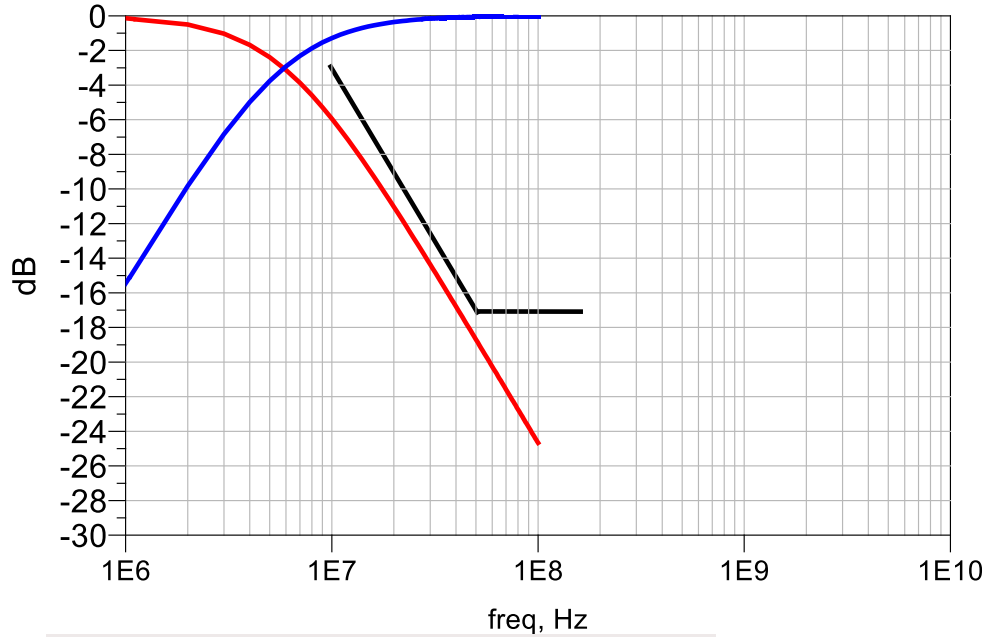
4	C-4L-1000 Coilcraft	2	L1: PFL1609-471 L2: PFL1609-471 L3: 1210POC-682 || 5.1kΩ L4: MSS6132T-223 ||5.1kΩ	470nH – 650MHz 470nH – 650MHz 6.8uH – 114MHz 22uH – 21MHz	990mA – 20% 990mA – 20% 1000mA – 105C 1120mA – 20%	***1000mA @ 85C*** ***800mA @ 105C*** ***600mA @ 125C***	Verified on EV kits

PFL1609-471 : 100mΩ @25°C
PFL1609-471 : 100mΩ @25°C
1210POC-682 : 240mΩ @25°C
MSS6132T-223 : 160mΩ @25°C

- DCR at 105C is increased by 31% from which maximum power loss on the PoC filter components may be calculated.

1. https://www.analog.com/media/en/technical-documentation/user-guides/gmsl2-hardware-design-guide.pdf

PoC filter based on a MDI-RL proposed[1] to 802.3dm



The proposed MDI Return Loss Limit is

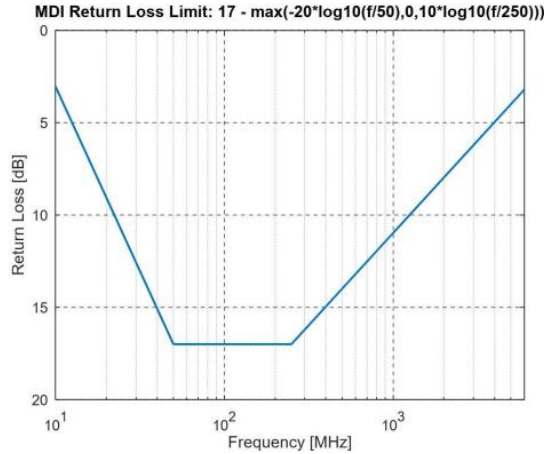
$$RL(f) > \begin{cases} 17+20\log_{10}(\frac{f}{50}) & f \le 50 \\ 17 & 50 < f \le 250 \\ 17-10\log_{10}(\frac{f}{250}) & f > 250 \end{cases}$$

where f is in MHz and the limit is defined in the frequency range

$10MHz < f < F_{max}$

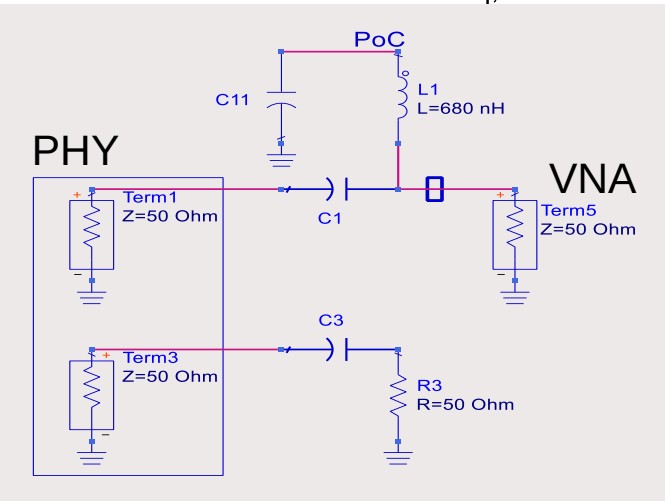
This limit should apply to both coax cables and balanced pairs

NOTE: F_{max} is expected to be few GHz



A proposed MDI RL to 802.3dm

1. https://www.ieee802.org/3/dm/public/0724/jonsson_houck_3dm_02_07_15_24.pdf



- The inductance of a real inductor drops by temperature and current. The simulated value of 0.68µH is an assumed minimum inductance that does not violate the proposed RL limit.
- It is seen that the proposed RL limit results in a high pass filter of about 6MHz.
- Also, note that noises below 1MHz are attenuated by more than 15dB when inductance is at 0.68µH. (would be 12dB rejection at 1µH)

PoC filter examples and total DCR for 802.3dm

A <u>single 1µH inductor</u> may be used for 802.3dm.

- PFL1609-102 (**up to 500mA**)
  - AEC-Q200 (–40°C to +125°C)
  - 1.8 x 1.1 x 1 mm
  - DCR: 230mΩ @25°C
  - SRF: 460MHz
- WCLA2520V1-1R0-R (**up to 800mA**)
  - AEC-Q200 (-55°C to +125°C)
  - 2.9 x 2.5 x 2.1 mm
  - DCR: 130mΩ @25°C
  - SRF: 345MHz
- PFL3215-102 (**up to ~2000mA**)
  - Industrial (-40°C to 85°C)
  - 3.2 x 2.5 x 1.5 mm
  - DCR: 38mΩ @25°C
  - SRF: 375MHz

- Single inductor PoC filter
- Lower DCR
- Smaller board area
- High SRF to provide higher BW

- For Industrial applications
- Current may be limited by connector and cable types

Power and Board space savings for 802.3dm vs GMSL2

Current Level	GMSL2 @ 105C		802.3dm* @ 105C	
	C-2L-300	**C-4L-1000**	**PFL1609**	**WCLA2520**
300mA	167mW	70mW	27mw	15mw
500mA	-	197mW	75mw	43mW
800mA	-	503mW	-	109mW

Size	GMSL2		802.3dm*	
	C-2L-300	**C-4L-1000**	**PFL1609**	**WCLA2520**
Total Footprint	$10mm^2$	$42mm^2$	$2mm^2$	$7mm^2$
Total Volume	$27mm^3$	$150mm^3$	$2mm^3$	$15mm^3$

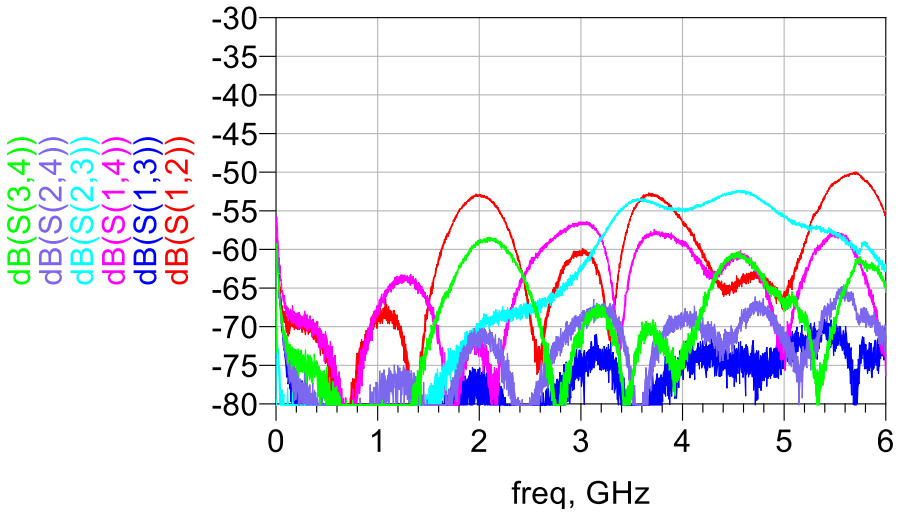
- Compare numbers in red to red and blue to blue.
- Footprint does not include practical space between inductors

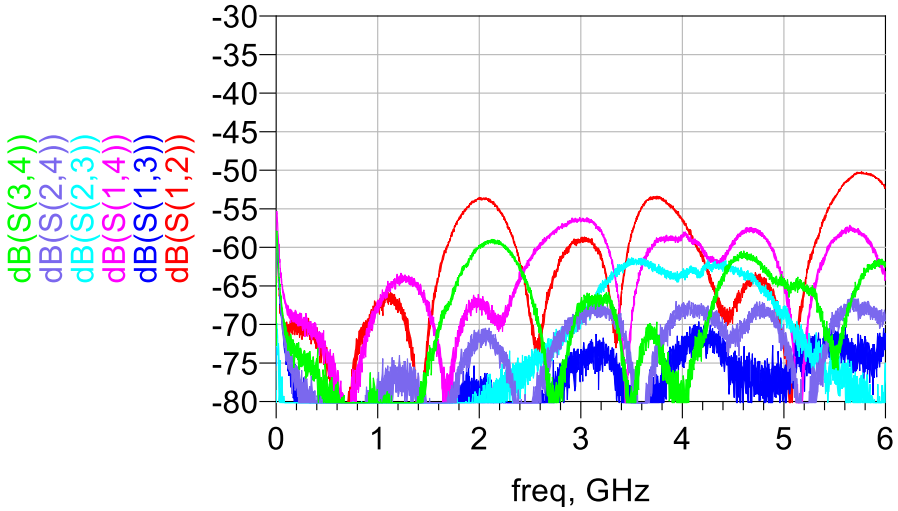
* Using single 1µH inductor.

- Using a single 1µH inductor, power saving in PoC filter alone may be more than a transceiver power designed based on SerDes technologies[1].
- Power, size and relative cost are optimized all at the same time using a single 1µH inductor.
- For implementation based on GMSL2, see the evaluation boards which are publicly available[2,3].

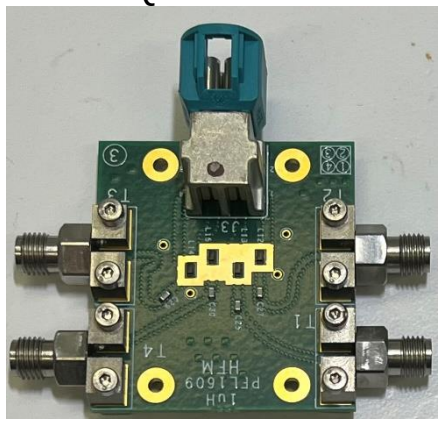
1. https://grouper.ieee.org/groups/802/3/dm/public/0724/Chini_Tazebay_3dm_01a_0724.pdf
2. https://www.analog.com/media/en/technical-documentation/data-sheets/max96717ev.pdf
3. https://www.analog.com/media/en/technical-documentation/data-sheets/max96724-bak-evk-max96724r-bak-evk.pdf

4-port Cross-talk measurements using PFL1609-102 for 802.3dm

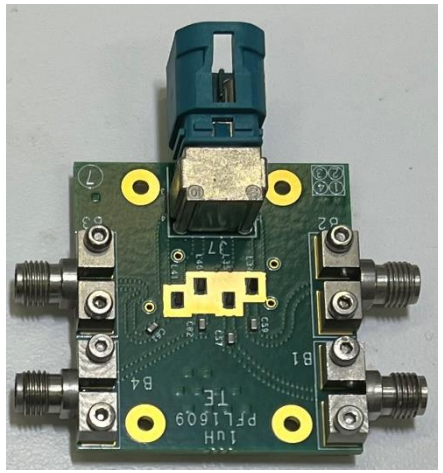




Quad HFM



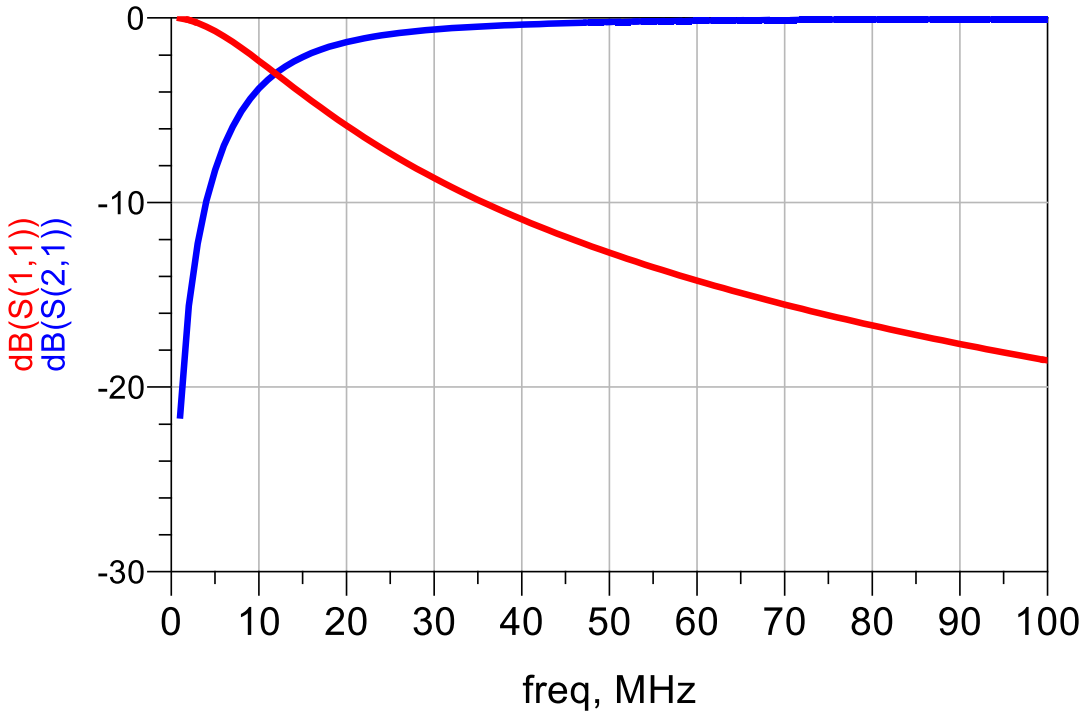
Quad MATE-AX

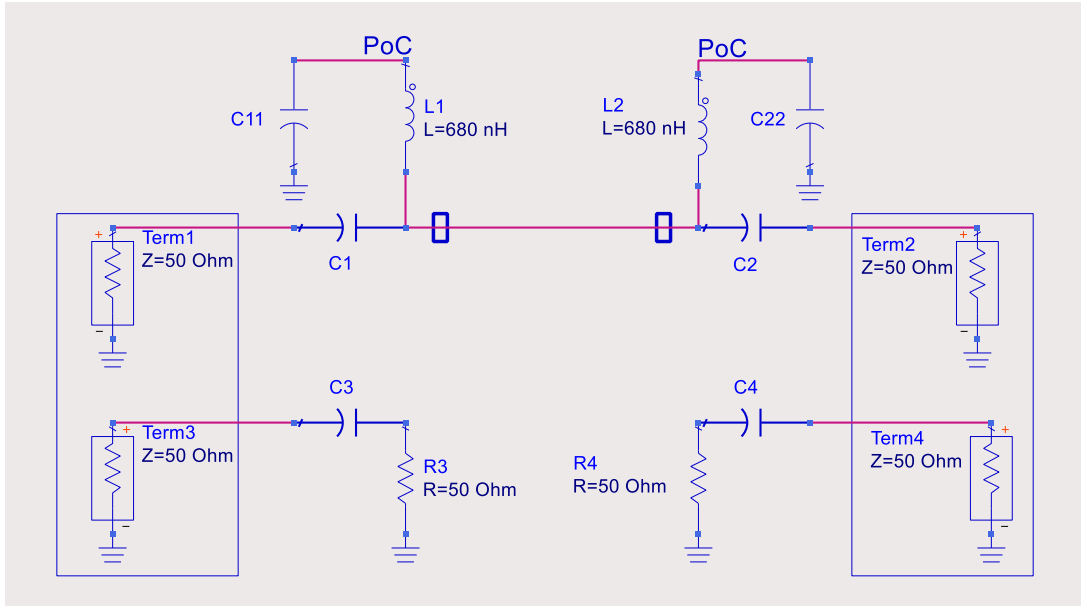


- The cross talk between ports is less than 50dB for frequencies below 5GHz while PoC inductors placed within half an inch area on the board.
- Compare with the PoC filters for a Quad deserializer that supports both GMSL1 and GMSL2 in the link referenced below.

  https://www.analog.com/media/en/technical-documentation/data-sheets/max96724-bak-evk-max96724r-bak-evk.pdf

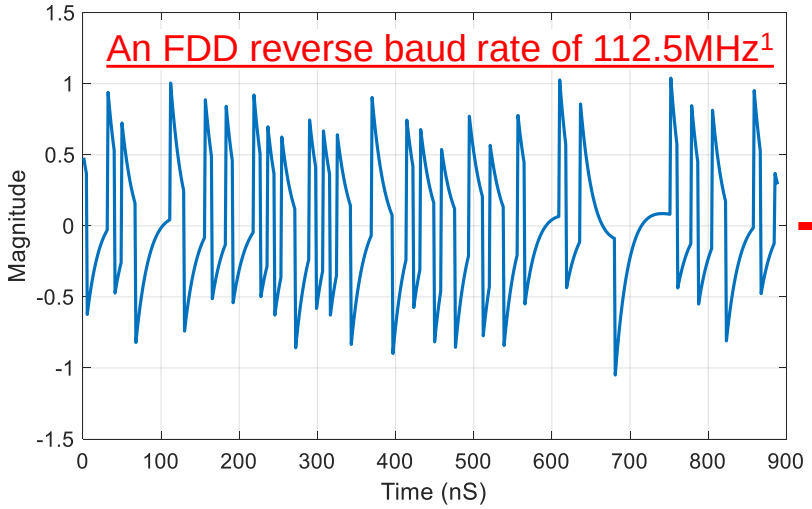
Channel IL/RL resulting from PoC filtering



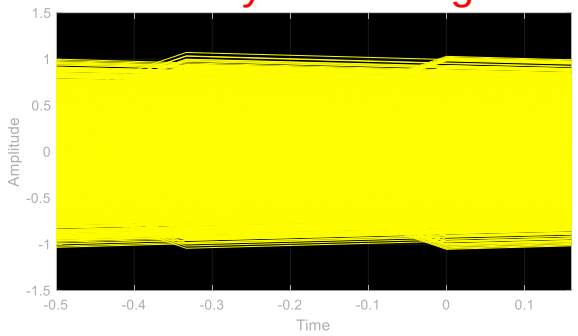


- A simulated value of 0.68µH is an assumed minimum inductance that does not violate the proposed RL limit.
- The additional effect of link segment return loss, imperfect PHY terminations (+/-10%) and Hybrid circuit (if required) should be considered for the analysis of total channel return loss.
- The effect of the high return loss on the FDD reverse link should be analyzed.

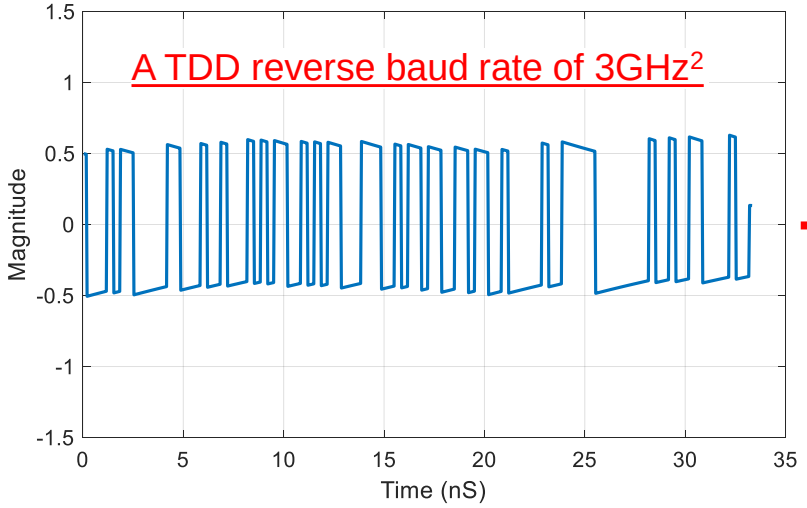
Signal dynamic range and distortion resulting from PoC filtering



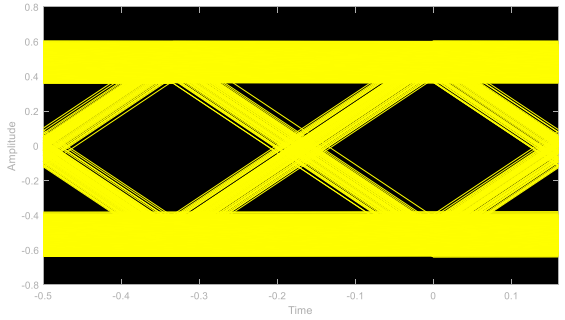
~ 2.1X dynamic range



Corresponding eye diagram



~1.35X dynamic range



Corresponding eye diagram

- Large dynamic range requires higher transceiver voltage and affects power consumption in the PHY (1V, 1.8 or more?).
- In the case of FDD, the eye is completely closed at the input of the receiver while it is open for TDD (Just for PoC filer effect)

1. https://www.ieee802.org/3/dm/public/0724/sedarat_3dm_202407.pdf
2. https://www.ieee802.org/3/dm/public/0724/Chini_Tazebay_3dm_01a_0724.pdf

Summary

- The proposed MDI-RL helps with PoC filter design with the following benefits:
  - Inductors with higher SRF (smaller parasitic capacitance) and thus high bandwidth with a single inductor.
  - Smaller footprints on the board.
  - Lower DCR which means less power loss and self-heat from the PoC inductors.
  - Lower noise and better reliability due to load variations (L $\frac{di}{dt}$).
  - Better rejection of low frequency noises (12-15dB noise rejection for frequencies below 1MHz).
  - Less cross talk coupling, allowing for compact board design in a quad deserializer.
  - Lower complexity (relative cost).

- In return for all the benefits, there is a trade-off between signal baud rate and lower part of return loss limit that should be observed.

Conclusions

- PoC is essential in automotive imaging sensor applications.
- Therefore, there is an opportunity for 802.3dm to address this need with optimized techniques which will yield to a more competitive solution.
- There is an inherent disadvantage for PoC in FDD solutions, on the other hand, TDD provides a significant advantage in terms of simplicity, power efficiency, cross talk, low frequency noise rejection and relative cost for PoC implementation.

Thank you!