

#### Beyond the crystal: Innovating ADAS with Simplified Sensor Modules Contribution to 802.3dm Task Force September 17, 2024

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# Topics

- What is crystal-less operation?
- Advantages of crystal-less operation
- How does crystal-less operation work
- What happens when a clock is not provided

## What is crystal-less operation

- Crystal-less operation gives the ability for the PHY on the module sensor to run with **no** crystal.
- Previous ethernet standards require a precise clock from a crystal or oscillator on both sides of the link to maintain accurate data transmission



Referenced: https://www.ieee802.org/3/dm/public/0724/houck\_3dm\_01\_0724.pdf

## Advantages of crystal-less operation

- Reduced Cost and Component count
  - No crystal oscillator
  - Lower power consumption (removal of crystal)
  - Reduces Camera PCB size
  - Reliability removal of moving part (oscillator)
- Simplified System design
  - Eliminates the need for synchronization techniques
- Simplified Timing synchronization
  - Using backchannel for clock synchronization ensure both sides of the link are locked to the same timing reference.
    - This could improve overall timing precision and reduce timing discrepancies.

Referenced: <u>https://www.ieee802.org/3/dm/public/0724/houck\_3dm\_01\_0724.pdf</u> Referenced: <u>https://www.ieee802.org/3/dm/public/0724/broedel\_matheus\_dm\_01\_size\_07152024.pdf</u>

Examp	ole for PCB size	reduction
Simulated for a 3MPx ima	ager:	
<ul> <li>(20x20-17x17) mm<sup>2</sup>/20</li> <li>(20x20-17x17) mm<sup>2</sup>/20</li> </ul>	$0x20 \text{ mm}^2 = 27.75\%$	
Expected that 2 PCB Is	ayers can be removed.	
<ul> <li>Potentially HDI-techno</li> </ul>	ology no longer necessar	<b>y.</b> 17
TOP Placement		
HDI = High Density Intercon	inect	
HDI - High Density Intercon	IEEE 802.3dm Task Force	

### How does crystal-less operation work

- The 100Mbps Signal sent to PHY
- Clock and Data Recovery (CDR)
  - The CDR extracts a clock from the 100Mbps continuously transmitted signal.
- Phase Lock Loop (PLL)
  - Used to lock to timing information from the 100Mbps backchannel to generate the required high speed clock for the PHY
- Clock Management Units (CMU)
  - Ensures the appropriate clock frequency is scaled depending on the link speed



#### What happens when a clock is not provided



#### Crystal less operation for Continuous Transmission vs. TDD

	802.3dm 100Mbps (Continuous Transmission)	802.3dm – 4Gbps (TDD)
Operation Type	Always Transmitting and Receiving	Time Division Duplex – Alternating Upstream and Downstream
Continuous Reference Clock	Always available	Only available during short periodic bursts
Crystal less Feasible	Yes	No/Possible?
CDR complexity	Low due to 100Mbps	High – Difficult to recover low jitter clock from 4Gbps TX
PLL Requirements	Low due to 100Mbps	<ul><li>Feasible?</li><li>PLL needs to handle switching between TX and RX</li><li>Unavailable reference clock leads to unstable TX</li></ul>
Jitter Sensitivity	Low due to 100Mbps	High – Difficult to recover low jitter clock from 4Gbps TX





It is proposed to provide **crystal-less operation** as a critical feature needed for 802.3dm to be competitive in camera module designs

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It is proposed to provide a **continuous clock reference** to simplify camera modules BOM and cost

Do not preclude timing recovery from 100Mbps without the use of a crystal



Essential technology, done right<sup>™</sup>