Relation between xMII, latency, and duplexing method

IEEE 802.3dm

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Motivation

- This presentation looks at the impact of the selected xMII speed on the overall Ethernet induced latency per hop.
- It distinguishes between the high speed downstream (DS) direction and the low speed upstream (US) direction.
- It considers 802.3ch and ASA-MLE for the DS and 802.3bw, 802.3ch with EEE, and ASA-MLE for the US.
- It shows that the latencies depend very much on actual system parameters selected, including the selected xMII speed.
- It shows that the shortest latencies can be achieved with 802.3ch (without EEE).
- It shows that all options can achieve the latency requirements of the camera and other sensor applications.

Content

- System overview
- xMII and latency in the DS
- xMII and latency in the US
- Summary and conclusion

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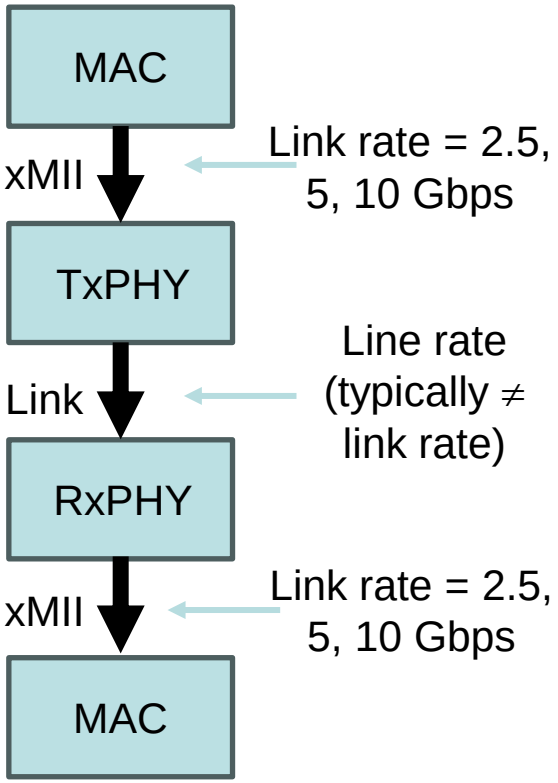
US = Upstream, low data rate direction
DS = Downstream, high data rate direction

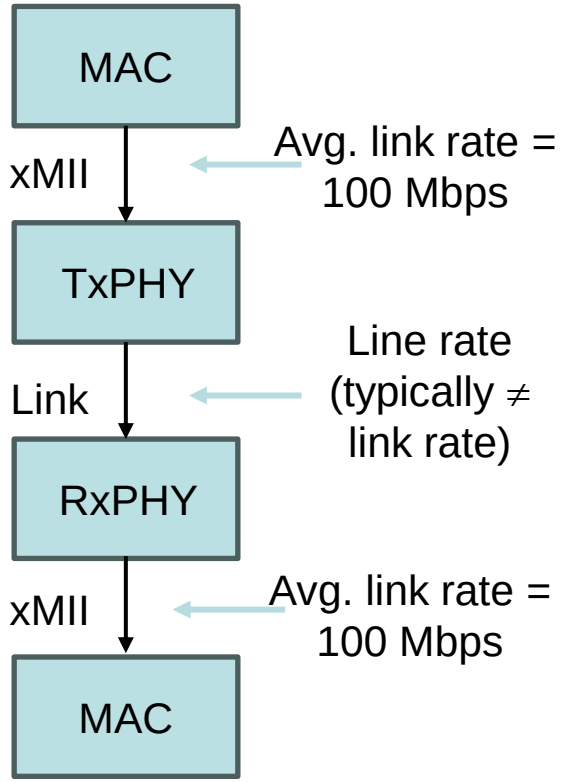
System overview.

DS



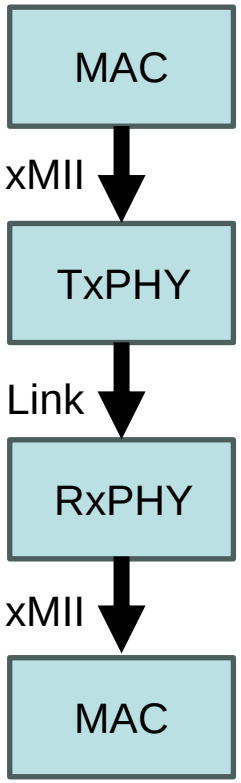
Assumption DS: Maximum length packets are sent to meet the data rate requirements.

US



Assumption US: Shorter length packets may be sent, when throughput reduction is acceptable.

Considered system parameters.



Packet frequency: Interval in which MAC may provide new packets in order to meet the nominal data rate. Depends on nominal data rate and Ethernet packet payload.

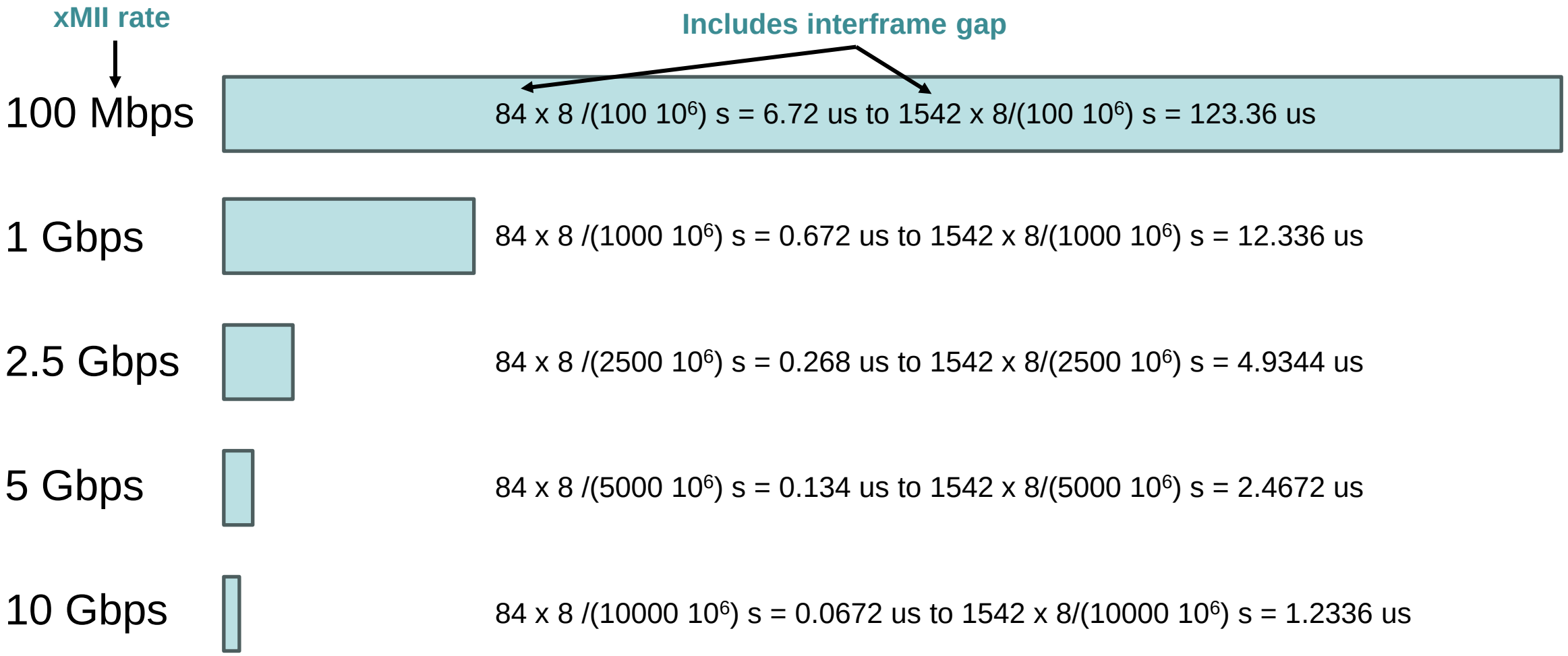
Tx+RxPHY delay: Bit level processing time. Depends on clock rate and processing effort (esp. FEC length). For 802.3 ch it decreases linearly with increasing line rate. Assumption therefore is that it decreases further with higher line rates, esp. if FEC is shorter.

Wait/wake times: Induced by EEE with wake signal or TDD cycle schedule. Depends on defined system parameters.

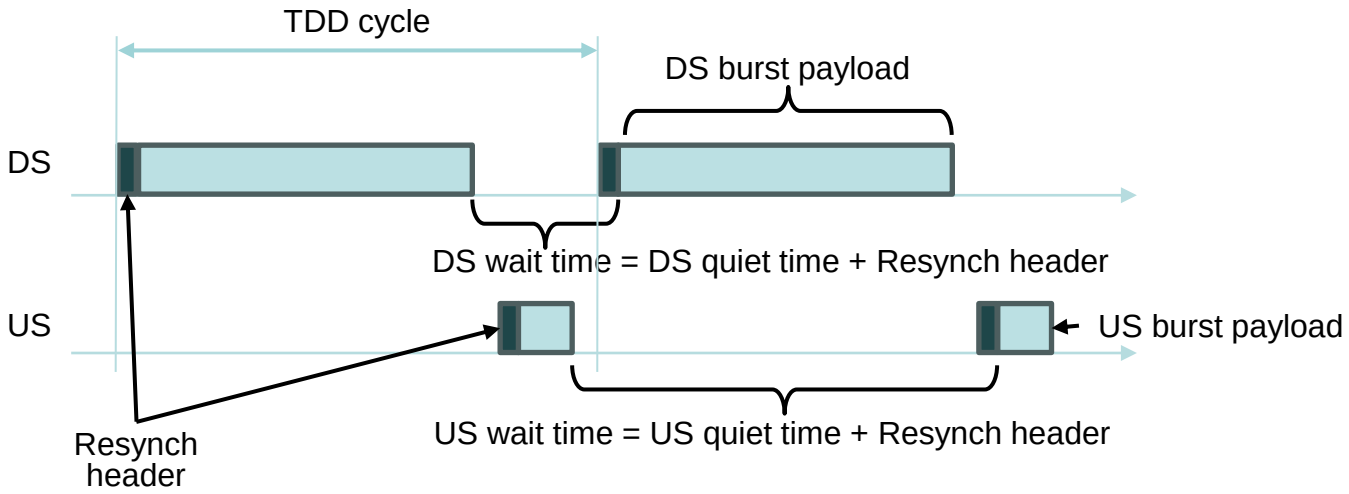
Propagation delay: Physics. Here maximum is assumed to be 90ns in all cases.

xMII/packet latency/delay: Full packet needs to be received in order to process the CRC. Depends on xMII rate and packet length. Differs from packet frequency if xMII rate differs from nominal data rate.

Min/max Ethernet packet latencies.



ASA-MLE nomenclature.



- Each burst payload contains an integer number of codewords.
- Each codeword contains 208 bytes of payload data.
- The TDD cycles/bursts on PHY level are not aligned with MAC level Ethernet packets.
- Each DS or US burst payload may thus contain several or only parts of one Ethernet packet, depending on the Ethernet packet length.

	Line rate	TDD cycle	DS Eth. payload bytes	DS wait time	US Eth. payload bytes	US wait time	Est. Tx + RxPHY delay
ASA-MLE 2.5	4Gbps	3.95us	1248	1.072us	208	3.472us	2.88us
ASA-MLE 5	8Gbps	2.99us	1872	0.832us	208	2.752us	1.44us
ASA-MLE 10	12Gbps	26.83us	33696	0.912us	416	26.51us	0.96us
ASA-MLE 10*	16Gbps	2.99us	3744	0.832us	416	2.752us	0.72us

*1Gbps US speed

↑ Decrease est. linear with increased line rate compared with 802.3ch

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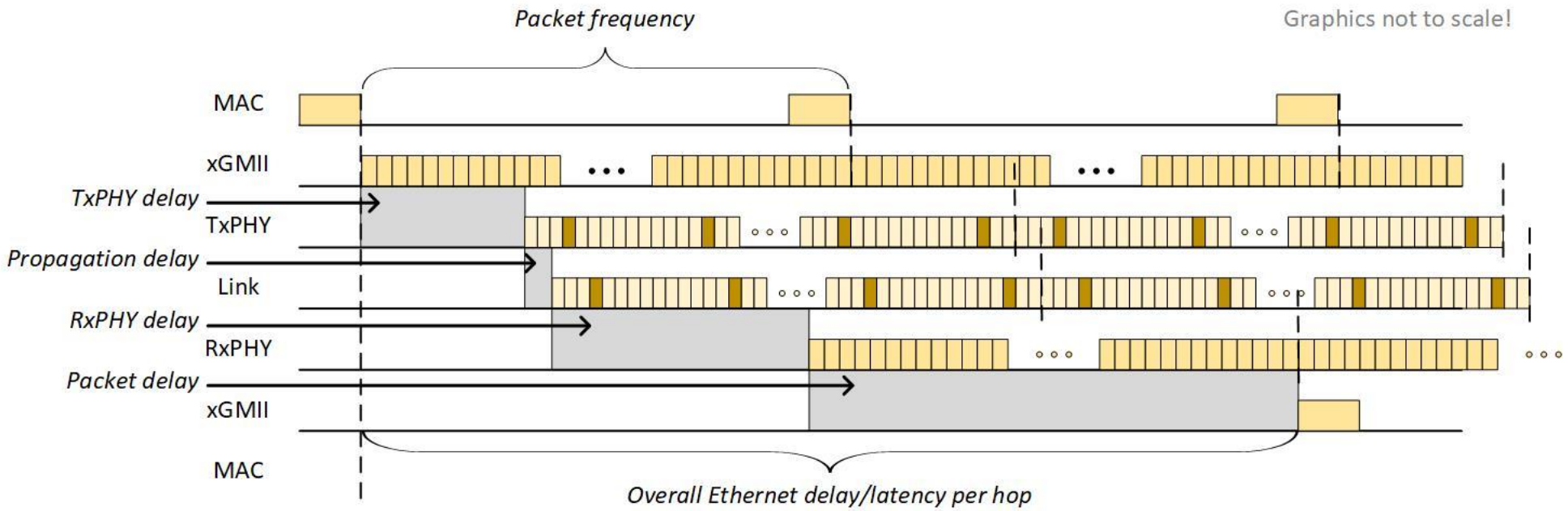
Latency in the DS for IEEE 802.3ch with XGMII



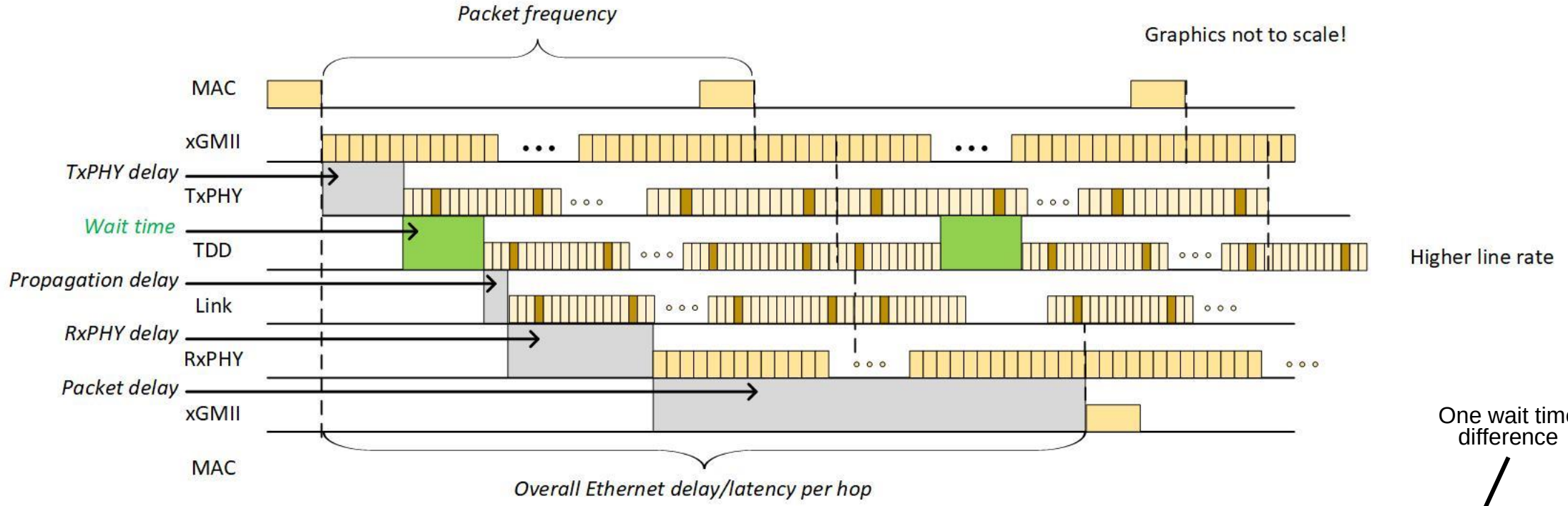
Original content/bit
PHY processed bit
Added/redundant bit

	xMII rate	Line rate	Max. packet delay/ frequency	Tx + RxPHY delay (no interleaving)	Propaga-tion delay	Overall Eth. hop delay
2.5GBASE-T1	2.5Gbps	2.813Gbps	4.93us	4.096us	90ns	**9.12us**
5GBASE-T1	5Gbps	5.615Gbps	2.46us	2.048us	90ns	**4.60us**
10GBASE-T1	10Gbps	11.25Gbps	1.23us	1.024us	90ns	**2.34us**

Max. interfering delay

The 802.3ch Tx + RxPHY delay decreases linearly with increasing line rate.

Latency in the DS for ASA-MLE with XGMII



	xMII rate	Line rate	Packet delay/ frequency	Tx + RxPHY delay (no interleaving)	Propaga-tion delay	Wait time	1542 byte packets per TDD cycle	Overall Eth. hop delay → min. → max
ASA-MLE 2.5	2.5Gbps	~~2.813~~ → 4Gbps	4.93us	~~4.096~~ → 2.88us	90ns	1.07us	0.81	~~9.12~~ → 7.9 → 8.97us
ASA-MLE 5	5Gbps	~~5.615~~ → 8Gbps	2.46us	~~2.048~~ → 1.44us	90ns	0.83us	1.21	~~4.60~~ → 3.99 → 4.82us
ASA-MLE 10	10Gbps	~~11.25~~ →12Gbps	1.23us	~~1.024~~ → 0.96us	90ns	0.91us	21.85	~~2.34~~ → 2.28 → 3.19us
ASA-MLE 10*	10Gbps	~~11.25~~ →16Gbps	1.23us	~~1.024~~ → 0.72us	90ns	0.83us	2.43	~~2.34~~ → 2.04 → 2.87us

One wait time difference

*1Gbps US speed

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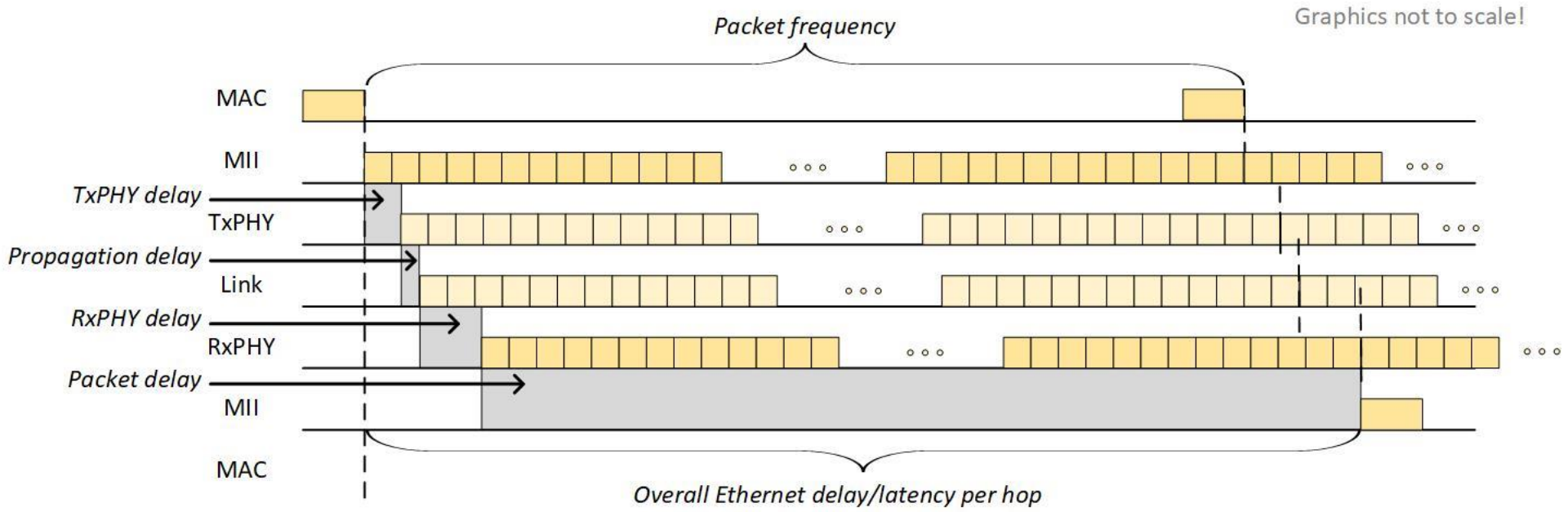
Latency in the US for 802.3bw with MII

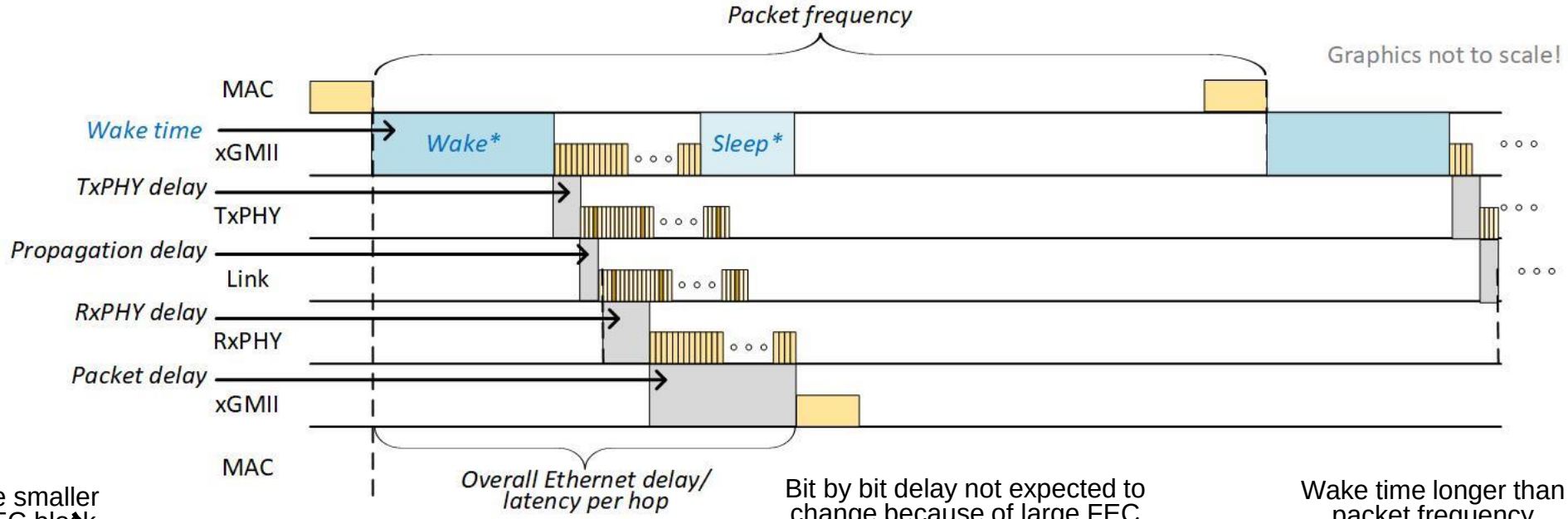


	xMII rate	Eth. packet length	Eff. through-put	Packet delay/ frequency	Tx + RxPHY delay	Propaga-tion delay	Overall Eth. hop delay
100BASE-T1	100Mbps	1542 bytes	96%	123.36us	1.320us	90ns	**124.77us**
100BASE-T1	100Mbps	84 bytes	1.75%	6.72us	1.320us	90ns	**8.13us**

→ Has to ensure that no longer packets can enter the segment

** How a high frequency EEE might be organized is outside the scope of this presentation.*

Latency in the US for 802.3ch with EEE and XGMII



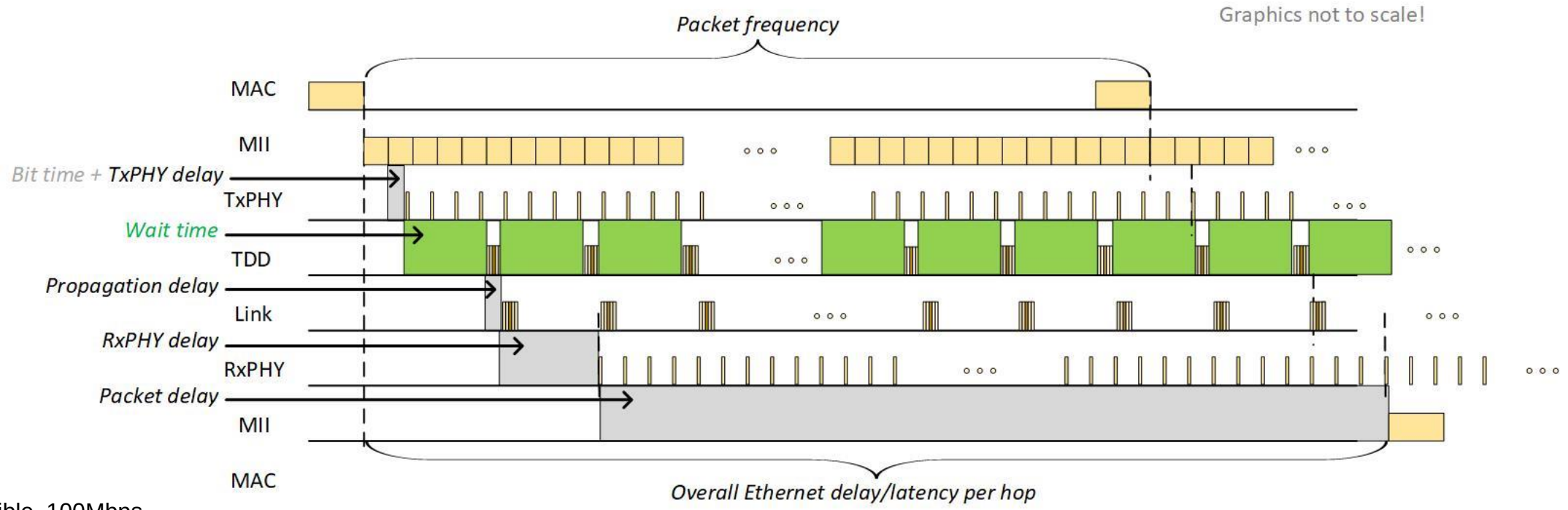
84 bytes are smaller than one FEC block

Bit by bit delay not expected to change because of large FEC blocks

Wake time longer than packet frequency

	US rate	Packet frequency	xMII rate	Tx + RxPHY delay (no interleaving)	Propaga-tion delay	Packet delay	Wake time	Overall Eth. hop delay
2.5GBASE-T1	100Mbps	123.36us	2.5Gbps	4.096us	90ns	4.93us	25.6us	~~124.77~~ → 34.72us
5GBASE-T1	100Mbps	123.36us	5Gbps	2.048us	90ns	2.46us	12.8us	~~124.77~~ → 17.4us
10GBASE-T1	100Mbps	123.36us	10Gbps	1.024us	90ns	1.23us	6.4us	~~124.77~~ → 8.74us
2.5GBASE-T1	100Mbps	6.72us	2.5Gbps	4.096us	90ns	0.268us	No EEE	~~8.13~~ → 4.45us
5GBASE-T1	100Mbps	6.72us	5Gbps	2.048us	90ns	0.134us	No EEE	~~8.13~~ → 2.27us
10GBASE-T1	100Mbps	6.72us	10Gbps	1.024us	90ns	0.067us	No EEE	~~8.13~~ → 1.8us

Latency in the US for ASA-MLE with MII (1)



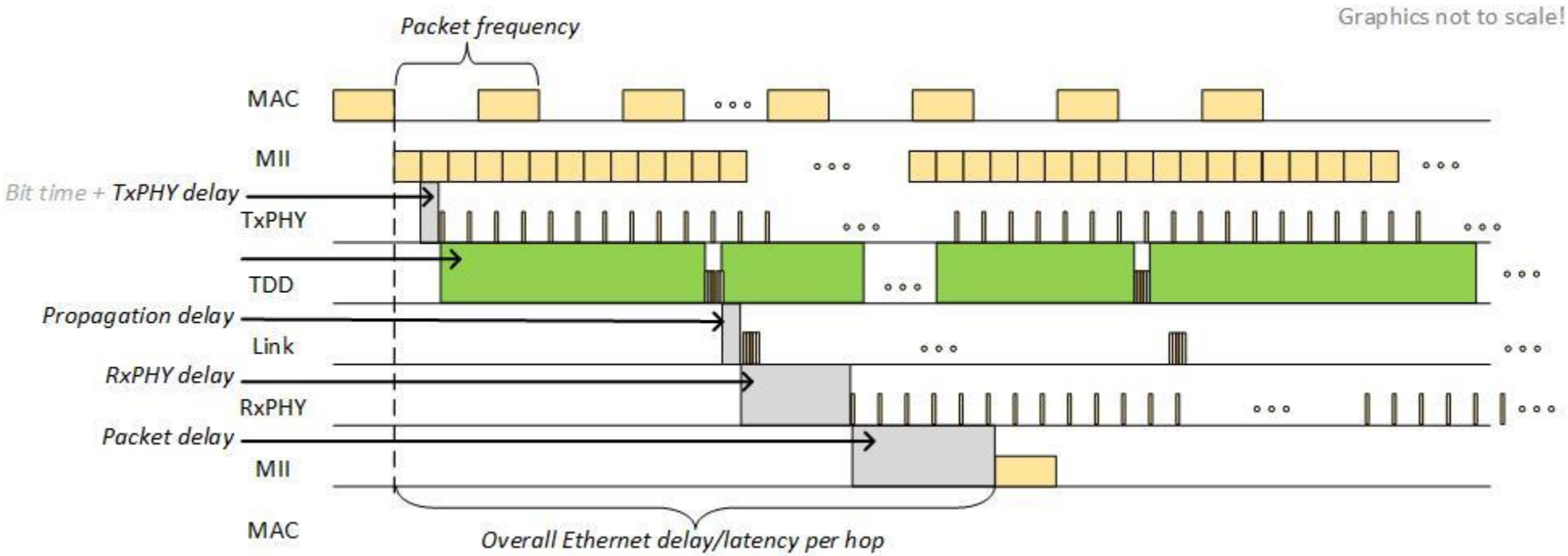
*1Gbps possible, 100Mbps for comparison reasons

Slower than expected

Spread over number of TDD cycles, filled with idles up to capacity

	US rate/ xMII rate	Packet frequen-cy/delay	Bit time	Tx + RxPHY delay	Propa-gation delay	Wait time	TDD cycles/ pack. freq.	Payload bytes/ US burst	Act. Eth. bytes/ US burst	Overall Eth. hop delay →min → max
ASA-MLE 2.5	100Mbps	123.36us	10ns	2.88us	90ns	3.472us	31.23	208	49.375	~~124.77~~ → ~~34.72~~ → 126.34 → 129.8us
ASA-MLE 5	100Mbps	123.36us	10ns	1.44us	90ns	2.752us	41.26	208	37.41	~~124.77~~ → ~~17.4~~ → 124.9 → 127.65us
ASA-MLE 10	100Mbps	123.36us	10ns	0.96us	90ns	26.51us	4.65	416	360.28	~~124.77~~ → ~~8.74us~~ → 124.42 → 150.93us
ASA-MLE 10*	100Mbps*	123.36us	10ns	0.72us	90ns	2.752us	41.26	416	37.41	~~124.77~~ → ~~8.74us~~ → 124.18 → 126.93us

Latency in the US for ASA-MLE with MII (2)



	US rate/ xMII rate	Packet frequen-cy/delay	Bit time	Tx + RxPHY delay	Propa-gation delay	Wait time	TDD cycles/ packet freq.	Eth. Packets/ US burst	Overall Eth. hop delay →min → max
ASA-MLE 2.5	100Mbps	6.72us	10ns	2.88us	90ns	3.472us	1.7	2.48	~~8.13~~→ ~~4.45~~→9.7→13.17us
ASA-MLE 5	100Mbps	6.72us	10ns	1.44us	90ns	2.752us	2.25	2.48	~~8.13~~→~~2.27us~~→8.26→11us
ASA-MLE 10	100Mbps	6.72us	10ns	0.96us	90ns	26.51us	0.25	4.95	~~8.13~~→ ~~1.8us~~→7.78→34.29us
ASA-MLE 10*	100Mbps*	6.72us	10ns	0.72us	90ns	2.752us	2.25	4.95	~~8.13~~→ ~~1.8us~~→7.54→10.29us

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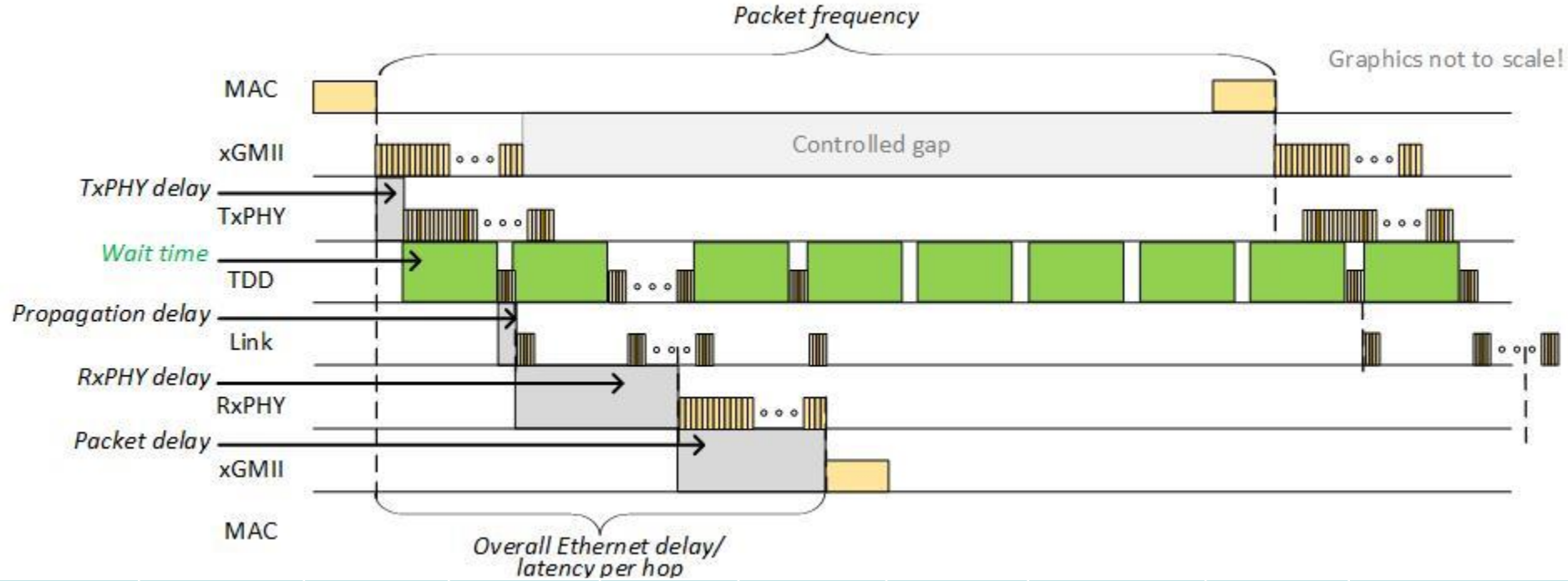
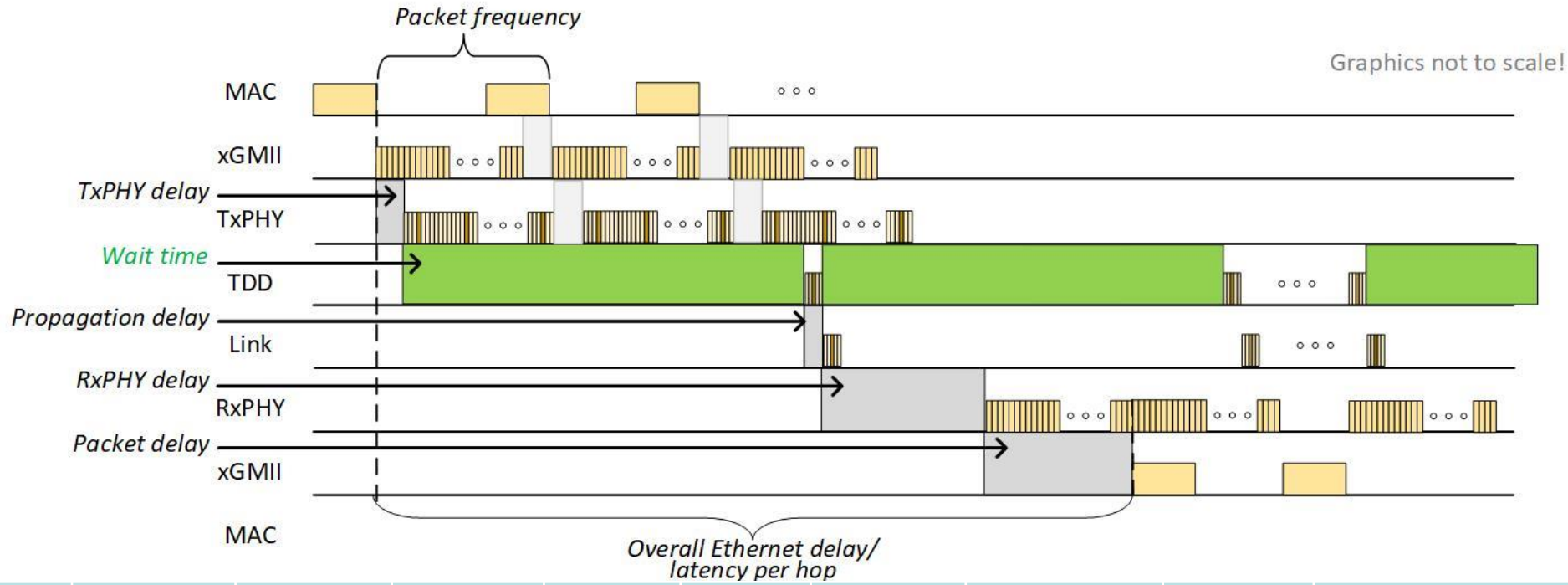
Latency in the US for ASA-MLE with XGMII (1)



	Nominal US rate	Packet frequen-cy	XMII rate	Tx + RxPHY delay	Propa-gation delay	Packet delay	Wait time	TDD cycles/ pack. freq.	TDD cycles needed	Overall Eth. hop delay →min → max
ASA-MLE 2.5	100Mbps	123.36us	2.5Gbps	2.88us	90ns	0.268us	3.472us	31.23	7.4	~~124.77~~ → ~~34.72~~ → 31.09 → 34.56us
ASA-MLE 5	100Mbps	123.36us	5Gbps	1.44us	90ns	0.134us	2.752us	41.26	7.4	~~124.77~~ → ~~17.4~~ → 22.69 → 25.45us
ASA-MLE 10	100Mbps	123.36us	10Gbps	0.96us	90ns	0.067us	26.51us	4.65	3.7	~~124.77~~ → ~~8.74us~~ → 80.87 → 107.39us
ASA-MLE 10*	100Mbps*	123.36us	10Gbps	0.72us	90ns	0.067us	2.752us	41.26	3.7	~~124.77~~ → ~~8.74us~~ → 10.02 → 12.77us

*1Gbps possible, 100Mbps for comparison reasons

Latency in the US for ASA-MLE with XGMII (2)



	Nominal US rate	Packet frequen-cy	XMII rate	Tx + RxPHY delay	Propa-gation delay	Wait time	TDD cycles/ pack. freq.	TDD cycles needed	Overall Eth. hop delay →min → max
ASA-MLE 2.5	100Mbps	6.72us	2.5Gbps	2.88us	90ns	3.472us	31.23	0.4	~~8.13~~ → ~~4.45~~ → 3.24 → 6.71us
ASA-MLE 5	100Mbps	6.72us	5Gbps	1.44us	90ns	2.752us	41.26	0.4	~~8.13~~ → ~~2.27~~ → 1.66 → 4.42us
ASA-MLE 10	100Mbps	6.72us	10Gbps	0.96us	90ns	26.51us	4.28	0.2	~~8.13~~ → ~~1.8~~ → 1.12 →27.63us
ASA-MLE 10*	100Mbps*	6.72us	10Gbps	0.72us	90ns	2.752us	41.26	0.2	~~8.13~~ → ~~1.8~~ →0.88→3.63us

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Summary and conclusion

- This presentation detailed the latency impacts of different transmission technologies, transmission speeds and xMII interfaces.
  - For the DS 802.3ch and ASA-MLE were investigated using an xGMII interface.
  - For the US 802.3bw, 802.3ch with EEE, and ASA-MLE were investigated using an MII or xGMII interface.

- All investigated solutions show acceptable latency values.
  - For 802.3ch (without EEE) they were shortest.
  - Without interfering traffic, 802.3ch and 802.3bw have fixed latency values, while for ASA-MLE they may vary within the range of the max wait time length (because the Ethernet packet frequency does not correlate with the TDD PHY-cycle).
  - The latency values for the ASA-MLE US traffic additionally vary depending on the selected system parameters and xMII interface type. Using XGMII in the US instead of the MII may further reduce the latency.

- Latency still does not represent a crucial decision item between the duplexing options.

Thank You!