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Effects of the System Interface on Latency

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ETHERNOVIA

Some timing numbers around a vehicle

In an anti-lock braking system, your car's wheel speed is monitored and if wheel lock is detected, a sensor sends a message to a controller that releases and applies the brake up to 20 times per second, preventing a lock up and helping you maintain control of your vehicle.
https://www.wagnerbrake.com/technical/parts-matter/automotive-repair-and-maintenance/guide-to-abs-brakes.html

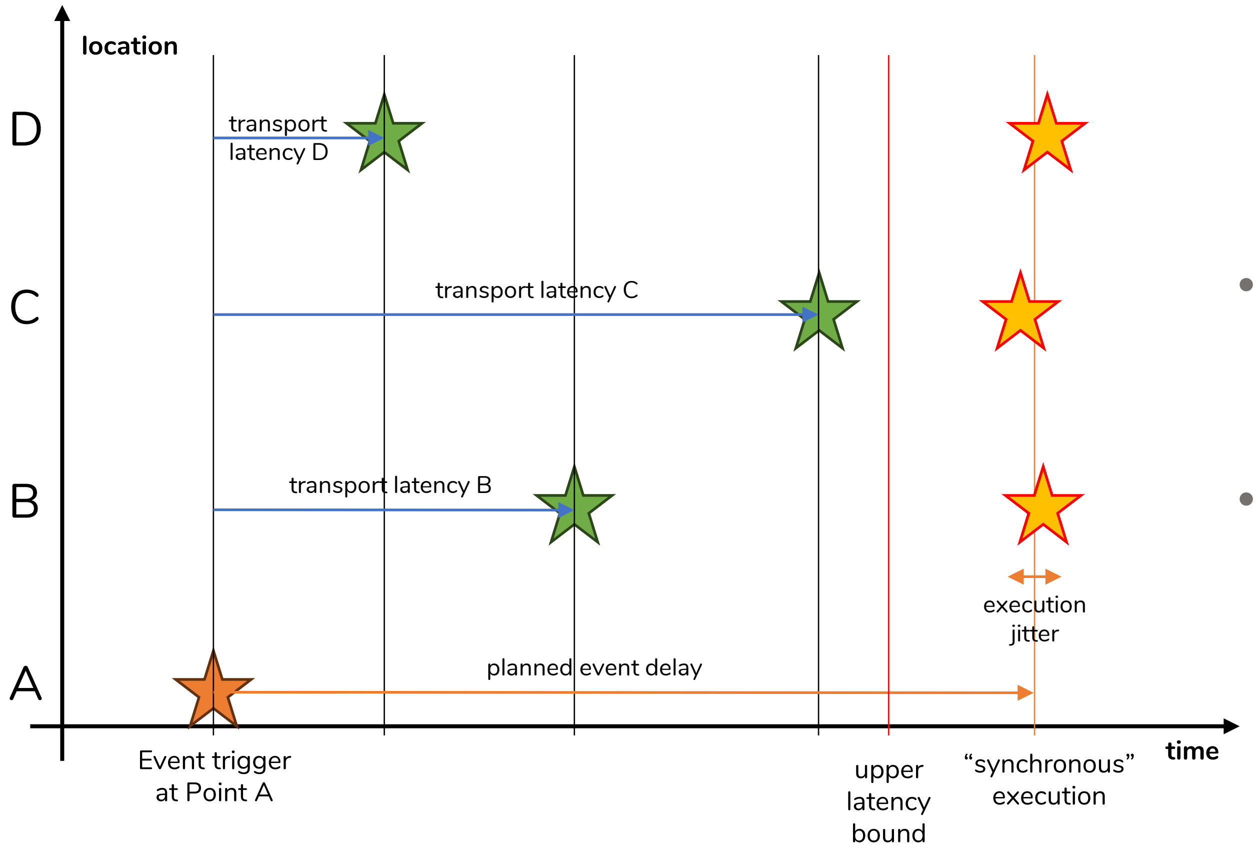
20 times per second = every 50ms

Airbags use nitrogen gas because it is non-toxic and inert, meaning it will not catch on fire or react with other materials. This entire inflation process takes place in **between 15 and 50 milliseconds**. This means only 0.015 to 0.050 seconds pass between the time the sensor detects the collision and the airbag inflates. 25 May 2022
https://mylawcompany.com/blog/how-serious-does-a-collision-have-to-be-for-airbags-to-deploy

During an image scan time of 30ms, the vehicle travels 2m at 250kph

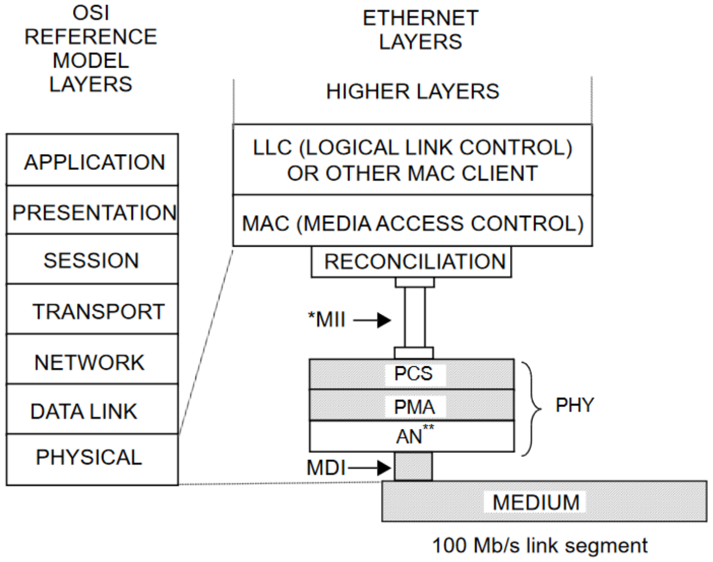
			Distance travelled					
			µs [mm]			ms [m]		
Vehicle Speed			1	10	100	1	10	100
1km/h	0.278m/s	0.6mph	0.000	0.003	0.028	0.000	0.003	0.028
50km/h	13.889m/s	31.1mph	0.014	0.139	1.389	0.014	0.139	1.389
80km/h	22.222m/s	49.7mph	0.022	0.222	2.222	0.022	0.222	2.222
100km/h	27.778m/s	62.1mph	0.028	0.278	2.778	0.028	0.278	2.778
120km/h	33.333m/s	74.6mph	0.033	0.333	3.333	0.033	0.333	3.333
250km/h	69.444m/s	155.3mph	0.069	0.694	6.944	0.069	0.694	6.944

Synchronous actions can be independent of Latency



- In order for events to occur synchronously, the transport only needs to be faster, than the maximum allowed latency (compare IEEE 1722 presentation time)
- This requires:
    1. Time Synchronization
    2. Bounded transport Latency
- Execution jitter will then depend on the event timing accuracy, no longer on the transport

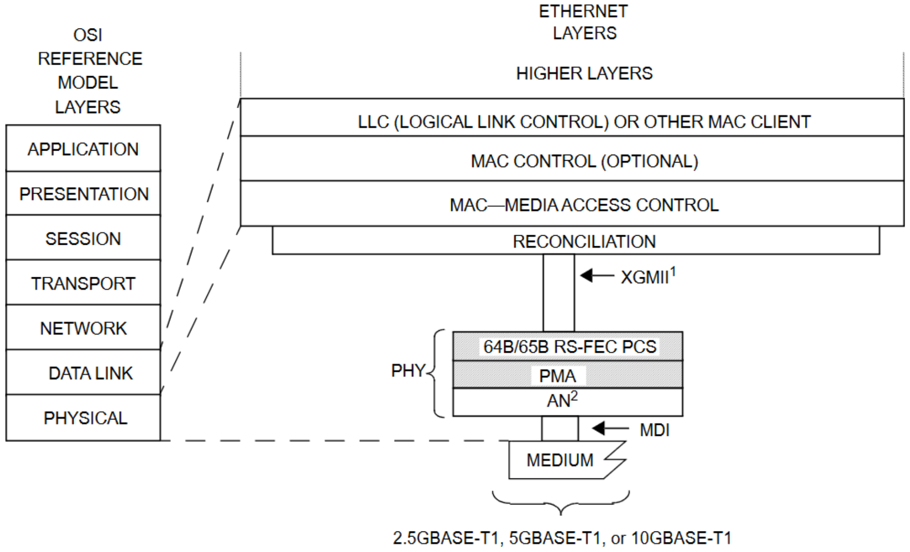
MII is optional



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
* Physical instantiation of MII is optional.
** Auto-Negotiation is optional

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 96–1—Architectural positioning of 100BASE-T1



MDI = MEDIUM DEPENDENT INTERFACE
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
NOTE 1—XGMII is optional
NOTE 2—Auto-Negotiation is optional

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

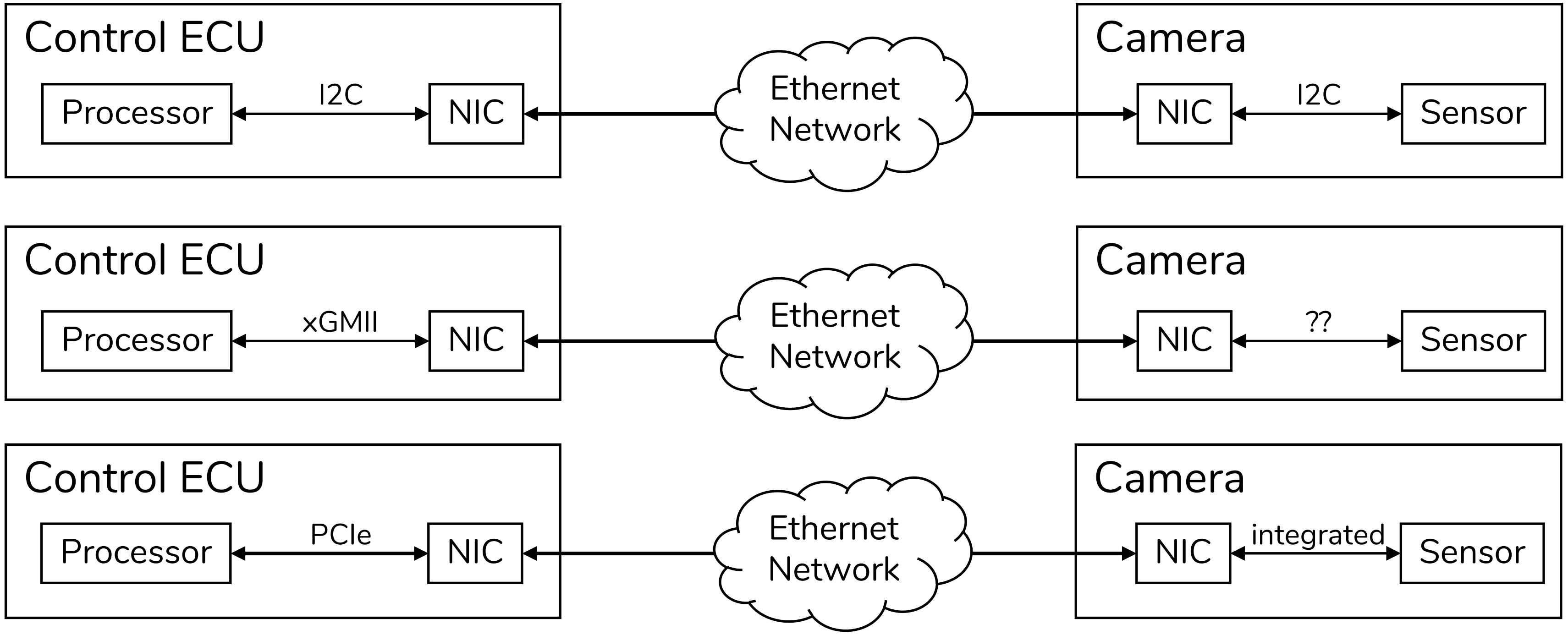
Figure 149–1—Relationship of 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model

IEEE Std 802.3-2022

If Latency is the problem, I2C is not the solution

Data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, up to 1 Mbit/s in Fast-mode Plus, or up to 3.4 Mbit/s in the High-speed mode. The bus capacitance limits the number of interfaces connected to the bus.

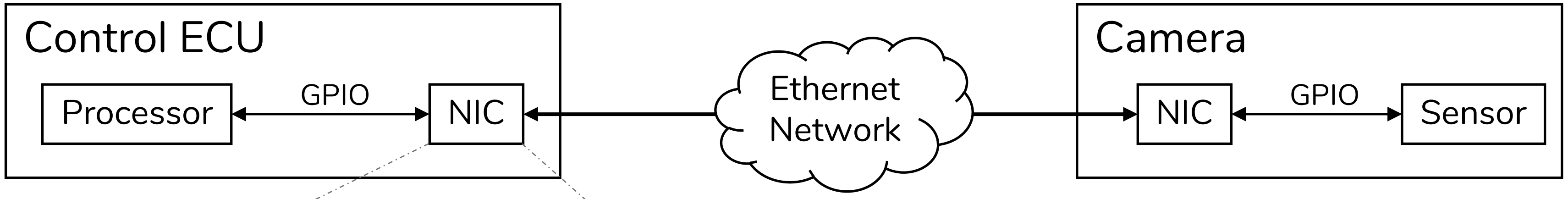
https://www.nxp.com/docs/en/user-guide/UM10204.pdf

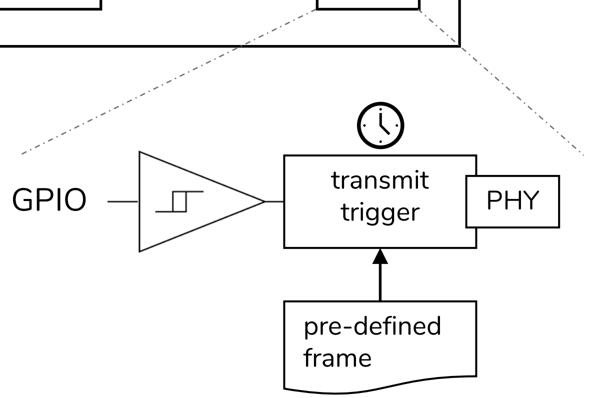


Don’t waste time between Processor and NIC!

Don’t waste time between NIC and Sensor!

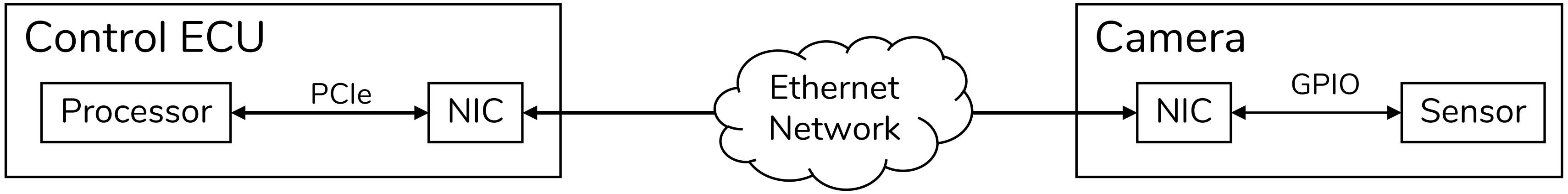
Physical or logical GPIO?





There is no MII interface in/to the NIC, so any wait times introduced by the PHY will be directly visible to the talker

A SW solution only requires PTP in the Processor and is likely much faster



Summary

- If latency is key, the “input” must be made efficent before low latency requirements are put on the transport
- Let’s not mix up Delay, Latency and Jitter
- Vehicle control loops mostly seem to operate on a 1 to 10ms time scale (see examples)

- IEEE 802.3 controls the PHY latency:
  - What RS-FEC code?
  - How much Interleaving?
  - Consider non-MII integrated PHY connections
- Below 1ms latency US for a minimum network (3 hops) seems feasible
  - 5ns/m × 15m = 75ns – link delays
  - 1500 Byte / 100Mbit/s = 120µs – max. store and forward latency last hop US
  - less than 5µs DS – PHY delay, with 10GBASE-T1 4x interleaving (IEEE Std 802.3: Table 149–20)
  - less than 1µs US – PHY delay, with 100BASE-T1 (IEEE Std 802.3: 96.10)
  - Network dependent TSN Latency – not under IEEE 802.3 control, must be optimized by the integrator

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