Jitter, Frequency Drift and Droop Proposal for TDD-based 802.3dm Specification

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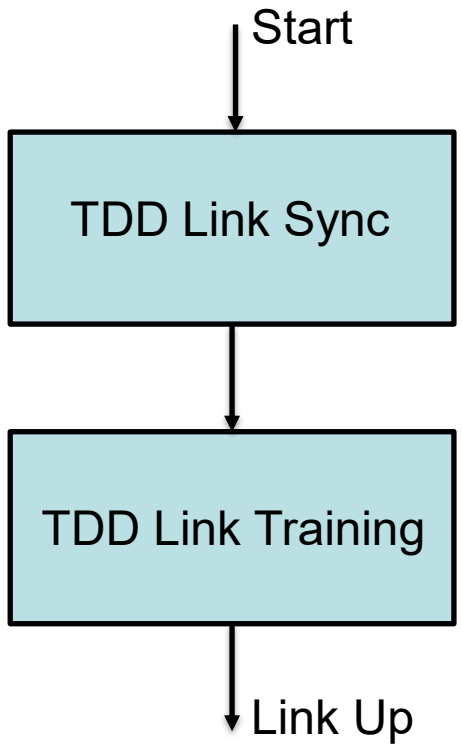
Ahmad Chini, Mehmet Tazebay
Broadcom

Contributors

- Afshin Momtaz, Broadcom
- Wei Zhang, Broadcom
- Kambiz Vakilian, Broadcom
- Mehdi Kilani, Broadcom
- Wei Lou, Broadcom
- Dongsoo Koh, Broadcom
- Xi Chen, Broadcom

TDD Linkup Process



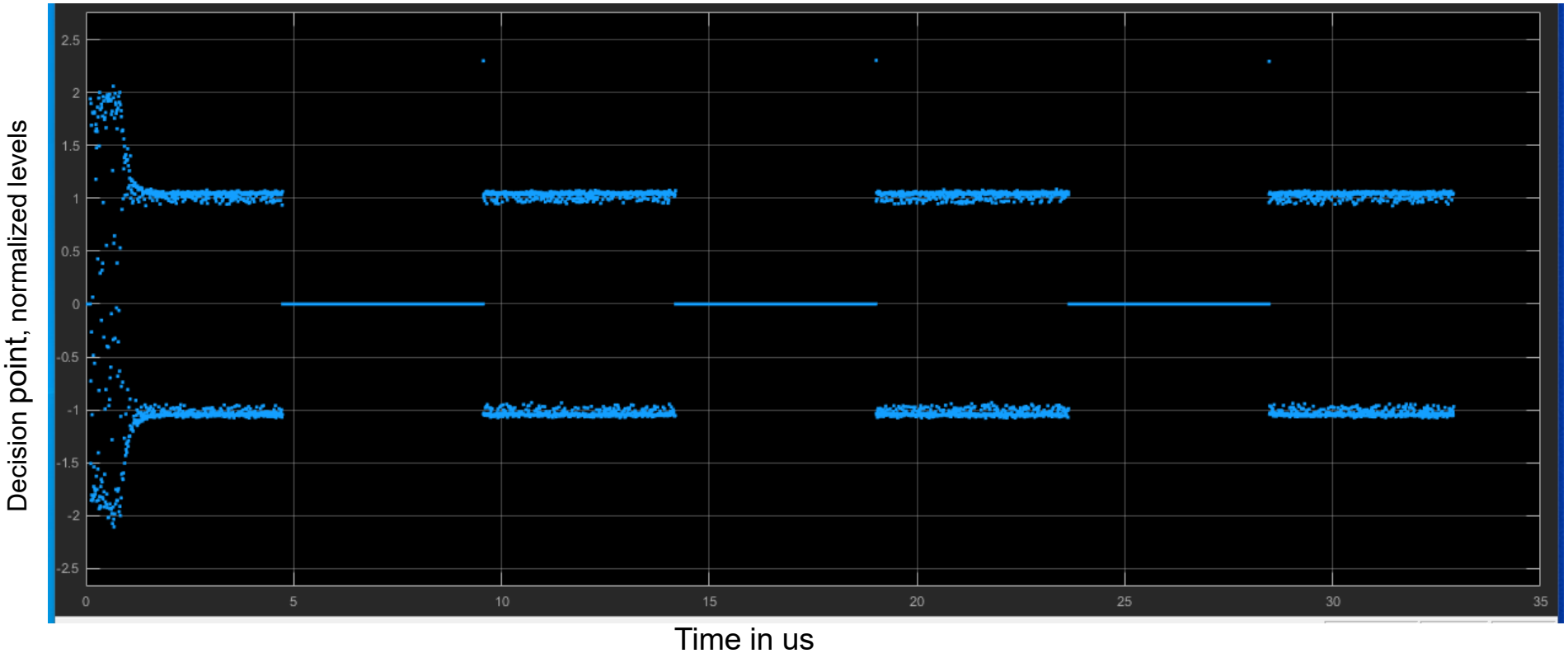
Timing Sync
Info Sync

Train at target Link Amplitude and Baud Rate*

- The Link Sync success is observable through the management interface as well as the MDI captures, and it is independently testable.
- The Link Sync has the same duty cycle in both directions, providing accurate timing and frequency lock for crystal-less Camera.
- The Link Training uses the normal mode duty cycles, and the behavior is observable for both through the management interface and MDI signal captures.

* No extended training required for PAM4.

Link Sync Simulation



- The crystal-less camera frequency was initially tuned using the TDD cycles to 200ppm accuracy.
- The next step shown takes less than 2us for CDR and DFE to converge.

  Generally, half duplex SerDes CDR algorithms are much quicker than the PHYs which are affected by echo.

Jitter and Frequency Drift Specifications

- The ECU side transmitter is assumed to use a continuous phase clock with a frequency offset less than +/-100PPM and with drift less than 1PPM/sec.
- The Camera side transmitter is assumed to use a continuous phase clock. The clock frequency shall track the ECU clock within +/-10ppm. There is no phase relation requirement between the Camera and ECU clocks. The tight locking requirement is meant to help the multi camera link synchronization.
- TDD refresh periods allow tuning the clock phase even if there is a drift during the silence periods. For that reason, some of the jitter and drift requirement for TDD-based 802.3dm may be relaxed as compared to the 802.3ch specification.

ECU side, Clock Leader

1. The RMS jitter measured in test mode2, shall be less than 1ps/2ps/4ps for the jitter frequencies greater than 100KHz when supporting 10Gbps/5Gbps/2.5Gbps correspondingly.
2. Peak to peak of Time Interval Error (TIE) measured in test mode1 over a period of 100us shall be less than 10ps/20ps/40ps when supporting 10Gbps/5Gbps/2.5Gbps correspondingly.

Camera side, Clock Follower

3. The RMS jitter shall be less than 1ps/2ps/4ps for jitter frequencies greater than 1MHz when supporting 10Gbps/5Gbps/2.5Gbps correspondingly. This requirement is verified in test mode1
4. Peak to peak of Time Interval Error (TIE) over any period of 10us, shall be less than 60ps/30ps/15ps for 2.5Gbps/5Gbps/10Gbps correspondingly. This requirement is verified in test mode1 over 50 overlapping periods of 10us each. The overlapping period of 5us is assumed.

Crystal-less Camera

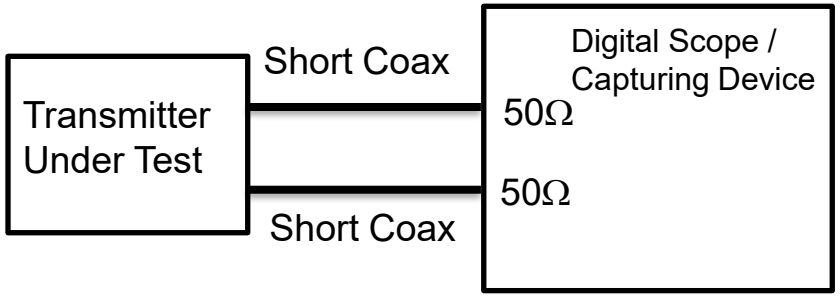
- The TIE measurement period of 10us is much less demanding than the 802.3ch 1ms measurement period. This allows for larger frequency and phase drift in the crystal-less camera.
- The ECU RMS jitter is measured for the frequencies above 100kHz. But for crystal-less camera, the RMS jitter is measured for the frequencies above 1MHz. Lower frequency jitter is limited by the TIE requirements.
- An existing digital PLL was verified by circuit design experts to meet the jitter and frequency drift requirements of a crystal-less camera. The frequency was stable over several seconds and the VCO jitter is less than 1ps when it is measured above 1MHz.
- The silicon temperature rise was measured in different conditions. The fastest recorded was 1C/20ms. Assuming 100PPM/C for a simpler VCO design, it takes 200us for 1PPM frequency change. That is less than 0.1PPM in 10us or 1ps change in TIE.

Jitter Test Modes

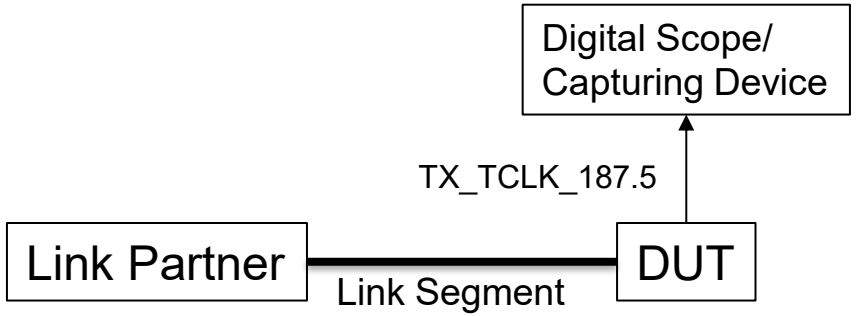
- **Test mode 1** enables the testing of timing jitter on MASTER and SLAVE transmitters. MASTER and SLAVE PHYs are connected over the link segment. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock; TX_TCLK_187.5 which is 187.5MHz.

- **Test mode 2** is for transmitter jitter testing on the MDI when the transmitter is in MASTER timing mode. When test mode 2 is enabled, the PHY shall transmit a periodic pattern of [+1 -1] with the transmitted symbols timed from its local clock of 3GHz.

Test Fixtures



- The transmitter test fixture1 for MDI Jitter, PSD, Droop and Nonlinearity measurements.
- For Coaxial applications, only one wire is connected.

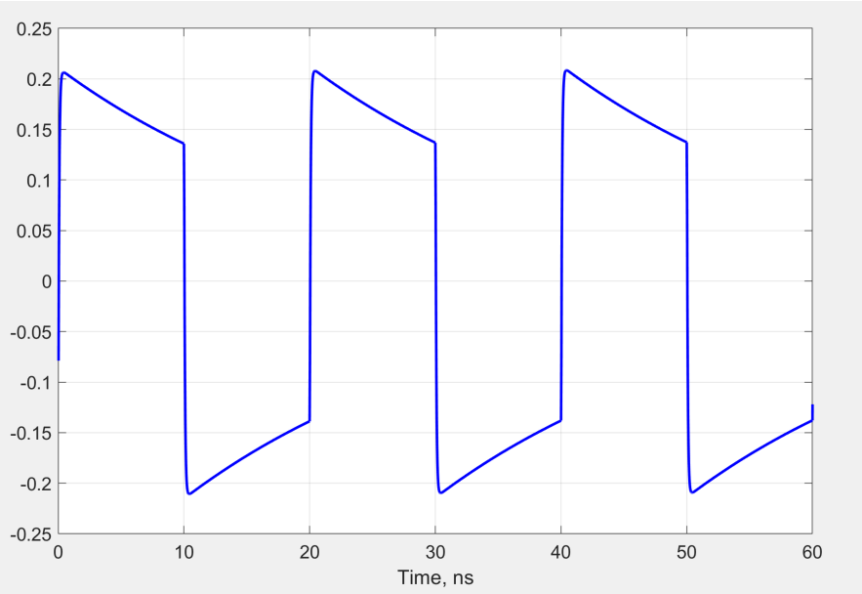


- For Jitter measurements, the measurement BW of the capturing device shall be more than 200MHz.

- The transmitter test fixture2 for MASTER and SLAVE clock jitter measurements

Droop Specification

- When the test mode 6 is enabled, the PHY shall transmit a continuous pattern of 30 {+1} symbols followed by 30 {–1} symbols with the transmitted symbols timed from its local 3GHz clock source.
- With the transmitter in test mode 6 and using the transmitter test fixture 1, the magnitude of both the positive and negative droop shall be less than 24%, measured with respect to an initial value at 2 ns after the zero crossing and a final value at 8 ns after the zero crossing (6 ns period).

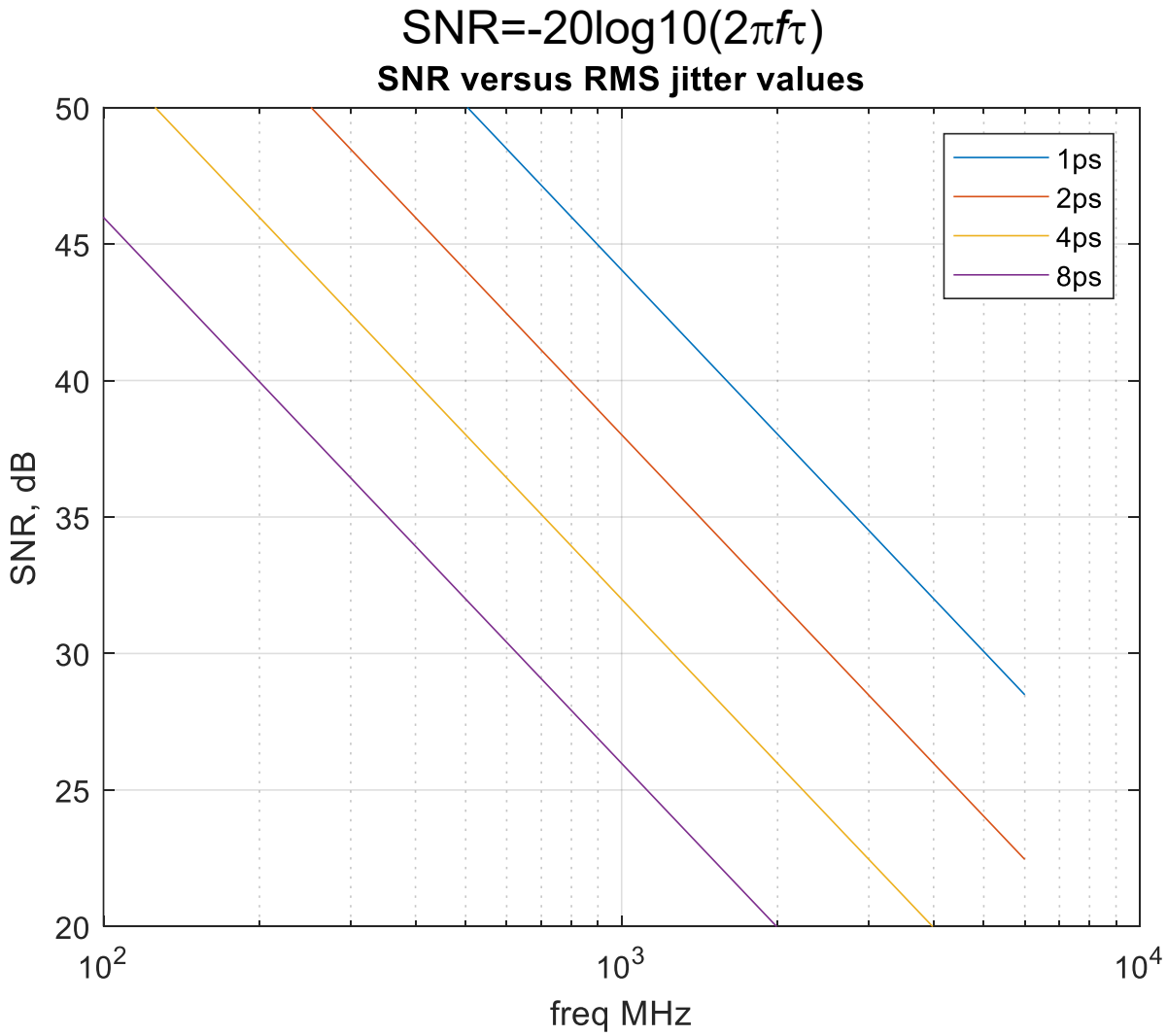


The droop requirement specified to match the MDI RL high pass corner.

Thank you

Questions?

SNR vs RMS Jitter



For a wideband signal, geometric mean of SNR from 10 % of Nyquist to Nyquist calculated to be:

SNR= 35.8dB for 2.5G (4ps) and 5G (2ps).

SNR= 41.8dB for 10G (10ps)