Imager/PHY Integration

IEEE 802.3dm

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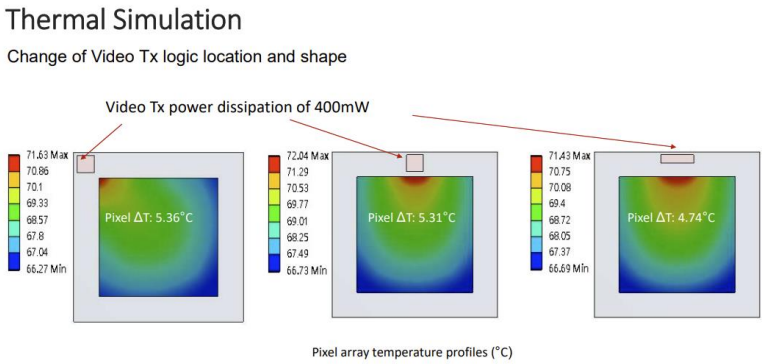
Hiok-Tiaq Ng
Aviva Links Inc.

Supporters

- Claude Gauthier – NXP
- Debajyoti Pal – Onsemi
- Ramanjit Ahuja – Onsemi

Introduction

- Current sensor module implementation
  - Discrete CMOS Image Sensor (CIS) chip
  - Discrete Serializer chip
- Monolithic sensor/PHY solutions reduce power/area/cost/module size
  - Obviates the usual MIPI interface
  - Reduces overall IO count
  - Reduces supply rails (if done right)
- Constraints for integration (Primer below and excerpted →)
  - Modules are small and passively cooled
  - Power dissipation and thermal load have to be managed
  - ISO 10605 level ESD protection migrates to monolithic sensor/PHY
  - Supply rail requirements should ideally coincide



Reference:

Automotive camera side PHY requirements study from CMOS Image Sensor (CIS) perspective

Image Sensor Supplies

- Many CIS are fabricated in 40nm/28nm CMOS technology
  - Suitable for PHY integration and could migrate to 16nm in future
  - CIS usually have three supply voltages
- Lowest supply at 1.1V nominal from below examples
  - Example datasheet showing 2.9V, 1.8V, 1.1V usage
  - Another datasheet of a different CIS showing 3.3V, 1.8V, 1.1V supplies
- 22nm and future 16nm CIS will use lower voltages
  - Low voltage core devices here commonly use 1V supply or lower.

- Integrated PHY should use this ~1V supply as much as possible
  - Ensures minimized power consumption → lower thermal impact on sensor

- References:
  - Wafer fab CIS process node options
  - Example of 3MP camera and its supply voltages
  - Example 5MP camera module and its supply voltages

1V PHY Design

- 1.1V – 10% = ~ 1V after accounting for supply tolerance/IR drop/test margin
- Future 0.9V supply level necessitate designing for 0.81V
- Digital portions of a PHY always use the lowest voltage
- Analog portions of a PHY consist of RX, TX and Clocking/PLL
  - RX: ADC or DFE/Comparator based designs can utilize 0.8V – 1.0V supplies
  - Clock: PLL/Phase Interpolators can also utilize 0.8V – 1.0V supplies
  - TX: DAC/Line Driver supply levels depend on output swing requirements
  - Many examples of above published in IEEE Journal of Solid-State Circuits

PHY TX Low Voltage Design

- Mutiple modalities of TX front end design
  - DAC + Line Driver
    - Line Driver is power hungry if high linearity is required thru Nyquist freq
  - Current mode DAC Driver
    - Usually less power than DAC + Line Driver
  - Voltage mode DAC Driver
    - Usually lowest power implementation
- Focus on *Current* and *Voltage* mode DAC Driver designs

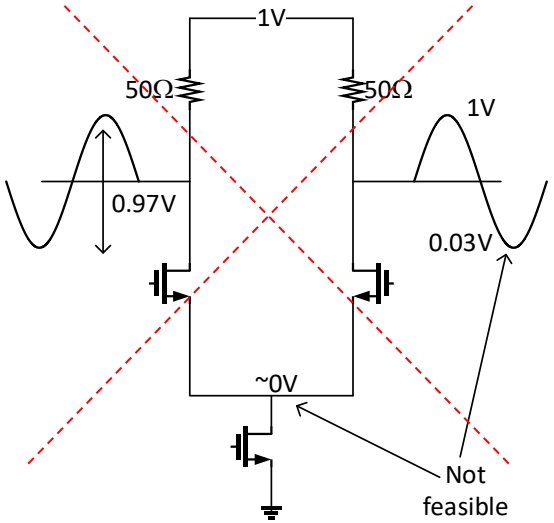
PHY TX Low Voltage Design: *Current* mode DAC

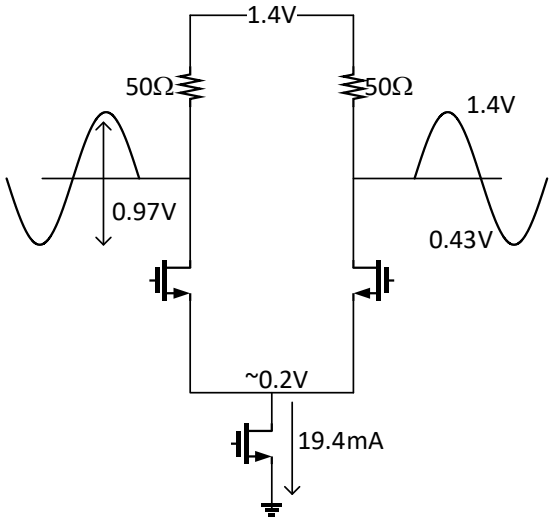
- ACT output swing sum of ↓TX + ↑TX = 0.65Vppse + 0.32Vppse = 0.97Vppse
  - Max swing to offset hybrid cancellation losses in ACT receivers
- TDD output swing = 0.5Vppse

ACT min power config ~1.4V

But only ~3V/1.8V or 1.1V available for shown CIS

19.4mA*1.8V = 34.9mW

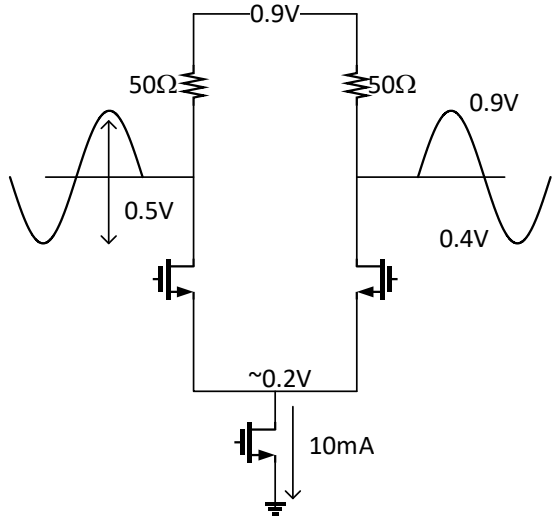




TDD min power config ~0.9V

0.9V not available on shown CIS

10mA*1.1V = 11mW



References:

https://www.ieee802.org/3/dm/public/0125/Chini_3dm_03a_0125.pdf

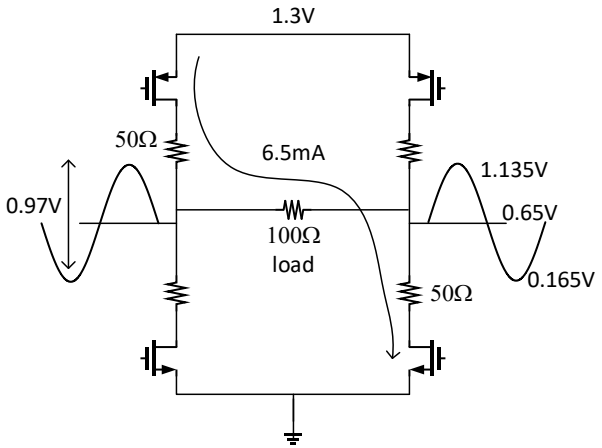
https://www.ieee802.org/3/dm/public/0725/sedarat_3dm_03_202507.pdf

PHY TX Low Voltage Design: *Voltage* mode DAC

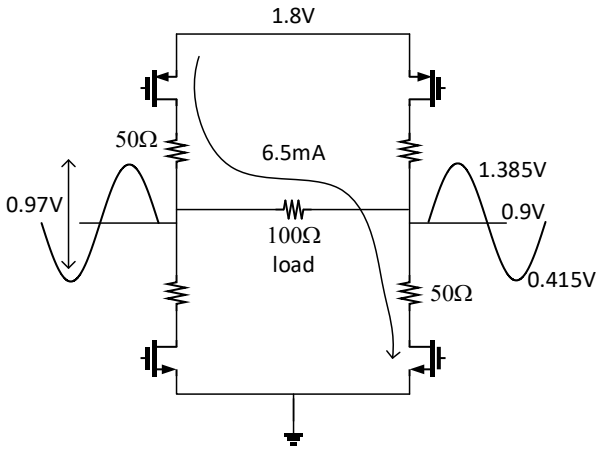
- Basically resistor and switch. Amenable to high speed signalling @ low-V
- ACT swing = 0.97Vppse TDD swing = 0.5Vppse

ACT min power config ~1.3V
But only ~3V/1.8V or 1.1V available on CIS
6.5mA*1.8V = 11.7mW
1.8V switching requires slower IO devices
25Gbps necessitates fast low-V core devices

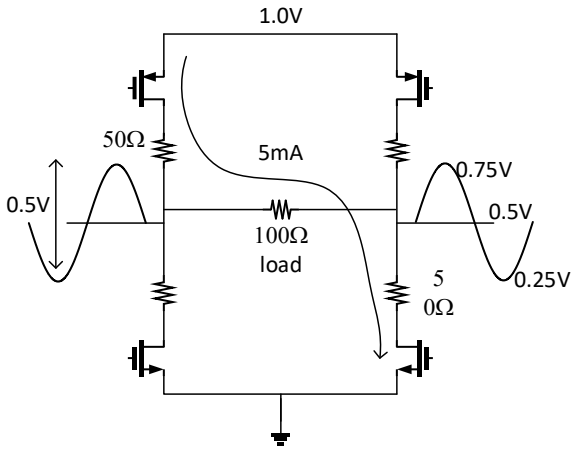
TDD min power config ~1.0V
Available supply config = 5mA*1.1V = 5.5mW
Easier path to 16nm at lower voltages
Easier path to low power 25Gbps TX



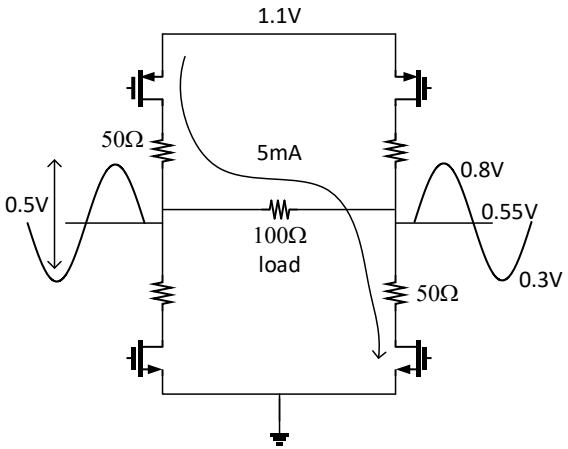
Min supply ACT config



Available supply ACT config



Min supply TDD config



Available supply TDD config

Summary

- Monolithic CMOS Image Sensor/PHY integration is an ultimate goal
  - Lower cost, lower power, smaller modules
  - Cost/power/size further reduced when sensor and PHY share same supplies
- MCM style integration of sensor/PHY also benefits from supply sharing
- Presented basic TX implementations for ACT and TDD

- TDD TX implementation is superior choice
  - Can be implemented with low supply voltages, even below 1V
  - Compatible with lowest supply found on sensors now and in future
  - Low voltages ensure fast core devices can be used, facilitating future higher datarates

- TDD is the right solution for sensor/PHY chip integration, and thus, for 802.3dm

Thank You