

PAM2 to PAM4 Transition in the Training



Key issues

- For both TD and ACT methods, the 10G training symbol is PAM2 while the data mode symbol is PAM4
- Transitioning from PAM2 to PAM4 adds extra steps and complexity
- If a unified sequence is used among the rates, this complexity "trickles down" into 2.5G/5G training
- Two approaches:
 - A) Separate training sequences per rate
 - B) Same training sequences for all rates, but train 10G with PAM4 symbols

ACT proposed training

- Extra complexity:
 - COUNTDOWN is the extra state in the training to move from PAM2 and PAM4 training
- Most of training is done with PAM2, not the intended modulation in the data mode (PAM4)
- An extra step for 2.5G/5G training

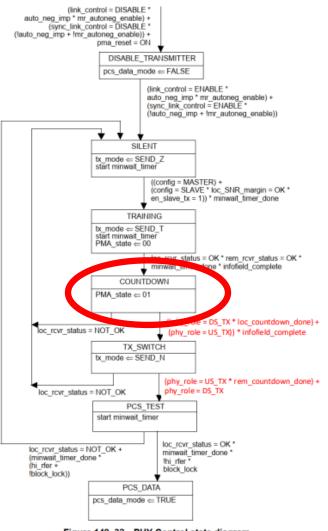


Figure 149–32—PHY Control state diagram

Option A: Separate trainings for lower rates and 10G

– Solution:

Separate simpler training sequence for 2.5G/5G;

– Pros:

- Optimized robustness and simplicity at 2.5G/5G (no PAM mode transition inside training)
- Minimizes risk for established 2.5G/5G interoperability

– Cons:

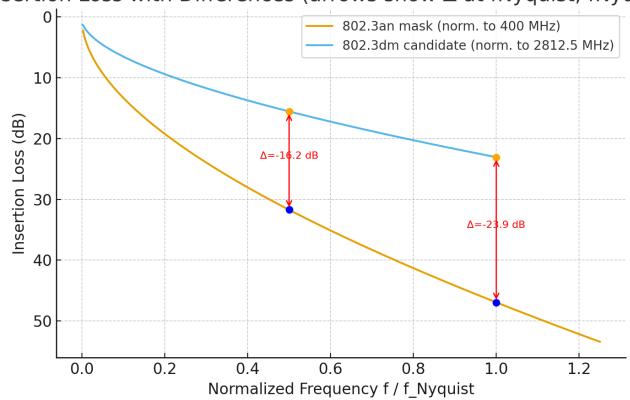
- Two state diagrams to maintain and validate
- Larger firmware/RTL footprint; higher verification/QA effort
- Potential for divergence over time, increasing maintenance costs

Option B: Use PAM4 for 10G training

- Solution:
 - Start 10G training with PAM4 symbols for 10G;
- Pros:
 - One state machine across 2.5G/5G/10G, maximizing reuse
 - Eliminates the PAM2-to-PAM4 mid-training transition at 10G
- Cons:
 - Early PAM4 training is more challenging: d_{min} is 3 times higher from PAM2 compared with PAM4

PAM4: Feasible and proven

Insertion Loss with Differences (arrows show Δ at fNyquist, fNyquist/2)



- Compared to 802.3an (10GBASE-T), which used PAM2 for training, 802.3dm offers much greater margin
- This is not new: IEEE 802.3ck electrical backplane and direct-attach copper PHYs

Conclusion

- Problem:
 - PAM2→PAM4 transition in 10G adds steps;
 - A unified state diagram pushes this complexity into 2.5G/5G.
- Solution: Train 10G directly in PAM4; use one state machine across 2.5G/5G/10G.