IEEE 802.3dm

Test Modes in ACT Upstream Direction

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July 2025

Overview

- IEEE 802.3dm taskforce need to specify test modes
  - To define test procedures and test limits to evaluate the
    - Quality of transmit signal
    - Quality of the clock
    - Performance of the receiver
  - To ensure interoperability of the PHYs
  - To ensure minimum link performance
- There is a proposal for test modes in downstream direction (sedarat_202507)
- This document presents a proposal for test modes in the upstream direction of ACT

Test Modes: ACT - Upstream

ACT transmit signal in the low-speed upstream direction is like that of clause 147 (802.3cg) and clause 188 (802.3da)

- Transmit PSD, power and magnitude
- Transmit linearity
- Timing jitter

Need an additional test for

- Pulse shape
- Linearity
- Proper DME spreading

Measurements and Limits

1. Transmit signal:
   a. PSD mask, and limits on power and signal swing
   b. Droop
   c. Linearity (also covers for pulse shape and Manchester encoding)

2. Clock:
   a. Master frequency precision and stability
   b. Master timing jitter
   c. Slave timing jitter

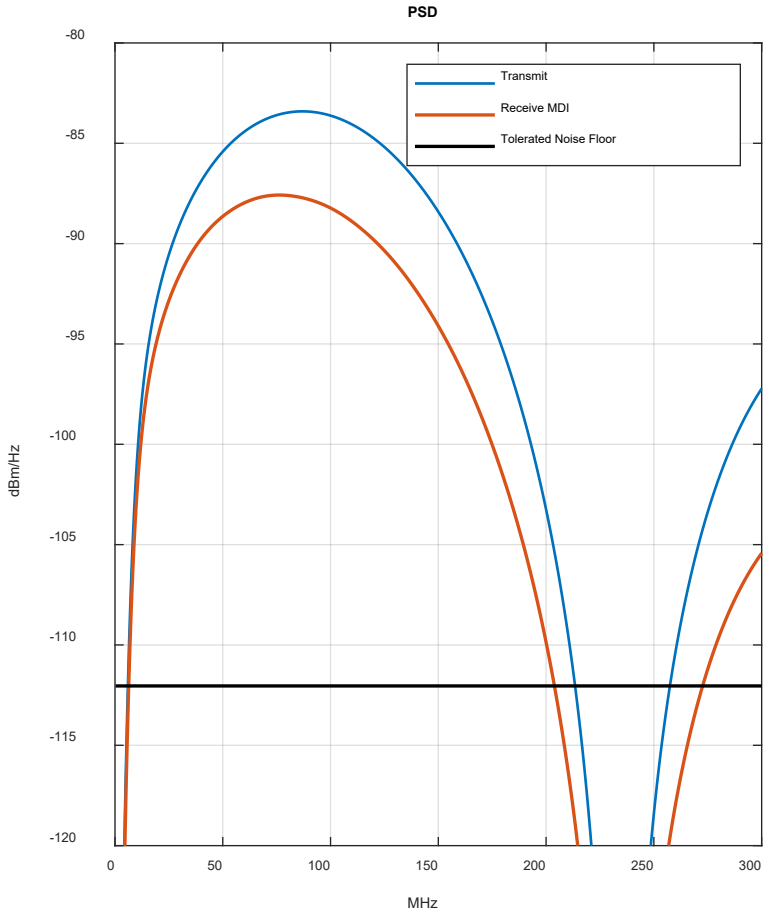
3. Receiver: BER target and tolerated alien crosstalk

Noise Budget

Following the conservative analysis in sedarat_2507_1 and sedarat_2507_2, consider roughly 8 dB of margin to accommodate for the worst-case (artificial) echo power and more than 100 mv of EMI at MDI:

➔ Target SNR = 25 dB

➔ Tolerated noise floor = -112 dBm/Hz



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Transmit PSD Mask, Power, and Swing

Transmit power levels and the PSD mask specified in Sedarat_Cordaro_202505:

Transmit Power (dBm)

	Coax		STP	
	Min	**Max**	**Min**	**Max**
100M	**-6**	**-3**	**-3**	**0**

Starting from the max transmit signal swing specified for 2.5G and 5G, and scaling according to transmit power, the proposed limit for upstream:

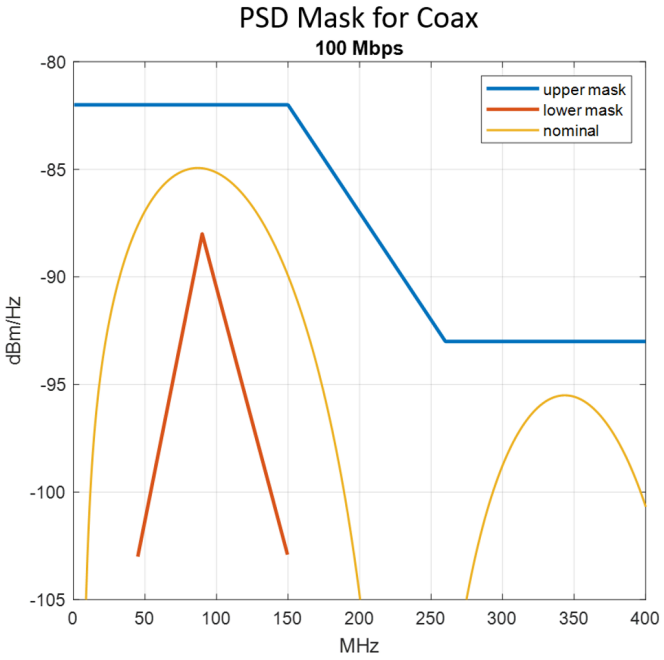
- STP: **0.8 V peak-to-peak**
- Coax: **0.4 V peak-to-peak**

PSD Mask - Upstream

$$UPSD(f) = \begin{cases} P_0 & 0 < f \leq 150 \\ P_0 + 15 - \frac{f}{10} & 150 < f \leq 260 \\ P_0 - 11 & 260 < f \leq 400 \end{cases}$$

$$LPSD(f) = \begin{cases} P_0 - 6 - \left(\frac{90 - f}{3}\right) & 45 < f \leq 90 \\ P_0 - 6 - \left(\frac{f - 90}{4}\right) & 90 < f \leq 150 \end{cases}$$

- P_0 is -82 dBm/Hz for coax, and -79 dBm/Hz for STP
- f is frequency in MHz



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Transmit Droop

- Transmit droop is the low-frequency signal dynamics due to AC coupling of the transmitter at the MDI
- AC coupling results in baseline wander in the received signal and must be kept within acceptable range
- ACT receiver is immune to baseline wander as DME modulation spreads the frequency content of the signal away from DC
- A corner frequency of 10 MHz, which corresponds to small and low-cost PoC circuit, is shown to yield good link performance

➔ Droop should be limited to 30% over 6 ns

Clock Precision and Stability - Leader

- The precision of clock frequency of the link Leader (Master) determines the capture range of initial clock frequency lock in the link Follower (Slave)

- The stability of the clock frequency of the Leader determines the dynamics of the control loop for phase tracking

- Using the clock specification in 149.5.2.6 for upstream direction as it is proven to be not challenging

  ➔ Leader Clock Precision: 50 ppm

  ➔ Leader Clock Stability: 0.1 ppm/second

Clock Precision and Stability - Follower

- The precision of the frequency of the free-running clock of the link Follower (Slave) is of importance only during Link-Synchronization phase

- While Link Synchronization is designed to be robust in presence of frequency offset, there should still be a limit for the case when link Follower operates as crystal-less

➔ Follower Clock Precision: 20%

Timing Jitter – Link Leader

- If configured as the link leader (Master), the upstream transmitter, which is also the source of timing for downstream transmitter, should provide low jitter so that both upstream and downstream receivers can operate within their performance targets

- This means that upstream link leader should follow the same specification of timing jitter as downstream link leader

Downstream Rate	10G	5G	2.5G
Upstream Jitter (ps) Configured as Link Leader	1	1.5	3

* Note that the jitter limits for downstream are derived by scaling the limits from 802.3ch. These numbers should be considered as preliminary and may be relaxed in future.

Timing Jitter – Link Follower

- The timing jitter of the upstream transmitter, which configured as link follower, affects the upstream receiver only
- The upstream receiver's bandwidth is much lower than downstream and can tolerate much higher timing jitter
- Scaling the jitter requirement from downstream by baud rate results in roughly the same level of noise margin as the limits proposed for downstream

➔ Follower Clock Jitter limit: 50 PS RMS

Transmit Linearity

- There is a need for a test of the transmit signal in time-domain to check for
  - Linearity
  - Proper Manchester encoding
  - Pulse shape

- A distortion test, similar to 802.3ch or 802.3bp, can cover all

- A target SNDR = 30 dB can provide roughly the same level of margin as in the proposal for downstream

Alien Crosstalk Noise Level

- The proposed downstream injected noise level offers 14 dB margin (sedarat_2507) with respect to tolerated noise floor

- Following the same margin for upstream

➔ Inject noise level = -126 dBm/Hz

- Injection levels for coax are specified 3 dB lower than STP

Summary

- Proposed limits for the test modes in upstream direction of ACT
  - Transmit signal quality: droop, linearity, power, swing, PSD
  - Clock quality: precision, stability, and jitter
  - Receiver performance

- The test limits for the upstream direction are chosen to yield similar link performance comparing to their counterparts proposed in the downstream direction


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Thank You