# TDD Baseline Proposal for 802.3dm

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# Foreword

- Previously, it was shown that the high speed half duplex transceivers (e.g. 10Gbps SerDes) are widely available and very cost effective compared to full duplex communication systems[1]
  - This technology has matured over the last 20+ and gotten really cost and power efficient with smaller and smaller process geometries
  - The half duplex communication transceivers can provide significant performance advantages and cost efficiencies for 802.3dm project.
- This contribution proposes using a TDD-based solution for 802.3dm.
- Two options are provided using a 8-bit or a 9-bit Reed-Solomon FEC.
- The proposals are compared with a well established and widely tested camera solution over coaxial cables (GMSL2).
- The proposed solution provides optimization on PoC, Ethernet packet encoding, up to 10Gbps support and two choices of FEC.

1. https://www.ieee802.org/3/dm/public/0724/Chini_Tazebay_3dm_01a_0724.pdf

# Outline

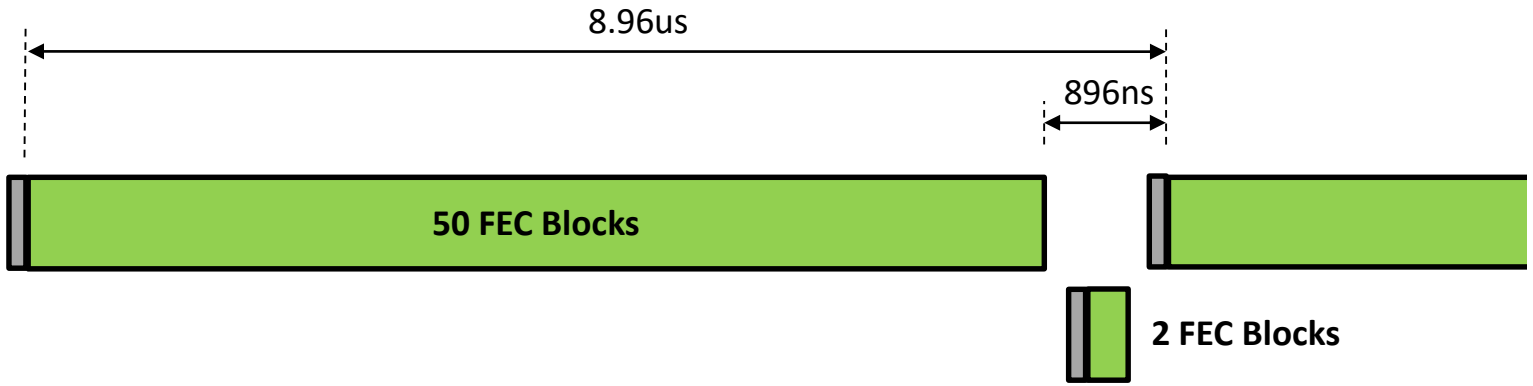
- Existing Solution (GMSL2)
- TDD Baseline Option #1
- TDD Baseline Option #2
- System Parameters
- Implementation Considerations
- Advantages of a TDD-based Solution
- Conclusions

# Existing Solution: GMSL2[1,2]

- Forward link of 3 Gbps/6Gbps with (9b to 10b) encoding (net forward data rate, slightly above 2.5Gbps /5Gbps 802.3dm target rates)
- Reverse link of 187.5Mbps
- Adaptive Equalizer both sides of the link (updated every ~1s)
- Echo cancellation circuit are used on both the serializer and deserializer
- Maximum channel insertion loss of -21dB at 3GHz.
- 1.8V Analog supply, about 180mW typical power.

1. https://www.analog.com/media/en/technical-documentation/data-sheets/max96717.pdf
2. https://www.analog.com/media/en/technical-documentation/data-sheets/max96724.pdf

# TDD Baseline Option #1 (w/8bit RS FEC)

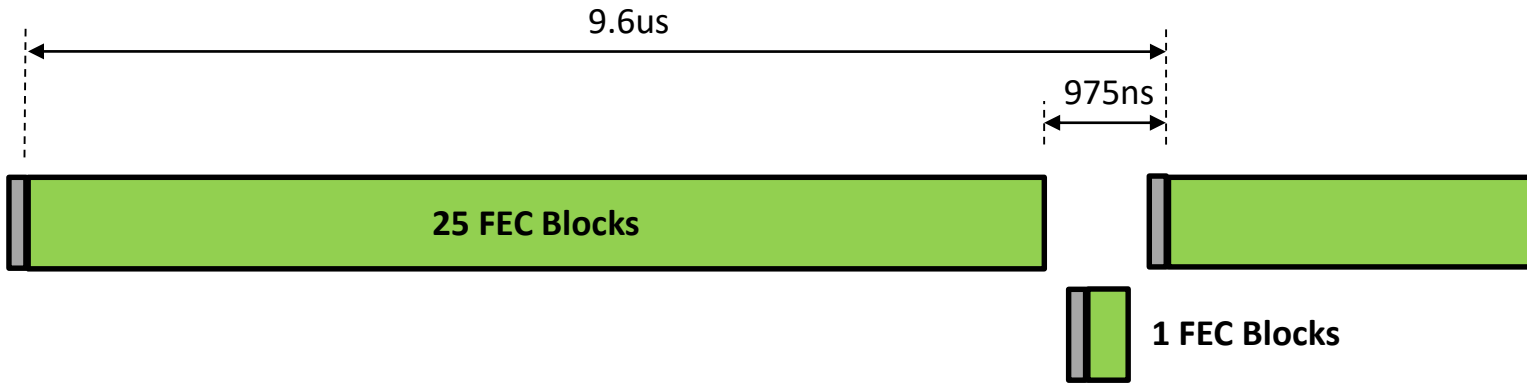



| | |
|---|---|
| **Ethernet Packets Boundary** | 64b/65b encoding |
| **Speed Grades (@ xMII)** | **Forward Link:** 2.5Gbps, 5Gbps & 10Gbps<br>**Reverse Link:** 100Mbps (PAM2, 2.5Gbps line rate) |
| **Modulation** | **PAM2** for 2.5Gbps and 5Gbps<br>**PAM4** for 10Gbps |
| **Baud Rate** | 3.125Gsps for 2.5Gbps (forward and reverse link)<br>6.250Gsps for 5Gbps and 10Gbps (forward link) |
| **TDD Cycle** | 8.96μs for ALL speed grades |
| **FEC block period** | 161.28ns for ALL speed grades |

# TDD Baseline Option #1 (w/8bit RS FEC) (cntd.)

| | |
|---|---|
| **FEC Type** | **S=8bit Reed-Solomon**<br>RS( 63S, 57S) for 2.5Gbps (56Byte at XGMII, 7 x 65b+1b reserve)<br>RS(126S, 114S) for 5.0Gbps (112Byte at XGMII, 14 x 65b+2b reserve)<br>RS(252S, 228S) for 10Gbps (224Byte at XGMII, 28 x 65b+4b reserve)<br>Each FEC block per TDD-cycle carries 50Mbps/100Mbps/200Mbps depending on the line rate |
| **IBG (Inter Burst Gap)** | 104ns between each side transmit time |
| **Total refresh sequence** | 1142bit at 3.125Gsps or<br>2284bit at 6.25Gsps |
| **FIFO** | **Forward Link :** 280-Byte for 2.5Gbps<br>560-Byte for 5.0Gbps<br>1120-Byte for 10Gbps<br>**Reverse Link :** 108-Byte at 100Mbps |
| **Latency** | **Forward link:** ~1.06μs (including one FEC block)<br>**Reverse link:** ~8.80μs (including one FEC block) |

# TDD Baseline Option #2 (w/9bit RS FEC)




| | |
|---|---|
| **Ethernet Packets Boundary** | 80b/81b encoding |
| **Speed Grades (@ xMII)** | **Forward Link:** 2.5Gbps, 5Gbps & 10Gbps<br>**Reverse Link:** 100Mbps (PAM2, 2.5Gbps line rate ) |
| **Modulation** | **PAM2** for 2.5Gbps and 5Gbps<br>**PAM4** for 10Gbps |
| **Baud Rate** | 3.0Gsps for 2.5Gbps (forward and reverse link)<br>6.0Gsps for 5Gbps and 10Gbps (forward link) |
| **TDD Cycle** | 9.6μs for ALL speed grades |
| **FEC block period** | 345ns for ALL speed grades |

# TDD Baseline Option #2 (w/9bit RS FEC) (cntd.)

| | |
|---|---|
| **FEC Type** | **S=9bit Reed-Solomon**<br>RS(115S, 108S) for 2.5Gbps (120Byte at XGMII, 12 x 81b)<br>RS(230S, 216S) for 5.0Gbps (240Byte at XGMII, 24 x 81b)<br>RS(460S, 432S) for 10Gbps (480Byte at XGMII, 48 x 81b)<br>Each FEC block per TDD-cycle carries 100Mbps/200Mbps/400Mbps depending on the line rate |
| **IBG (Inter Burst Gap)** | 104ns between each side transmit time |
| **Total refresh sequence** | 1266b at 3Gsps<br>2532b at 6Gsps |
| **FIFO** | **Forward link :** 304-Byte for 2.5Gbps<br>608-Byte for 5.0Gbps<br>1216-Byte for 10Gbps<br>**Reverse link :** 116-Byte at 100Mbps |
| **Latency** | **Forward link:** ~1.3us (including one FEC block)<br>**Reverse link:** ~9.6us (including one FEC block) |

# System Parameters

| | GMSL2 | TDD w/9b FEC | TDD w/8b FEC |
|---|---|---|---|
| **2.5Gbps Modulation & Baud rate** | PAM2, 3Gsps | PAM2, 3Gsps | PAM2, 3.125Gsps |
| **5.0Gbps Modulation & Baud rate** | PAM2, 6Gsps | PAM2, 6Gsps | PAM2, 6.25Gsps |
| **10Gbps Modulation & Baud rate** | X | PAM4, 6Gsps | PAM4, 6.25Gsps |
| **GPIO Delay Compensated Reverse link** | 10-15µs | ~10µs | ~9.2µs |
| **GPIO Jitter** | +/-10ns | +/-4ns | +/-4ns |
| **Low cost and power equalizer** | Yes | Yes+ lower Voltage | Yes+ lower Voltage |
| **Echo Canceller** | Yes, both sides | No | No |
| **Ethernet** | X | Yes | Yes |
| **PoC** | Ok (+22µH) | Best (1µH) | Best (1µH) |
| **Linkup time From power up** | 45ms | <45ms | <45ms |

# System Parameters (cntd.)

| | GMSL2 | TDD w/9b FEC | TDD w/8b FEC |
|---|---|---|---|
| **Crystal-less Camera** | Yes | Yes | Yes |
| **FEC** | RS-7bit, ~5% parity<br>Optional | RS-9bit, ~6% parity | RS-8bit, ~10% parity |
| **Video Latency** | +(1-2)µs | 1.3µs | 1.1µs |
| **Reverse link** | 187.5Mbps | 100 Mbps | 100 Mbps |
| **FIFO, forward link** | No | Yes (see Implementation) | Yes (see Implementation) |
| | | | |

# Implementation Considerations

- **FIFO Implementation cost:** A 1200B FIFO running at 6GHz (16b x 750MHz) takes ~0.006mm$^2$ to build in 16nm technology. That is less than 5% of a SerDes type transceiver design[1] which is the most cost efficient implementation used in many image sensor applications.
- **OAM:** One or more RS FEC symbols may be dedicated to OAM.
- **Camera side FEC decoding:** Error correction is optional in the camera side. Algebraic single symbol RS decoding along with syndrome calculation for error detection may be considered.
- **Delay Compensated GPIO:** The inherent time accuracy of TDD cycles may be compensated for propagation delay to drive GPIO with about 10µs delay and with +/-4ns accuracy for time critical synchronization.
- **Crystal-less Camera:** TDD signaling sent to reverse link is from a free running transmitter that is based on a local crystal. The signaling provides two accurate clock reference for camera to tune its local VCO. A continuous TDD cycling (~100kHz) and a 3GHz high resolution bursts. Together, they are used to track frequency and set the VCO input Voltage. Similar to SerDes type receivers, fast tracking capability of TDD allows rejecting low frequency jitter and baseline wander (if any). Initial tuning and locking of the camera frequency happens during start up.

1- https://www.ieee802.org/3/dm/public/0724/Chini_Tazebay_3dm_01a_0724.pdf

# Advantages of a TDD-based Solution

- **Modulation:** PAM2 is considered with highest ingress noise margin for 2.5G/5G. It has been proven in the field over coaxial with a very large number of successful implementations even with an optional FEC and low power low complexity equalizers[1] (GMSL2 and others).
- **Synchronization:** The inherent timed operation of TDD simply allows for multi camera synchronization in a typical implementation. For a large network development, PTP may be used as well.
- **Camera initialization:** Startup can be a lot faster for reverse link than normal mode using reduced TDD cycles (TBD, up to 10X). That helps initialize cameras much quicker than normal.
- **PoC:** TDD allows using a small inductor down to 1µH which in-turn allows for much smaller boards with lower power and complexity as well as improved cross talk.
- **Loop Timing:** Loop timing is not a requirement for TDD but the camera frequency may be locked through the link instead of using a local crystal.

1- https://www.ieee802.org/3/dm/public/0724/Chini_Tazebay_3dm_01a_0724.pdf

# Advantages of a TDD-based Solution (cntd.)

- **Single Chip Solution:** While a camera use case may benefit from a two-chip solution, many applications may be addressed with a single configurable chip given 2.5Gbps rate is used in both sides of a TDD PHY
- **Clock Requirement:** Unlike 802.3ch which requires longer term stable clocking (measured over 1ms), TDD uses fast SerDes type clock recovery (e.g. measured above ~1MHz and over ~1-2us) in forward link.
- **Flexible Rates:** For camera use cases, 100Mbps reverse link is sufficient. For applications requiring higher reverse rates, the TDD examples in this document, are flexible enough to support (e.g. 10G/400M, 9.6G/1G, 2G/600M, etc.) and subject to consideration.

# Conclusions

- Two TDD baseline examples provided to show possibilities and also to make it clear the solution is flexible and open to incorporate contributions from other 802.3dm participants.
- For modulation, the proposal follows the well established practice of using PAM2 for baud rates up to about 6Gsps. PAM2 provides highest margin for ingress noise for 2.5Gbps and 5Gbps xMII rates.
- While GMSL2 FEC is optional, stronger FEC incorporated into the TDD baselines.
- The proposed TDD baselines allow simple and power efficient analog type equalization used in SerDes and most of the existing camera solutions.
- The additional advantages of TDD enable flexible and single chip PHY solutions for many other application beyond camera (including display).
- Constructive comments and contributions are very welcome.

Thank you for your attention!

Questions?