TDD Benefits and Baseline Proposal for 802.3dm

IEEE 802.3dm

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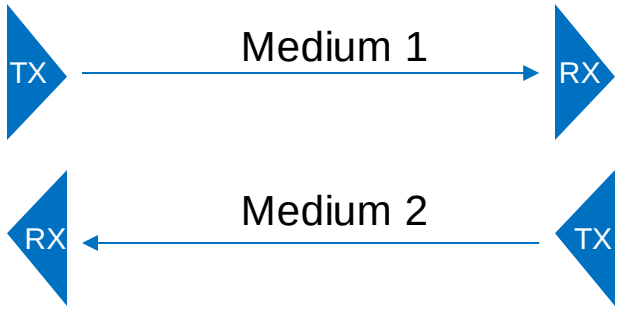
Listed in no particular order

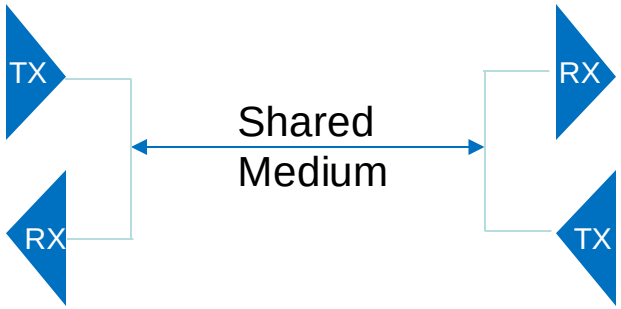
What is TDD?

"Normal" SERDES



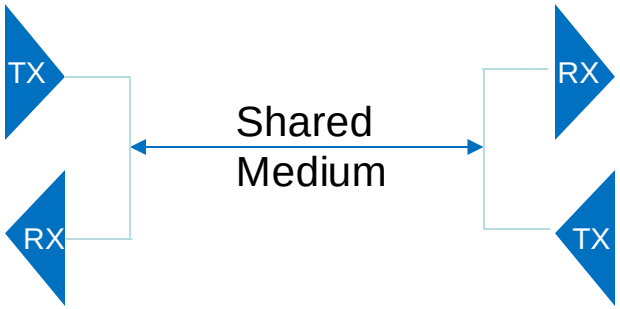
- **Simultaneously** transmit and receive on **2 separate mediums**
- Each side RX performs equalization but no additional complications
- Works well when two separate channels are available
- Almost all data-center SerDes work like this.

Symmetrical" PHYs



- **Simultaneously** transmit and receive on **1 shared medium**
- Each side performs equalization and very complex signal processing/ echo-cancellation
- Often used when 1 medium is available and bandwidth is **Symmetrical in both directions**
- Most Base-T PHYs work like this

Asymmetrical PHYs



- **Non-Simultaneously** transmit and receive on **1 shared medium**
- Each side RX performs equalization but no complicated echo cancellation
- Generally used when the bandwidth requirement is not the same in both directions
- Several Billion Asymmetrical communications Semiconductors shipped per year work like this

This is TDD!

Who uses TDD? Is it New?

- TDM/TDD is by far the most widely used communication technology on the Planet for Asymmetrical bi-directional communication

- Examples of TDM (Note that TDD is TDM applied to 2 nodes)
  - WiFi – 4 Billion per year
  - Bluetooth – 5 Billion per year
  - Both are Asymmetrical and Bi-directional!

- No other technology comes anywhere close to total of these numbers for yearly port shipments

- In contrast – Are there any chips shipping per year using “ACT”?

But that is Wireless. What about Wired?

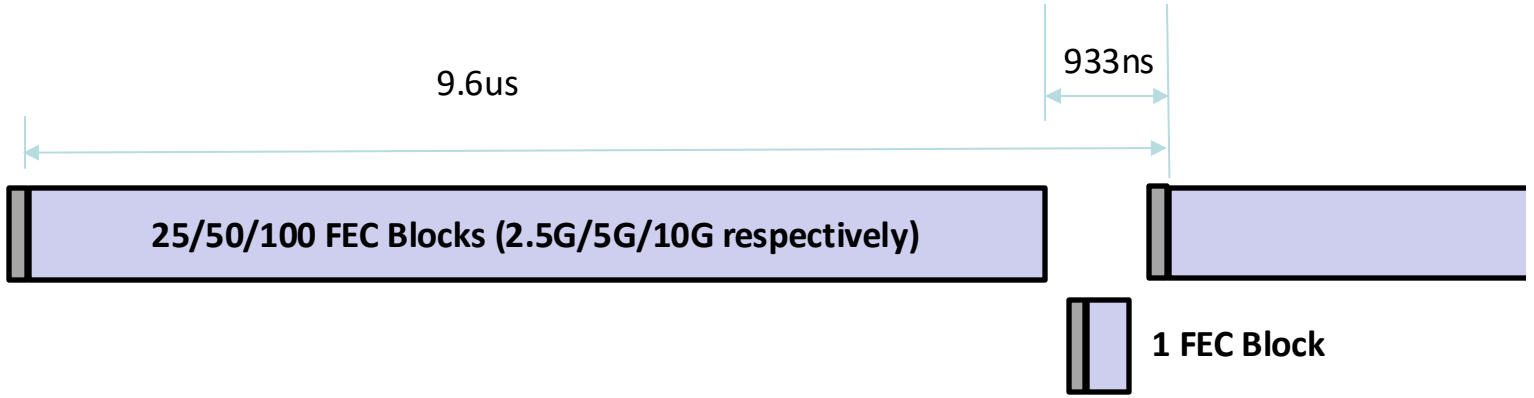
- ASA recognized early on that automotive SerDes should be optimized for Asymmetry
- Based on this as one of the key factors, ASA chose TDD back in 2020
- **"Ten Semiconductor Suppliers to Contribute to the Automotive SerDes Market with ASA-Motion Link Compliant Semiconductor Products within the next Year"**
  - https://auto-serdes.org/news/asa-successfully-establishes-multi-vendor-market-for-camera-and-display-connectivity-953/
- 3 companies have already shown ASA Quad Devices

Is there precedence for TDD in IEEE 802?

- IEEE 802 has a long legacy of TDM (remember TDD is a subset)
  - 802.11 PHYs (WiFi) have predominantly used TDM
  - 802.3 PHYs are traditionally focused on Symmetrical communication rather than Asymmetrical communication. Hence, the general lack of TDD in the past
  - Some 802.3 PHYs have elements of TDM
    - 10Base-T1 is TDM (with Collison avoidance)
    - EPON is TDM (?)

- Given the Asymmetrical nature of automotive applications, it is time for 802.3 to move to TDD
  - Forward direction (Video)
    - TDD results in the Simplest possible TX and RX
    - Any form of “overlapping” signals is more complex than non-overlapping signals at about the same baud rate and same modulation
  - Reverse direction (control)
    - TDD can result in very simple TX and RX
    - Depends on the choice of baud rate and modulation

TDD Baseline Proposal (w/8bit RS FEC)



Speeds	**Forward (video) Direction:** 2.5Gbps, 5Gbps & 10Gbps **Reverse (control) Direction:** 100Mbps (using base of 2.5Gbps)
Modulation	**PAM2** for 2.5Gbps and 5Gbps **PAM4** for 10Gbps
Baud Rate	3.00Gsps for 2.5G (forward and reverse link) 6.00Gsps for 5G and 10G (forward link)
TDD Cycle	9.6µs for ALL speeds
FEC block period	346.66ns for ALL speeds (including interleaving)
Coding at xMII	64b/65b

TDD Baseline Proposal (w/8bit RS FEC) – Continued

FEC Type	**S=8bit Reed Solomon** RS(122S, 130S) for 2.5G (120 Bytes at XGMII, 15 x 65b+1b reserve) RS(122S, 130S) for 5G (120 Bytes at XGMII, 15 x 65b+1b reserve) RS(122S, 130S) for 10G (120 Bytes at XGMII, 15 x 65b+1b reserve) 5G 2x interleaving 10G 4x interleaving
IBG (Inter Burst Gap)	104ns
Resync bits	568 bits for 2.5G 1136 bits for 5G 2272 bits at 10G
FIFO size	Similar to TDD proposal by Ahmad Chini and Mehmet Tazebay
PHY Delay	**Forward Direction:** ~1.28us (including one FEC block) **Reverse Direction:** 9.6µs (including interleaved FEC block)

Comparison of System Parameters

	Proprietary SerDes	TDD w/9b FEC (Chini and Tazebay option 2)	TDD w/8b FEC (Chini and Tazebay option 1)	TDD w/8b FEC Interleaved (this proposal)
2.5Gbps Modulation & Baud rate	PAM2 3Gsps	PAM2 3.00Gsps	PAM2 3.125Gsps	**PAM2** **3.00Gsps**
5.0Gbps Modulation & Baud rate	PAM2 6Gsps	PAM2 6.00Gsps	PAM2 6.25Gsps	**PAM2** **6.00Gsps**
10Gbps Modulation & Baud rate	?	PAM4 6.00Gsps	PAM4 6.25Gsps	**PAM4** **6.00Gsps**
GPIO Delay * Compensated Reverse Direction	Up to 15us MAX96717 – **Table 9** Up to 12.2us DS90UB953 - **Table 7-5**	~10us	~9.2us	~9.2us
GPIO Jitter	+/-10ns - MAX96717 12us - DS90UB953 - **Table 7-5**	+/-4ns	+/-4ns	+/-4ns
Low cost and power equalizer	Yes	Yes+ lower Voltage	Yes+ lower Voltage	Yes+ lower Voltage
Echo Canceller	Yes, Both sides	No	No	No
Ethernet	X	Yes	Yes	Yes

* For timing sensitive aspects such as Frame Sync, compensated mode provides lower jitter and hence is more appropriate to consider. Values are for the “reverse direction”.

System Parameters (cntd.)

	Proprietary SerDes	TDD w/9b FEC (Chini and Tazebay option 2)	TDD w/8b FEC (Chini and Tazebay option 1)	TDD w/8b FEC Interleaved (this proposal)
Crystal less Camera	Yes	Yes	Yes	Yes
FEC	RS-7bit, ~5% parity Optional	RS-9bit, ~6% parity	RS-8bit, ~10% parity	RS-8bit, ~10% parity
PHY Delay for video direction	1 to 2us	1.3us	1.1us	~1.1us
Reverse link	187.5Mbps	100 Mbps	100 Mbps	100 Mbps
xMII	**N/A**	**80b/81b**	64b/65b	**64b/65b**
PHY Level OAM bits	N/A	TBD	TBD	**1 bit per RS Frame**
PoC	Ok (22+uH)	Best (1uH)	Best (1uH)	Best (1uH)
Linkup time	45ms	<45ms	<45ms	<45ms

Summary of the TDD Baseline Proposal

				Dn = Downnstream (Forward Direction)							Up = Upstream (Reverse Direction)												
				Per RS frame				Burst			Per RS frame												
Dn Line Rate [Gbps]	Up Line Rate [Gbps]	Resync Header [ns]	IBG [ns]	64/65 blocks	OAM bits	Payload bytes	Parity bytes	# of RS frames Per burst	Length [bits]	Length [ns]	64/65 blocks	OAM bits	Payload bytes	Parity bytes	# of RS frames Per burst	Length [bits]	Length [ns]	Total time Dn [ns]	Total time Up [ns]	Total TDD Cycle [ns]	Dn Payload per burst [bits]	**Dn Data Rate [Gbps]**	Up Payload per burst [bits]	**Up Data Rate [Mbps]**
3	3	189.333	104	15	1	122	8	25	26000	8666.7	15	1	122	8	1	1040	346.6666667	8856.0	536.0	9600.0	24000	**2.5000**	960	**100.0**
6	3	189.333	104	15	1	122	8	50	52000	8666.7	15	1	122	8	1	1040	346.6666667	8856.0	536.0	9600.0	48000	**5.000**	960	**100.0**
12	3	189.333	104	15	1	122	8	100	104000	8666.7	15	1	122	8	1	1040	346.6666667	8856.0	536.0	9600.0	96000	**10.000**	960	**100.0**

- ✓ 3.00Gsps and 6.00Gsps signaling
- ✓ 64b/65b - maps nicely to existing 802.3 framework (xMII)
- ✓ Same FEC base for all speeds
- ✓ Dedicated PHY OAM bits
- ✓ Excellent PHY Delay profile
- ✓ Low complexity implementation – no echo cancellation at all!

Simple, efficient and optimized to meet all the adopted objectives!!

Thank You!

Your feedback is welcome and will be used to improve the proposal.

Looking forward to building consensus.