Integration into Cameras

Contribution to 802.3dm Task Force

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Introduction

- In this presentation, we share ways to optimize 802.3dm solutions to provide camera integration options

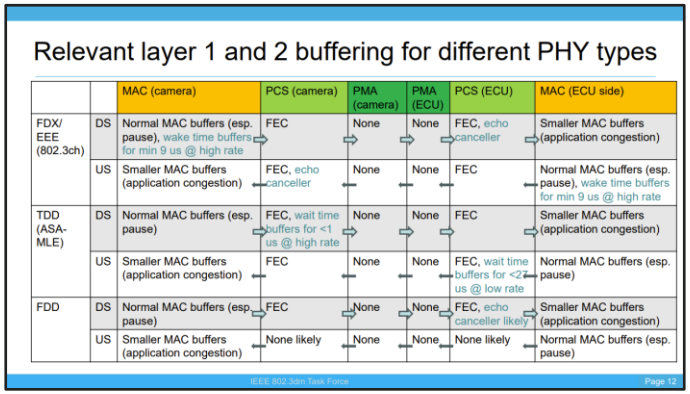
Discussion Topics:

- Technology comparison
- Latency and Buffer Requirements
- Equalization Need in TDD vs ACT
- Power and Thermal Management

Competing solutions – Summary

	Incumbents	Ethernet 802.3ch	Ethernet 802.3dm	
	GMSL/ FPD-Link	802.3ch/ EEE	ASA-MLE / TDD	ACT
Standard	Proprietary	IEEE	Alliance	IEEE Proposal
Latency	++	+	–	+
Imager integration	Not Available	–	–	+
Relative Silicon size	+	–	–	+
Xtal-less	+	–	–	+
PoC filter	–	+	+	+

Latency and Buffering Requirements – Sensor Side



Relevant layer 1 and 2 buffering for different PHY types

		MAC (camera)	PCS (camera)	PMA (camera)	PMA (ECU)	PCS (ECU)	MAC (ECU side)
FDX/ EEE (802.3ch)	DS	Normal MAC buffers (esp. pause), wake time buffers for min 9 us @ high rate	FEC	None	None	FEC, echo canceller	Smaller MAC buffers (application congestion)
	US	Smaller MAC buffers (application congestion)	FEC, echo canceller	None	None	FEC	Normal MAC buffers (esp. pause), wake time buffers for min 9 us @ high rate
TDD (ASA-MLE)	DS	Normal MAC buffers (esp. pause)	FEC, wait time buffers for <1 us @ high rate	None	None	FEC	Smaller MAC buffers (application congestion)
	US	Smaller MAC buffers (application congestion)	FEC	None	None	FEC, wait time buffers for <2 us @ low rate	Normal MAC buffers (esp. pause)
FDD	DS	Normal MAC buffers (esp. pause)	FEC	None	None	FEC, echo canceller likely	Smaller MAC buffers (application congestion)
	US	Smaller MAC buffers (application congestion)	None likely	None	None	None likely	Normal MAC buffers (esp. pause)

IEEE 802.3dm Task Force Page 12

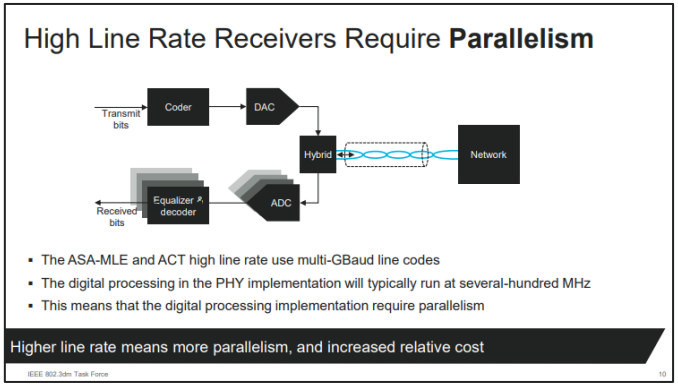
Data Rates	Latency – High Speed (µsec)	ASA-MLE Buffer [bytes]	ACT Buffer Size	ASA/ACT Line Rate Ratio
2.5G/100M	1.1	344	No Latency	x344
5G/100M	0.832	520	No Latency	x520
10G/100M	0.912	1140	No Latency	x1140

ACT does NOT require additional memory buffers

Reference: https://ieee802.org/3/dm/public/0724/matheus_dm_02b_latency_07152024.pdf

Reference: https://ieee802.org/3/dm/public/0724/matheus_dalmia_dm_03b_buffering_07152024.pdf

Equalization Need in TDD vs ACT – 100Mbps RX



2.5G/5.0G – TDD at least 200% bigger than ACT due to Equalizers and/or ADC size on 100Mbps RX Sensor side

- >100% PHY increase for basic EQ/ADC – (DFE and CTLE)
- >100% PHY increase for adaptive EQ and DFE
  - Real time adjustments

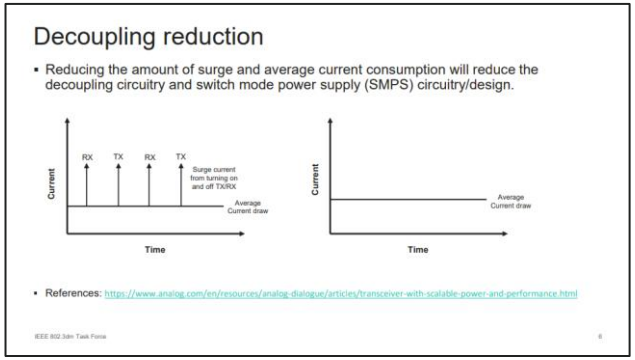
- High speed requirements for TDD >5Gbps – may require Full Adaptive Equalization
  - Common for practice for applications that need ISI correction, frequency compensation, and dynamic adaptation

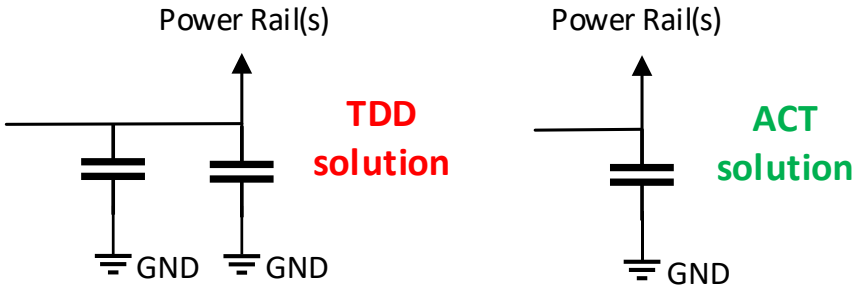
ACT PHYs can operate without equalizer(s)

Reference: https://ieee802.org/3/dm/public/0924/jonsson_3dm_01_09_15_24.pdf

Power and Thermal Management

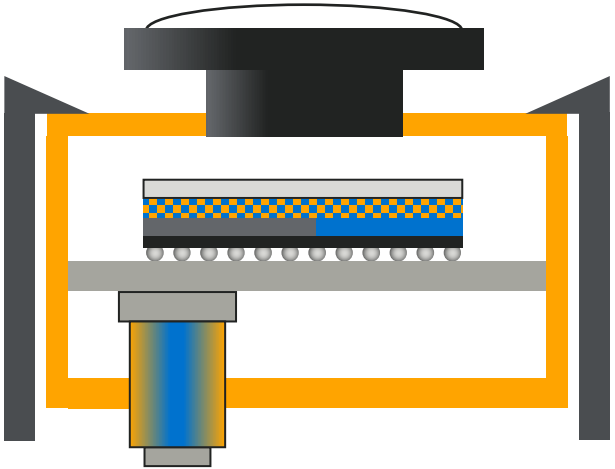
- Rapid switching between TX and RX causes **current fluctuations** especially when each component transitions in and out of active states.
- **TDD system require additional power management circuitry** to stabilize power and reduce noise during transitions from idle to active states





Reference: https://ieee802.org/3/dm/public/0724/houck_3dm_01_0724.pdf

For imager integration, ACT is much better



Compared to other candidates, ACT offers:

- Smaller size = < Power Dissipation
- Lower complexity
- Better suitability for older process nodes

Unlike full-duplex and TDD approaches, ACT can be cost-effectively implemented in process nodes typically used for image sensors, for both low speed and higher link speeds (receiver is always 100Mbps)

See more details in https://www.ieee802.org/3/dm/public/0924/jonsson_razavi_3dm_01_09_15_24.pdf

Summary

1. Simplified Receiver Design: ACT 100Mbps receiver does not require high speed components – **smaller and more power efficient**

2. Continuous data flow in ACT **eliminates the need for buffers** required to manage burst data in TDD

3. ACT use independent TX and RX paths **provide simple, low power, and more space-efficient circuitry**. Critical for asymmetric data rates

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