PHY Delay Survey

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November 11, 2024

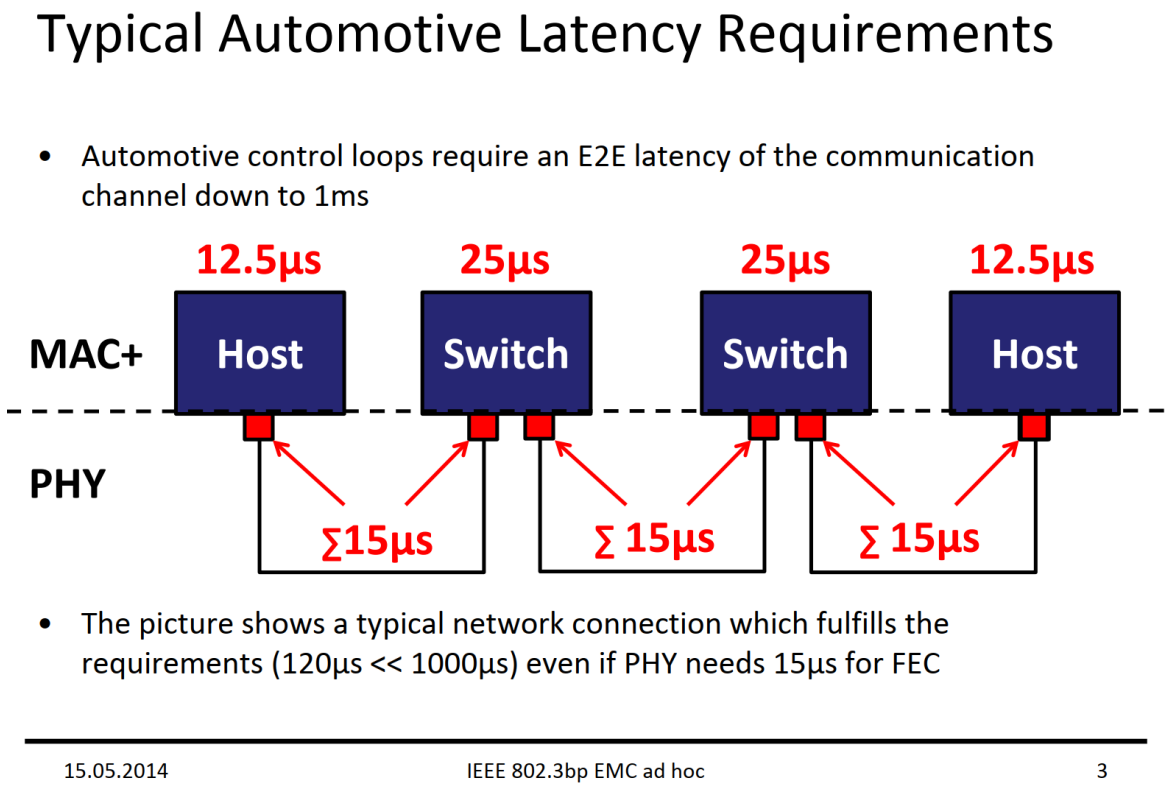
Recommended PHY Delay Values

- Presented / supported by individuals from 5 different OEMs in May 2014
- https://grouper.ieee.org/groups/802/3/bp/public/may14/Krieger_3bp_01_0514.pdf

- Recommends 15 us PHY latency

- To meet automotive control loops

- Unlikely that OEMs today will want greater PHY latency vs 10 years ago
  - If anything, less latency is better



Incumbent Solutions

- Public information from datasheets
- Incumbent solutions all well under 15us

PHY	Reference	Condition	Delay us
FPD-Link III	DS90UB953 Table 6-6	GPIO Forward Channel	0.225
FPD-Link III	DS90UB953 Table 6-7	GPIO Back Channel	1.5/3.2
FPD-Link IV	DS90UB954 Section 7.5.3.1	I2C - PHY Forward Channel piece only	0.225
FPD-Link IV	DS90UB954 Section 7.5.3.1	I2C - PHY Reverse Channel piece only	1.5
GMSL-2	MAX96717F Table 9	GPIO - Forward Link, no delay compensation	1.0
GMSL-2	MAX96717F Table 9	GPIO - Reverse Link, no delay compensation	6.0
GMSL-2	MAX96724/F/R Table 6	I2C - Forward Link	< 10
GMSL-2	MAX96724/F/R Table 6	I2C - Reverse Link	< 10

All BASE-T1 PHYs to Date

- Some specify transmit PHY and receive PHY separately
  - TX MII to MDI, MDI to RX MII
- Some specify transmit + receive total
  - TX *MII to RX *MII
- All well under 15us

PHY	Reference	Condition	Transmit us	Receive us	Delay us
10BASE_T1L	Clause 146.10	transmit + receive	3.2	6.4	9.6
10BASE-T1S	Clause 147.11	Worst case transmit + receive	0.44	4.0	4.44
100BASE-T1	Clause 96.10	transmit + receive	0.36	0.96	1.32
1000BASE-T1	Clause 97.10	merged transmit + receive			7.168
2.5GBASE-T1	Table 149-20	merged transmit + receive			4.096
5GBASE-T1	Table 149-20	merged transmit + receive, 1X interleave			2.048
5GBASE-T1	Table 149-20	merged transmit + receive, 2X interleave			2.7648
10GBASE-T1	Table 149-20	merged transmit + receive, 1X interleave			1.024
10GBASE-T1	Table 149-20	merged transmit + receive, 2X interleave			1.3824
10GBASE-T1	Table 149-20	merged transmit + receive, 4X interleave			2.048
25GBASE-T1	Table 165-18	merged transmit + receive, 1X interleave			1.024
25GBASE-T1	Table 165-18	merged transmit + receive, 2X interleave			1.47456
25GBASE-T1	Table 165-18	merged transmit + receive, 4X interleave			2.3552
25GBASE-T1	Table 165-18	merged transmit + receive, 8X interleave			4.096

Estimated Delays From Ongoing Standards

- Estimated delay values are in the ballpark achievable delay but not yet agreed upon
  - Maximum numbers permitted for a compliant device
- Algorithm delay is the minimum theoretically possible delay
  - Assume delay from implementation is 0ns

PHY	Reference	Condition	Algorithm Latency us	Estimated Delay us
100BASE-T1L	802.3dg	Low Latency Mode merged transmit + receive	0.64	1.2
100BASE-T1L	802.3dg	500m Long Reach Mode merged transmit + receive	10.69	13.0
Lo_3dm_02_0924.pdf		merged transmit + receive upstream	1.284	2.0
Lo_3dm_02_0924.pdf		merged transmit + receive downstream		See 2.5/5/10GBASE-T1
jonsson_3dm_01_09_15_24.pdf		merged transmit + receive upstream	2.12	3.2
jonsson_3dm_01_09_15_24.pdf		merged transmit + receive downstream		See 2.5/5/10GBASE-T1

Conclusion

- Recommend group adopt 15us as the maximum PHY transmit + receive delay in either direction
- Incumbent solutions as well as all BASE-T1 PHYs to date easily meet the 15us limit
- We should work to come in well under this target number

THANK YOU